

THERMAL STABILITY AND IV CHARACTERISTICS OF *IN-SITU* EPITAXIAL AL ON GaAs P-HEMT GROWN BY SOLID SOURCE MBE.

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ABSTRACT

The fabrication and characterisation of AlGaAs/InGaAs/GaAs pseudomorphic-HEMT (p-HEMT) with *in-situ* deposited epitaxial aluminium gate by MBE is reported. A simpler technique of fabricating HEMT without the inherent problem associated with gate recess is described. Its advantages over conventional method of fabricating HEMT are also shown. The near ideal epitaxial-Al/AlGaAs Schottky barrier contact is exploited in this work, resulting to an excellent I-V and thermal treatment characteristics. This epitaxial Al diodes have better ideality factor, higher barrier height and higher breakdown voltage but high series resistance than that of Au diodes.

INTRODUCTION

The AlGaAs/InGaAs/GaAs pseudomorphic HEMT has been widely investigated ever since it was introduced by Ketterson et al [1] in 1985. Since then, tremendous progress on the device's material structure and fabrication techniques have been made for use in a large range of application, especially in radar and communication. However, the AlGaAs/InGaAs/GaAs p-HEMT superiority is now being surpassed by better performance from InGaAs/InAlAs/InP and InGaP/InGaAs/GaAs structure devices [2-5].

The conventional AlGaAs/InGaAs/GaAs p-HEMT device performance suffers badly due to high leakage current and low gate to drain breakdown voltage. Its first major problem in device fabrication is the difficulty in getting a uniform and reproducible wet etchant selectivity of the GaAs cap layer over the AlGaAs supply layer [6-7]. This process is critical in order to control the threshold voltage of the device. Ideally, the etch process should be selective enough to stop on AlGaAs supply layer without any lateral undercut in the cap layer which is difficult to control. Dry etching can achieve the required selectivity but it degrades the two-dimensional electron gas (2DEG) properties due to ion beam induced damage [7-8].

The second critical step in the fabrication stages is the gate formation. In conventional p-HEMT fabrication, most of the gate metal is formed by method of evaporation. This means that the cap layer has to be removed first before the metal is evaporated. Since the AlGaAs layer is easily oxidised upon exposure to air, a great variation in the Schottky characterisation are obtained. These variants are due to the high AlAs mole fraction on the Schottky layer, which makes the formation of interfacial oxide layer on Schottky layer unavoidable.

With progress in advanced growth techniques such as Molecular Beam Epitaxy (MBE), it has become possible to prepare interfaces which are oxide free and Schottky barrier metal grown *in-situ* are possible [9]. In addition, by using MBE, it is possible to grow a planar doped layer (δ -doped) in the AlGaAs Schottky layer. With δ -doped layer, problems such as controlling the device pinch-off and threshold voltage, carrier confinement for short channel effect, high gate leakage current and low breakdown voltage can be minimised or eliminated [10-13]. The δ -doped approach also allows for a reduced aspect ratio due to higher doping levels employed without degrading the breakdown voltage.

Based on this information, we propose a new p-HEMT structure that makes use of the *in-situ*

gate deposition of the epitaxial Al on δ -doped pseudomorphic material grown by MBE. A "jumbo" FET (gate length from $5\mu\text{m}$ to $15\mu\text{m}$) mask with a self-aligned technique has been designed for this device. We report here on the first pseudomorphic AlGaAs/InGaAs/GaAs HEMT (p-HEMT) demonstrator using epitaxial Al as a gate metal. Results from this work should serve as preliminary indications of the potentials for smaller gate devices ($0.5\mu\text{m}$ to $1\mu\text{m}$) and processing methods.

FABRICATION

The p-HEMT heterostructure used in this work consist of $0.5\mu\text{m}$ undoped GaAs buffer layer, followed by 150\AA of undoped $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ channel layer, a 30\AA AlGaAs spacer layer, a delta-doped layer with density of $5 \times 10^{12} \text{ cm}^{-2}$ and undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ with a thickness of 300\AA . Finally, an epitaxial Al (of approximately $0.5\mu\text{m}$ thickness) was evaporated as shown in Figure 1. Details of the growth method and sample assessments are described in detailed elsewhere [9].

Epitaxial Aluminium $0.5\mu\text{m}$		
$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$	300\AA	δ -doped $5 \times 10^{12} \text{ cm}^{-2}$
AlGaAs	30\AA	
$\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$	120\AA	
GaAs	$0.5\mu\text{m}$	
$\frac{\text{AlGaAs}}{\text{GaAs}}$	$\frac{200\text{\AA}}{20\text{\AA}} \times 10$	
GaAs	$0.25\mu\text{m}$	
Semi-insulating GaAs		

Figure 1: The schematic of the epitaxial Al-AlGaAs/InGaAs/GaAs p-HEMT structure.

Hall mobility measurements using Keithley Hall Effect setup indicates a room-temperature 2DEG concentration of $2.53 \times 10^{12} \text{ cm}^{-3}$ with a mobility of $5647 \text{ cm}^2/\text{V.s}$ and 77K 2DEG concentration of $2.34 \times 10^{12} \text{ cm}^{-3}$ with a mobility of $15812 \text{ cm}^2/\text{V.s}$.

Since the epitaxial Al already in place for the gate formation, the fabrication process was reduced to five basic steps:

- 1) Isolation of the transistor by mesa etching.
- 2) Etching of the epitaxial Al for gate formation.
- 3) Formation of the ohmic contact on source and drain.
- 4) Deposition of Si_3N_4 in order to prevent any surface conduction and edge protection from overlay metal.
- 5) Deposition of overlay metal to gate, source and drain for bonding purposes.

The mesa was defined by conventional photolithography. After the removal of the epitaxial Al using very diluted NaOH (~5%) the AlGaAs/InGaAs/GaAs was etched down to the buffer layer using a nonselective etchant $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ to a thickness of $0.6\mu\text{m}$. Gate formation was then made by etching the epitaxial Al layer on top of the mesa using ~5% NaOH.

Etching of the gate recess was not required since the gate was already formed on the AlGaAs Schottky layer, thus problems such as lateral cut, uneven slope and edge uniformity associated with the recess etch were eliminated.

The ohmic contact patterns were defined using a lift-off technique. A AuGe/Ni/Au metal system was used for the source and drain since it is widely used as an ohmic contact to GaAs and AlGaAs materials. After alloying at 450°C for 30s in rapid thermal annealer (RTA), a specific contact resistivity, ρ_c of $3.6\text{-}5.6 \times 10^{-6} \Omega\text{cm}^2$ and a contact resistance, R_c of 0.24-0.28 $\Omega\cdot\text{mm}$ were routinely obtained. These values are higher than that normally obtained by ohmic contact on n^+ -cap layer ($\sim 3\text{-}4 \times 10^{-7} \Omega\text{cm}^2$ for ρ_c and 0.1-0.05 $\Omega\cdot\text{mm}$ for R_c). This is clearly due to the fact that the ohmic contacts in this structure are on a high band-gap AlGaAs layer and the AlGaAs surface gets oxidised prior to the deposition of the ohmic metal. Using a similar structure but with undoped GaAs cap layer (50Å), contact resistance R_c was significantly reduced to 0.1 $\Omega\cdot\text{mm}$ [14]. Thus, future plan for this structure is to incorporate a thin GaAs layer ($\sim 15\text{-}20 \text{ \AA}$ thick) on top of the AlGaAs Schottky layer prior to deposition of epitaxial Al.

Finally, the device was passivated using Si_3N_4 in order to protect the surface from any contamination and possible surface conduction between source-gate and gate-drain contacts.

DEVICE PERFORMANCE

Dc characteristic

All dc characteristics were made using Keithley parameter analyser. Typical forward I-V characteristics of the epitaxial Al diode with circular Schottky diameter of 150 μm are shown in Figure 2. The device have a forward turn-on voltage of 0.9 V and linear over five decades of current. The breakdown voltage of the epitaxial Al diodes, defined as the voltage at which the reverse current is 100 μA , was 15 V and was fairly abrupt. The barrier height, Φ_b and ideality factor, n measured from the forward bias part of the I-V characteristics were as detailed in Table 1. The barrier height, Φ_b was slightly lower and the ideality factor, n was slightly higher than what obtained from previous work ($\Phi_b=0.9, n=1.03$) [9] due to higher series resistance from the source/drain contact. However, these values remained fairly constant even when treated to temperatures up to 500°C in a rapid thermal annealer for 2 minutes. The reverse breakdown voltage, V_b was at 15V before the heat treatment and reduced to 12V after heat treatment as shown in Figure 3. The series resistance also increased from 18 Ω to 25 Ω . This was possibly due the degradation of the ohmic contacts.

	300K	77K
Mobility, μ (cm ² /V.s)	5647	15812
Sheet Density, n (cm ⁻²)	2.53×10^{12}	2.34×10^{12}
Ideality factor, n	1.2	-
Barrier Heights, Φ_B (eV)	0.79	-

Table 1: Hall data, barrier heights and ideality factor measured from epi-Al p-HEMT structure.

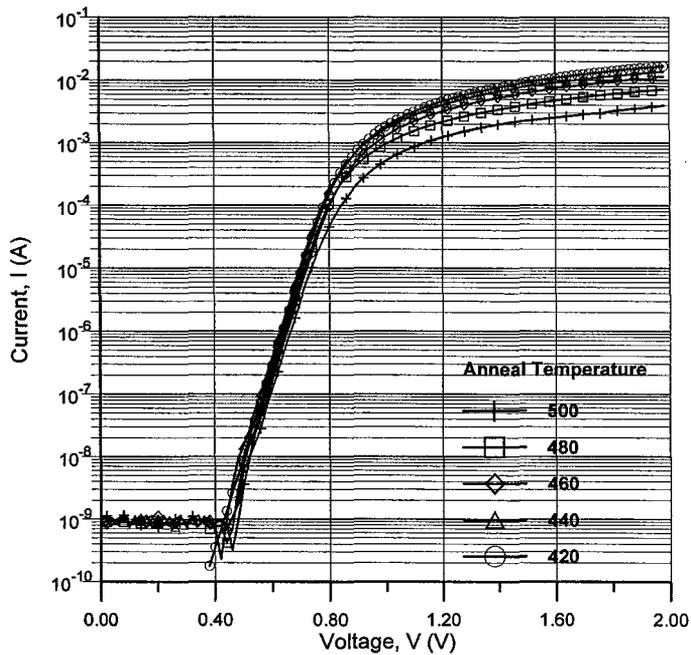


Figure 2: Forward I-V characteristics of the epi-Al diodes annealed at various temperature. Note that the series resistance started to increase as anneal temperature increased.

For a $5 \times 100 \mu\text{m}^2$, the device pinch-off was very well defined at -2.1V as shown in Figure 4 (a). A maximum transconductance of 89.7 mS/mm was obtained at $V_g = 0.2\text{V}$ as shown in Figure 4 (b) which is slightly lower than conventional p-HEMT, due to higher contact resistance. However, both I-V transfer characteristics and figure of merits on transconductance shows better device performance than conventional p-HEMT even at elevated temperature of 500°C , in agreement with data from forward-reversed bias in figure 2. Also at $T=500^\circ\text{C}$, the transconductance as function of gate voltage shows a broad plateau around its peak in contrast to conventional p-HEMTs which show a sharp peak in the transconductance due to the onset of parallel conduction in the doped high-bandgap materials at high gate biases.

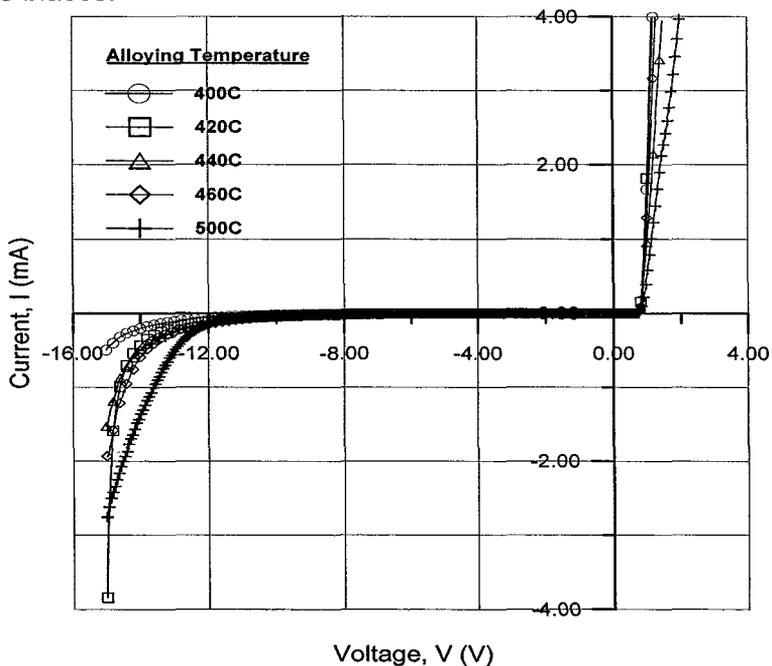


Figure 3: I-V characteristic of the epi-Al diodes at various anneal temperature.

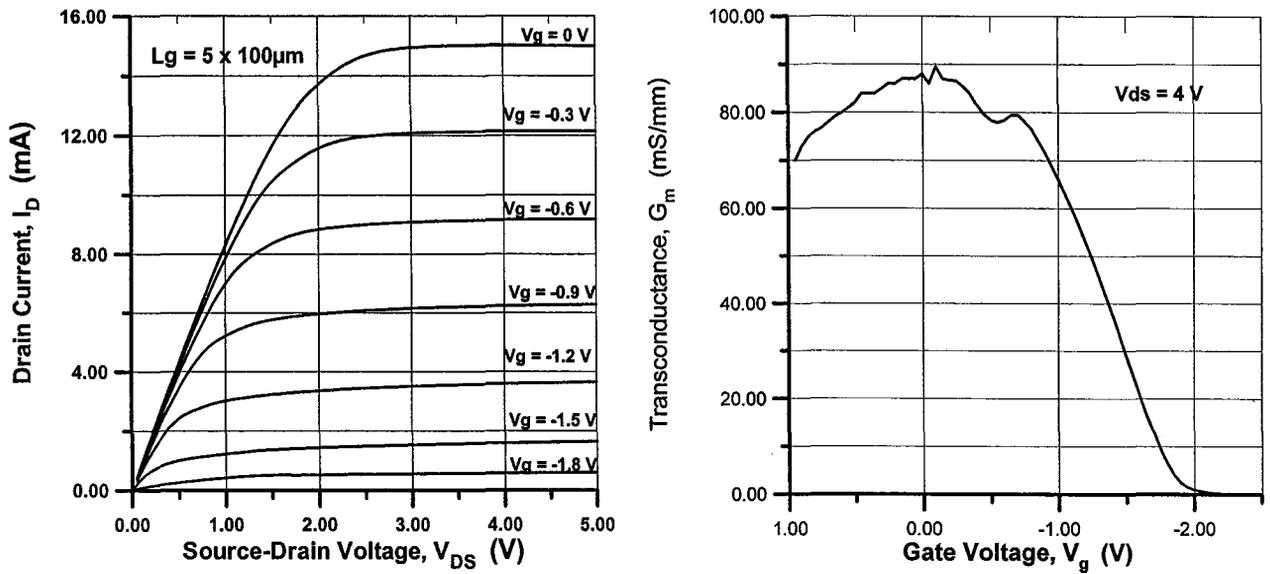


Figure 4: (a) The I-V transfer characteristics and (b) Transconductance of the measured data from epi-Al p-HEMT at elevated $T=500^\circ\text{C}$

SUMMARY AND CONCLUSION

The fabrication and characterisation of an AlGaAs/InGaAs/GaAs pseudomorphic HEMT (p-HEMT) with *in-situ* deposited epitaxial aluminium gate by MBE has been reported. A new processing technique was developed where recess etch and gate metal deposition were no longer required. Thus, problems related to recess etch and etchant selectivity were eliminated. The processing steps were also reduced from normally six major steps to five. The electrical characteristics and the thermal stability of the epitaxial Al p-HEMT were investigated. The results from transistor I-V characteristic were compared with those obtained from a commercial software simulation package (HELENA). The transconductance from HELENA is slightly higher than one obtained from this work. This is due to the higher series resistance on the epitaxial Al transistor. However, thermal treatment of the transistor showed the superiority of the epitaxial Al gate. It is very important to point out that in this newly proposed p-HEMT structure, the ohmic contacts are defined and formed after the gate definition. Because of the high temperature anneal required to fabricate the ohmic contact, the gate metal must be able to withstand such temperatures. The epitaxial Al Schottky contact is thermally stable up to $\sim 500^\circ\text{C}$, therefore permitting the fabrication of this new p-HEMT structure. The same is not true of conventional Ti/Pt/Au or Ti/Au gate metals.

These results also show the potential of the epitaxial Al p-HEMT as a power device due to the epitaxial Al diode stability over a large temperature range and a high transconductance on the transistor I-V characteristics. For low-noise application, the parasitic contact resistance of the ohmic contact have to be lowered in order to obtain a lower ideality factor.

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