In the name of Allah
The compassionate
The merciful

Free Level Threshold Zone
(FLTZ) Logic
For mixed Analog – Digital closed loop circuitry

By

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DEDICATIONS

I wish to dedicate all efforts and outcomes of this thesis to those who dedicated their life for their moral belief in dear ***Islam*** and those who would sacrifice everything for the pride and harmony of my dear country ***Iran***

I dedicate this thesis to my Parents and my wife, Dr. Homeira, whose help have always given invaluable support in my life.

I dedicate all my experiences approached by this project to my children, Sara and Golnaz. It may open a new vision in science as a guide for their future progress.

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LIST OF SYMBOLS

A_0	Gain of Operational Amplifier
ADSL	Asymmetric Digital Subscriber Line
β	Substitution for capacitor error equal to $C_f(C_s + C_f)$
C	Capacitor
CCPR1L	Capture Compare PWM Register 1 Low byte
CCP1CON	Capture Compare PWM 1 Control register
ΔC	Mismatch error source in MOS capacitors
C_f	Frequency compensation Capacitor
C_s	Input signal Capacitor
D	Duty cycle
E	Electro Force or Battery
e	Natural Logarithm
EMI	Electro Magnetic Interference
$E(X)$	Mean of random variable X
F(x)	Frequency of detailed index by (x)
$F(X)$	Function of X
$I_{(x)}$	Current of detailed index by (x)
L	Inductor
P	Probability
P_D	Dissipated Power

$P_{D(FLTZ)}$	Dissipated Power of FLTZ
PR2	PIC MCU Register to specify the frequency in PWM mode
R	Resistor
r	Dynamic saturated resistor of MOSFET transistor
$R_{(x)}$	Resistor of detailed index by (x)
$T_{(x)}$	Frequency Period of detailed index by (x)
$\mu_B(x)$	Fuzzy set distribution membership
$Var(X)$	Variance of variable X
$V_{(x)}$	Voltage of detailed index by (x)
x	Variable
X_C	Capacitor resistance proportional to the frequency
X_L	Inductor resistance proportional to the frequency

LIST OF ABBREVIATION

A	Analog
AC	Alternative Current
AD	Analog to Digital
ADA	Analog to Digital to Analog
ADC	Analog to Digital Converter
ADSL	Asymmetric Digital Subscriber Line
AR*X*	Analog Reference (*X* = port bit number)
ASM	Assembly
BJT	Bipolar Junction Transistor
CCD	Charge Couple Device
D	Digital
DA	Digital to Analog
DAC	Digital to Analog Converter
DC	Direct Current
DNL	Deferential Non Linearity
DR	Dynamic Range
EMF	Electromagnetic Field
EMI	Electromagnetic Interference
ENOB	Effective Number Of Bits
FFT	Fast Fourier Transform
FLTZ	Free Level Threshold Zone

FM	Frequency Modulation
GIO	General Input Output
GPIO	General Programmable Input Output
HID	High Intensive Discharge
INL	Integral Non Linearity
I/O	Input Output
LED	Light Emitting Diode
LMS	Least Mean Square
LSB	Least Significant Bit
MCU	Microcontroller unit
MHz	Mega Hertz
MOSFET	Metal Oxide Surface Field Effect Transistor
MSB	Most Significant Bit
MSPS	Mega Sample Per Second
OP – AMP	Operational Amplifier
PIC	Programmable Integrated Circuit
PLL	Phase Locked Loop
PN	Positive Negative
PWM	Pulse Width Modulation
RMS	Root Mean Square
SAR	Successive Approximation Register
SMPS	Switch Mode Power Supply
SNDR	Signal to Noise + Distortion Ratio

SNR	Signal to Noise Ratio
TTL	Transistor Transistor Logic
TV	Television
UJT	Uni Junction Transistor
VCO	Voltage Controlled Oscillator
ZIF	zero insertion force

LIST OF PUBLICATIONS & SEMINARS

Alireza Nazem, (2006), An introduction to oscillation analysis of Free Level Threshold Zone on a non-Schmitt input pin of a sequential logic device in a closed loop circuit and comparison in fuzzy Logic. *International Journal of Engineering Science & Technology. Volume 5, Number 1, December 2006, 125-131*

Alireza Nazem & Mohd Rizal Arshad, (2007), Introduction of FLTZ logic for Analog circuits controlled by Microcontrollers. *International Conference on Robotics, Vision, Information, and Signal Processing Penang, Malaysia 28 – 30 November 2007*

Alireza Nazem, (2007), Free Level Threshold Zone (FLTZ) Logic for mixed Analog – Digital closed loop circuitry. *School of Electrical and Electronic Engineering. Universiti Sains Malaysia.*, Pulau Pinang, Malaysia, 31st June 2007

Logik Zon Ambang Bebas Takat (FLTZ) untuk Litar Gabungan Suapbalik Analog - Digital

ABSTRAK

Para penyelidik sentiasa mencari cara-cara penambahbaikan kaedah antara muka antara domain Analog dan Digital. Tidak dapat dinafikan bahawa terdapat perkembangan di dalam pembangunan teknik-teknik penukaran AD/DA untuk pelbagai aplikasi. Namun begitu, masih terdapat ruang pembaikan di dalam bidang ini. Modul-modul AD dan DA sekarang memerlukan ruang permukaan yang besar, menggunakan banyak tenaga, mengakibatkan kelengahan transmisi dan ada kalanya mengakibatkan kehilangan data. Terdapat banyak masalah di dalam hampir semua teknik konvensional, sedangkan teknik-teknik yang lebih inovatif untuk AD/DA belum lagi dibangunkan. Projek ini difokuskan kepada kaedah unik yang tidak mengambilkira keperluan penukaran AD/DA dalam pemprosesan logik berturutan, atau MCU dengan penggunaan port pemulaan *Input bukan-Schmitt* yang dipasang secara terus di dalam litar gegelung tertutup dan mengawal peranti analog. Asas untuk logik FLTZ bergantung kepada hayunan tidak stabil daripada output digital iaitu input yang mengesan nilai-nilai (1) dan (0) di tahap voltan ambang. Satu lagi konsep FLTZ yang boleh diambilkira ialah apabila PWM dalaman digunakan pada mod latarbelakang dan dikawal oleh FLTZ hasil daripada pengesanan input. FLTZ asalnya diuji dan dibangunkan menggunakan pengawal mikro jenis PIC. Hasilnya membawa kepada pengenalan FLTZ di dalam peranti *Switch Mode Power Supply* (SMPS) dengan penggunaan MCU dalam litar gegelung tertutup. FLTZ boleh mengurangkan blok, penggunaan tenaga, kehilangan data, kehilangan kuasa, kos, saiz cip dan kelengahan transmisi di dalam MCU bukan hanya dengan mengambilkira penukaran AD/DA konvensional, tetapi juga sebagai voltan rujukan purata. Oleh kerana FLTZ mempengaruhi kod program, di samping ia bergantung kelajuan peranti (frekuensi jam), ia dapat menghasilkan banyak penyelesaian untuk pelbagai aplikasi seperti VCO untuk pengawal sistem komunikasi dan pengawal kelajuan automatik untuk kereta.

Free Level Threshold Zone (FLTZ) Logic For mixed Analog – Digital closed loop circuitry

ABSTRACT

Researchers have always look for ways to improve the interfacing method between the Analog and Digital domain. Undeniably, the last few decades have witnessed the development AD/DA conversion techniques for various applications. Nevertheless, there still exist rooms for further progress and development of this important area. Current AD and DA modules occupy space (surface), consume power, cause transmission delay and sometimes introduce data loss as well. The conventional techniques for AD/DA conversions have yet to be improved specially due to transmission delay and data loss by the cause of sampling. In this project, the focus is on a unique method that ignores the need of conventional AD/DA converters in a sequential logic processor or MCU by making use of non-Schmitt Input initialized port(s) which is(are) directly attached in a closed-loop circuit to read from and control analog device(s). The basic of Free Level Threshold Zone (FLTZ) Logic relies on the unstable generated oscillation of a digital output where the program-referred non-Schmitt input, is detecting (0) and (1) values at the stage of threshold voltage. Another concept of FLTZ may be considered when an internal Pulse Width Modulation (PWM) is initialized on the background mode and controlled by FLTZ due to the input detections. FLTZ initially tested and developed using PIC™ microcontrollers. The outcome successes lead to an introduction of FLTZ in Switch Mode Power Supply (SMPS) device by direct use of an MCU in a closed-loop circuitry. FLTZ technique addresses the way of minimizing the blocks in an Analog-Digital architecture over 20%, as well as power consumption (>10%), data loss, power loss (>10%), cost, chip size over 10% and transmission delay in MCU architecture not only by ignoring conventional AD/DA converters, but also providing a reference voltage. As the effect of FLTZ is related to the driving program codes, thus dependent to the speed of the device (clock frequency), FLTZ creates effective solutions for various kinds of applications such as VCO for communication system, and automotive speed cruise.

Chapter 1

Introduction

1.1 Overview

The Free Level Threshold Zone (FLTZ) is an approach to minimize a mix analog and digital design by splitting away A to D and D to A blocks in a closed-loop circuitry. While an analog variation in time can be analyzed and controlled continuously by complicated mathematical calculations, a digital processing addresses to the logic numerical analysis, algebra and probability environment. An analog value in Logic mode is more accessible to be analyzed. It can be processed back to an analog value again after digital to analog conversion. An example of a filtering concept is imaged in figure 1.1:

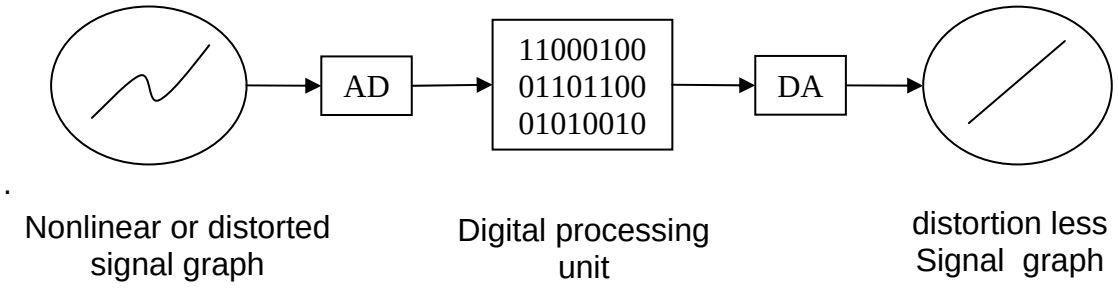


Figure 1.1 Block diagram of basic Digital filtering system

In this thesis, an efficient practical approach is presented for a closed loop MCU controlled concept where AD and DA blocks can reliably be eliminated. The efficiency increases by the resolution, detecting the value on the non-Schmitt input pin, where the Clock frequency is specifying the resolution respectively. Further more, a practical HID ballast solution is presented in the

thesis. FLTZ has also provided a wide range of control and diagnosis accessibility in a developed Switch Mode Power Supply (SMPS) circuit while a simple reliable circuitry is concerned.

1.2 Research objectives

The main objective for this thesis is to represent an innovative control technique for splitting away the Analog-Digital conversion blocks based on closed loop design, resulting simplification of circuitry, faster data processing and cheaper system development beside less power consumption and loss. While the sub-objectives are:

1- To introduce FLTZ as reference voltage for voltage regulators

2- To draw a comparison between FLTZ and Fuzzy logics to bear an improved practical integrated technique in the field of electronic control systems.

3- To design and develop a reliable and accurate Switch Mode Power Supply (SMPS) for constant power control for HID lamps by using the FLTZ logic (figure 1.2).

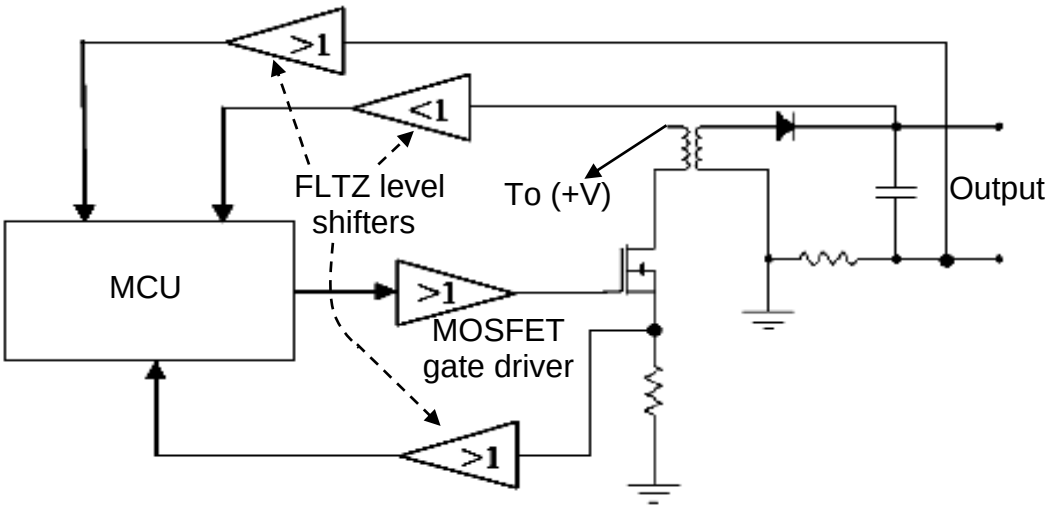


Figure 1.2 The practical SMPS block diagram for FLTZ

4- To introduce FLTZ as a solution for the VCO applications that can be in gear with PLL, FM tuning system.

1.3 Thesis overview

This thesis is organized in six chapters as follows:

A brief introduction is given in Chapter 1, whilst Chapter 2 presents the literature describing the theory behind Analog / Digital conversion methods and existing conventional techniques which are currently in use. Chapter 3 represents a brief introduction of the novel technique of FLTZ in closed loop circuitry, ending with a comparison of the FLTZ and Fuzzy logics as multi-valued logics.

In Chapter 4, experimental setup and implementation of two practical applications has been drawn. HID ballast as a successful product which is designed and developed using FLTZ technique for High Intensive Discharge lamps (HID lamps) in 2006 has been given in detail and a Voltage Controlled Oscillation circuit (VCO) is also discussed. Chapter 5 is offering the results and discussion of the thesis and finally Chapter 6 concludes the work of this research. This chapter also outlines the benefits of FLTZ and some suggestion for future research.

Chapter 2

Literature review

2.1 Introduction

Analog to digital converters are the fundamental building blocks in highly integrated mixed-signal integrated circuits. Introducing digital methods and circuitry in practical systems is primarily a question of the associated costs. Special consideration must be given to the additional cost of the AD converters [1]. An Analog to Digital Converter (ADC) is an electronic circuit that measures an analog signal such as a voltage that is proportional to a continuous physical quantity, such as temperature, pressure, or speed and converts it to a digital representation of the signal. It compares the analog input signal to a known reference signal and then produces a digital representation of the analog input. The output of an ADC is a digital binary code, which can represent only a bounded number of values. Thus an ADC inherently introduces a quantization error, which is information that is lost. The more digital codes that the ADC can resolve the more resolution it has and the less information lost due to the quantization error. Current digital applications create a need for high resolution and high speed analog to digital converters. Modern analog to digital converters are divided into two different categories, Nyquist rate ADCs [2] [3], and over sampled ADCs. Nyquist-rate ADCs produce a series of output codes in which each code corresponds directly with one sample of the analog input signal. To avoid aliasing of frequency spectra, the input signal bandwidth must be limited to half the sampling frequency as implied by the Nyquist criterion [4]. Over-sampled ADCs sample an analog input at a much higher rate than the Nyquist rate of the input signal and, obtain the desired output code by filtering out

quantization noise that is outside of the signal bandwidth. Flash, successive approximation, and pipeline ADCs are two types of Nyquist-rate ADCs [5]. Sigma-delta method is in over sampled ADC category. Each ADC structure has its own advantage and disadvantage as discussed in the following sections.

2.2 Flash Analog-to-Digital Converter

Flash analog to digital converters, also known as parallel ADCs, are made by cascading high speed comparators as shown on Figure 2.1.

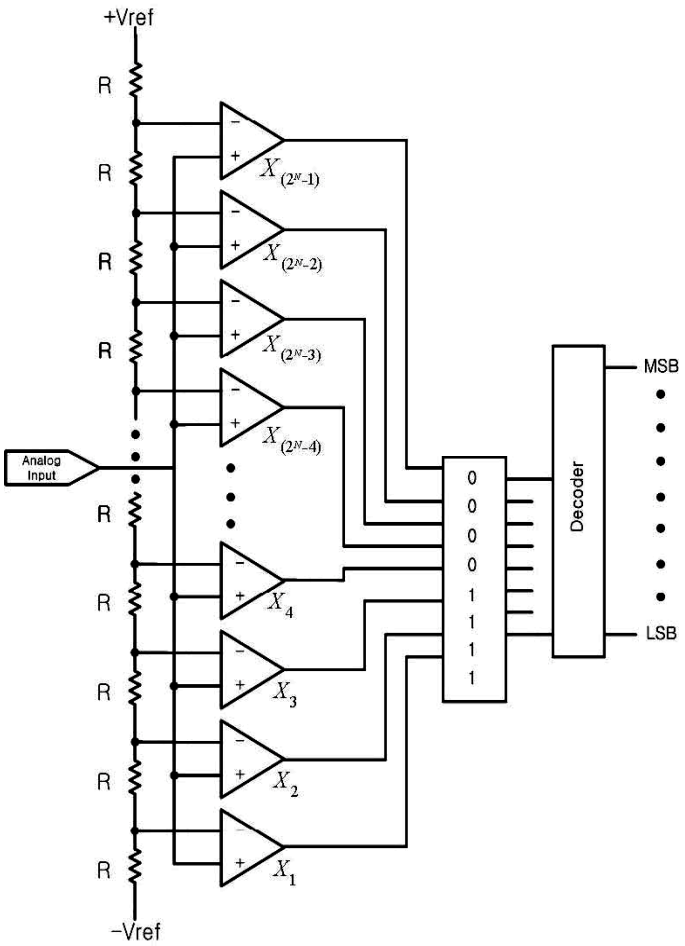


Figure 2.1 Typical Flash analog to digital converter[6]

Flash ADCs are ideal for applications requiring very large bandwidth; however, they typically consume more power than other ADC architectures and are generally limited to 8-10 bits resolution [7]. As shown in Figure 2.1, a typical N-bit flash ADC employs $2^N - 1$ comparators, with 2^N matched resistors to provide a reference voltage for each comparator [6]. Each comparator represents 1 LSB and produces a (1) when its analog input voltage is higher than the reference voltage which is applied to it; otherwise, the comparator output is (0). If the analog input is between V_{X4} and $V_{X5,}$ comparators X1 through X4 produce (1)s and the remaining comparators produce (0)s, the point where the code changes from ones to zeros is the point where the input signal becomes smaller than the respective comparator reference voltage levels. This output pattern is frequently called ‘a thermometer code’ since the height of the (1)s rises and falls with the input voltages.

These comparators are typically a cascade of wideband low gain stages, they are low gain comparators. The input offset of each comparator is smaller than a LSB of the ADC, otherwise, the comparator’s offset could falsely passes through the comparator, resulting in ‘bubbles’ in the thermometer code [8]. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a (1) or a (0). The result is subsequently converted to a binary output by an encoder. The principal advantage of the flash architecture is high throughput rate. The conversion of each sample takes only one single clock period. Many issues limit the utility of this approach for resolution above 8 bits, the exponential growth of the input capacitance, the power dissipation and the area are useless. Furthermore the offset of the comparators, the feed through of the analog input to the resistor

ladder, the slew-dependent comparator delay and bubbles in the thermometer code degrade the static and dynamic performance substantially [8] [9].

2.3 Successive-Approximation-Register ADC

Successive approximation register (SAR) ADCs are suitable for medium to high resolution applications [10]. SAR ADCs provide up to 5 mega sample per second with resolutions from 8 to 16 bits. This combination makes them ideal for a wide variety of applications, such as portable instruments, pen digitizers, and industrial controls [11]. This conversion process basically consists of starting with the most significant bit (MSB) and successively trying a (1) in each bit of a DA decoder. If the DA output is larger, the (1) is removed from that bit as the process continues and a (1) is tried in the next most significant bit [12]. The SAR ADC basically implements a binary search algorithm; the basic architecture is quite simple as shown in Figure 2.2. The analog input voltage V_{in} is held on a sample/hold, to implement the searching algorithm, the N-bit register is first set to mid scale, this forces the DAC output V_{DAC} to be V_{ref} /2, where V_{ref} is the reference voltage provided to the ADC. A comparison is then performed to determine V_{in}, if is less than or greater than V_{DAC} . If V_{in} is greater than V_{DAC} , the comparator output is a logic 'high' or (1) and the MSB of the N-bit register remains at (1). Conversely, if V_{in} is less than V_{DAC} , the comparator output is a logic (low) and the MSB of the register is cleared to logic (0).

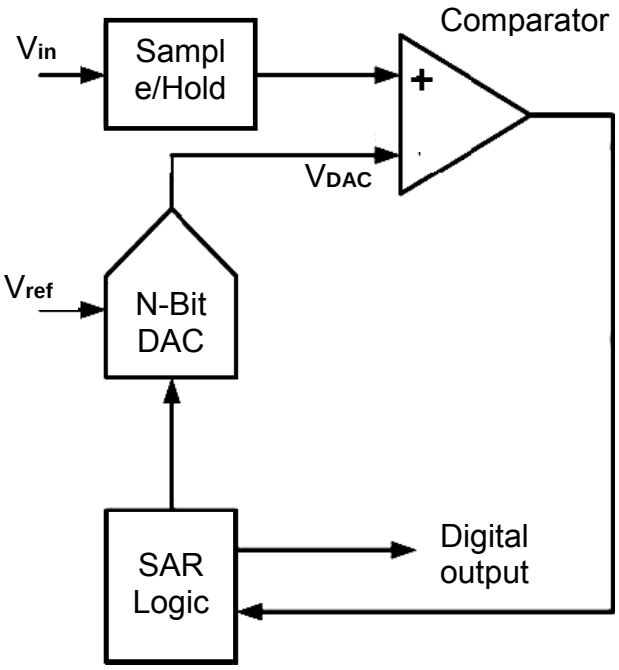


Figure 2.2 Successive approximation register (SAR) ADC

The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete, and the N−bit digital word is available in the register.

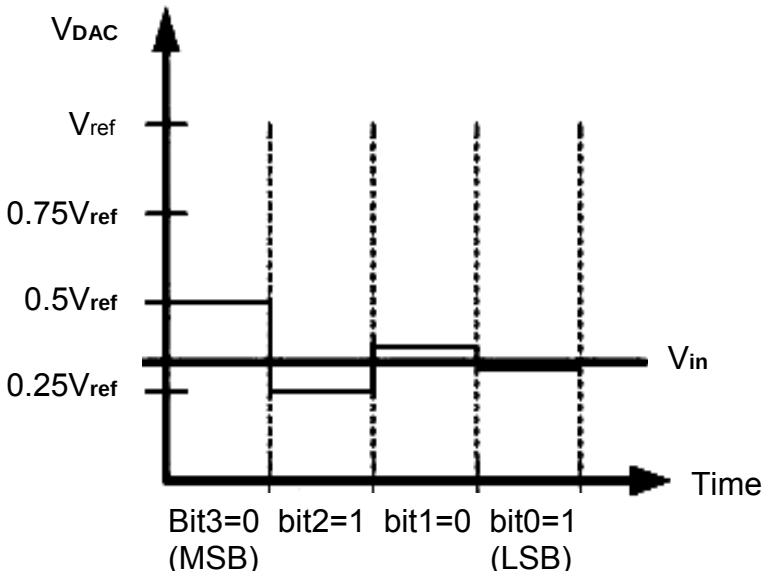


Figure 2.3 An example of a 4-bit conversion.

Figure 2.3 shows an example of a 4-bit conversion. The y-axis represents the DAC output voltage. In the example, the first comparison shows that $V_{in} < V_{DAC}$. Thus, bit 3 is set to (0). The DAC is then set to 0100 and the second comparison is performed. Since $V_{in} > V_{DAC}$, bit 2 remains at (1). The DAC is then set to 0110, and the third comparison is performed.

Bit 1 is set to (0), and the DAC is then set to 0101 for the final comparison. Finally, bit 0 remains at (1) because $V_{in} > V_{DAC}$. Notice that four comparison periods are required for a 4-bit ADC. Generally speaking, an N−bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is completed. One other feature of SAR ADCs is that power dissipation scales with the sample rate, unlike flash or pipeline ADCs, which usually have constant power dissipation versus sample rate [10]. This makes the SAR ADC's especially useful in low-power applications or applications where the data acquisition is not continuous [13].

2.4 Sigma-Delta Analog to Digital Converter

Sigma-Delta ADCs are popular for high-resolution audio rate applications such as mobile telephones, digital audio, and ADSL Communication. 20-bit ADCs and known without the need for any trimming [14]. A sigma-delta ADC combines a modulator with a high rate decimating filter. It can be high resolution by using a high over sampling ratio, but recently some high bandwidth sigma-delta type converters have reached a bandwidth of 1MHz to 2MHz with 12 to 16 bits of resolution. These are usually very high order sigma-delta modulators incorporating a multi-bit ADC and multi-bit feedback DAC, and the main applications of these sigma-delta converters are in ADSL [15] [16].

The structure of the basic sigma-delta converter is shown in Figure 2.4.

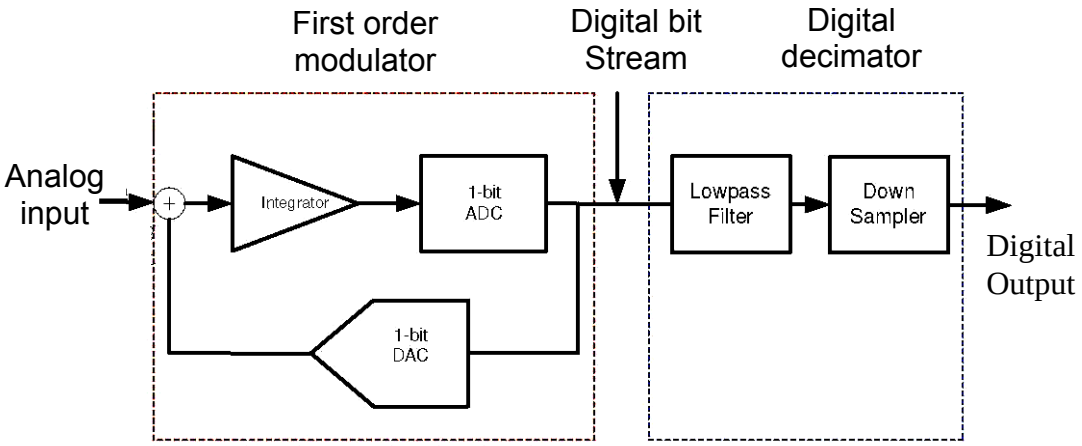


Figure 2.4: The Sigma-Delta Over Sampling ADC Architecture[15]

The modulator consists of an integrator and a comparator, with a 1-bit DAC in a feedback loop, the internal DAC is simply a switch that connects the comparator input to a positive or negative reference voltage the modulator produces an output that consists of a stream of digital (1)s and (0)s, where the percentage of (1)s varies in direct proportion to the analog input. The digital decimator that follows performs both digital filtering and down sampling of the 1-bit input data stream. The sigma-delta ADC also includes a clock unit that provides proper timing for the modulator and digital decimator [17]. A significant problem with the sigma-delta converter, resulting directly from its nonlinear nature and feedback, is the presence of *tone* components in the output in response to DC inputs, or even small amplitude sinusoidal inputs. Clearly, these tones are highly undesirable in audio and speech applications, for this reason, higher than second order modulators are used to lower down some of the idle tone problems. In general, for an N order modulator every doubling of the over sampling ratio provides an additional 6N +3dB of SNR. Higher order

modulation can also be achieved by cascading several lower order stages. This avoids problems with stability, while maintaining the advantages with respect to SNR and limit cycles. Fourth order modulators of two cascaded second-order stages are common. There are also architectures which employ multi-bit quantizers. For example, in a second order modulator, each additional bit in the quantizer will result in a SNR improvement of about 6dB.

2.5 Pipeline Analog-to-Digital Converter

The pipeline analog to digital converter has become the most popular ADC architecture for sampling rates from a few MSPS up to 100 MSPS, with resolutions from 8 bits to 16 bits. These kinds of resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic biomedical imaging, digital receiver, digital video for high density TV, ADSL, cable modem, and fast Ethernet. Lower-sampling-rate applications are still the domain of the SAR and sigma-delta ADCs. The highest sampling rates are still obtained using flash ADCs. However, various forms of the pipeline ADCs have so far developed greatly in speed, resolution, dynamic performance [18] [19] [20].

Figure 2.5 shows a block diagram of a 12-bit pipeline ADC. The analog input V_{in} is first sampled and held by a sample and hold circuit, while the flash ADC in stage one quantizes it to 3 bits. The 3 bit output is then fed to a 3 bit DAC, and the analog output is subtracted from the input. This residue is then multiplied up by a gain factor and fed to the next stage. This gained-up residue continues through the pipeline, providing 3 bits per stage until it reaches the 4 bit flash

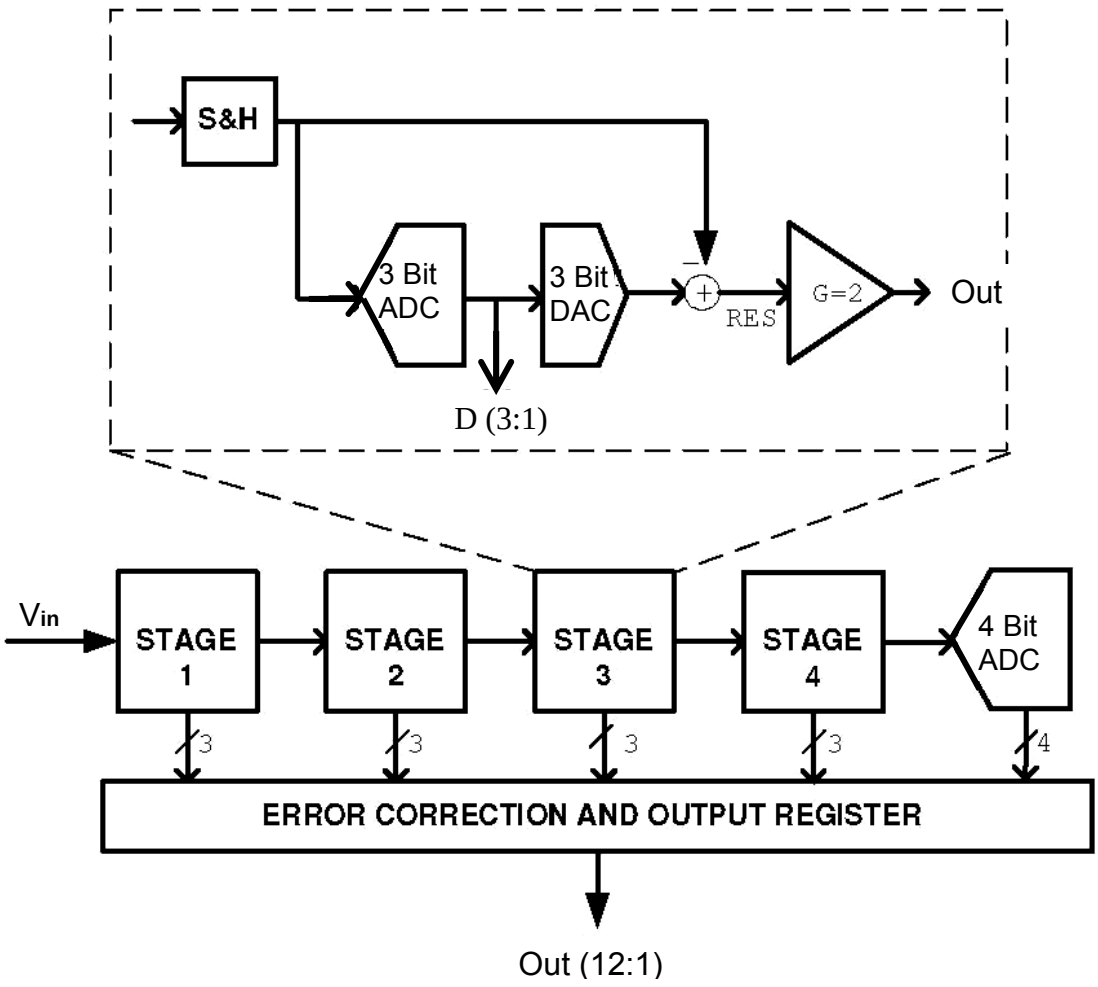


Figure 2.5 Pipeline ADC Architecture[19]

ADC which resolves the last 4 LSBs. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note that as soon as a certain stage finishes processing a sample, determining the bits and passing the residue to the next stage, it can start processing the next sample due to the sample-and-hold embedded within each stage. This pipelining action accounts for the high throughput [21].

In a SAR ADC, the bits are decided by a single high speed, high accuracy comparator bit by bit, from the MSB down to the LSB, by comparing

the analog input with a DAC, whose output is updated by previously decided bits and successively approximates the analog input. This serial nature of SAR limits its operating speed to no more than a few MSPS, and still slower for very high resolutions. A pipeline ADC, however, employs a parallel structure in which each stage works on one to a few bits concurrently. Although there is only one comparator in a SAR, this comparator has to be fast and as accurate as the ADC itself. In contrast, none of the comparators inside a pipeline ADC needs this kind of accuracy. However, a pipeline ADC generally takes up significantly more device area than a SAR of equivalent resolution. Fast flash ADCs exist with sampling rates as high as 1.5 GSPS, but it is much harder to find a 12-bit flash. This is simply because in a flash ADC, the number of comparators is 256 for an 8 bit converter and the number goes up by a factor of 2 for every extra bit of resolution. At the same time each comparator has to be twice as accurate. In a pipeline ADC, however, to a first order the complexity only increases linearly with the resolution, not exponentially. At sampling rates obtainable by both a pipeline and a flash, a pipeline ADC tends to have lower power consumption than a flash [22]. So the pipeline ADC is the architecture of choice for sampling rates from a few MSPS up to 100 MSPS. Figure 2.6 illustrates the bandwidth and sampling rate of the ADCs. An ADC with a 12-bit-resolution does not necessarily have 12 bit accuracy, because the converter sometimes exhibits lower performance than expected due to non linear parameters. ADC characteristics are helpful to select the appropriate ADC architecture.

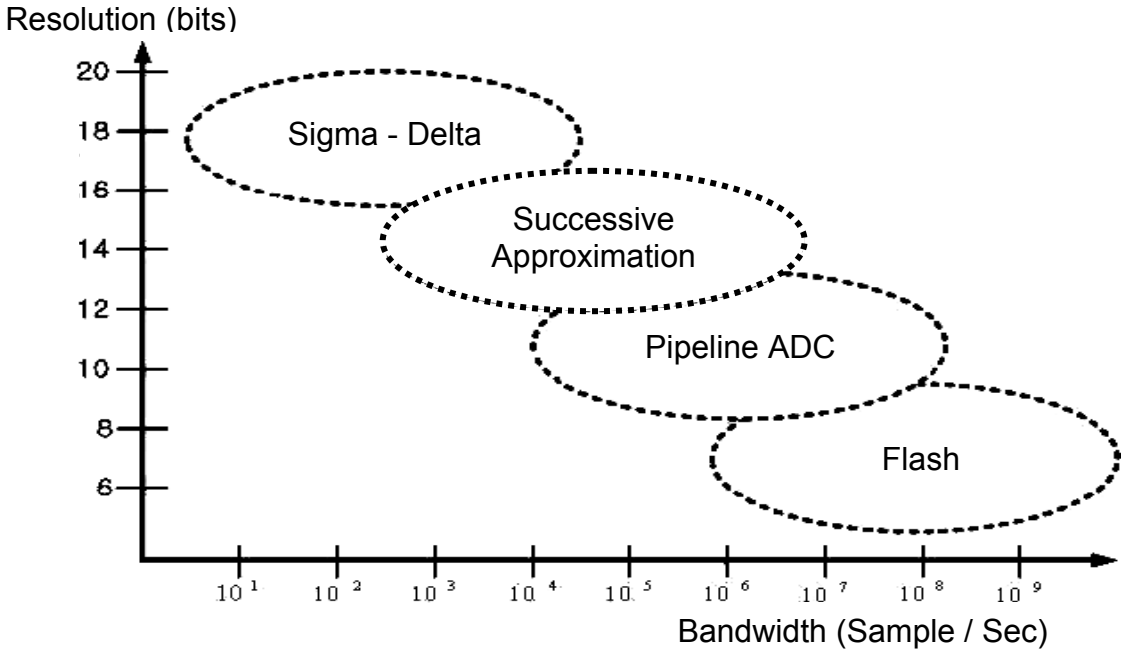


Figure 2.6 Basic ADC Comparison with Resolution and Bandwidth

Each component in a system will have associated errors, so the goal of the converter specification is to keep the total error below a certain value. Often the ADC is the key component in the signal path, so care is required to select a suitable device. The accuracy of the ADC is dependent on several key specifications, which include deferential non linearity errors (DNL), integral non linearity errors (INL), offset and gain errors, and the accuracy of the voltage reference, temperature effects. If 0.1% or 10 bits of accuracy ($1/2^{10}$) is needed, then it makes sense to choose a converter with greater resolution than this. If a 12 bit converter is selected, it may be assumed to be adequate, but without reviewing the specifications, there is no guarantee of 12 bit performance. For example, a 12 bit ADC with 4 LSBs of integral non linearity error gives only 10 bits of accuracy at best (assuming the offset and gain errors have been calibrated). ADC performance can be defined in two different ways, static

performance and dynamic performance. Dynamic performance is especially important for telecommunication systems [23] [24].

2.5.1 Differential Non Linearity (DNL)

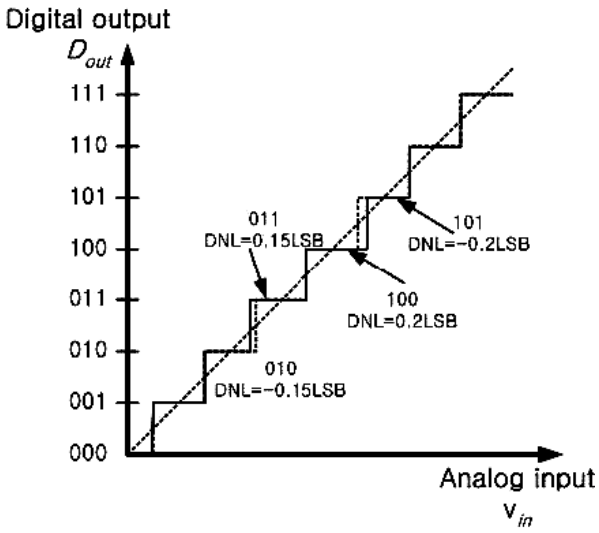
The Differential Non Linearity (DNL) error is defined as the difference between an actual step width and the ideal value of 1 Least Significant Bit (LSB). For an ideal ADC, the differential non linearity coincides with 0 LSB, and the transition values are spaced exactly 1 LSB apart. A DNL error specification of less than or equal to 1 LSB guarantees a monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases or remains constant, thereby avoiding sign changes in the slope of the transfer curve. DNL error is defined as follows,

$$DNL = \left[\frac{(V_{D+1} - V_D)}{V_{LSB}} - 1 \right], \quad \text{where} \quad 0 < D < 2^N - 1 \tag{2.1}$$

Where V_D is the value of the digital output, V_{LSB} is value of the least significant bit and D represents the digit.

With a DNL error less than 1 LSB, the device is guaranteed to have no missing code as shown in Figure 2.7(a), and with a DNL value -1, the device has missing codes as shown in the Figure 2.7(b).

(a)



(b)

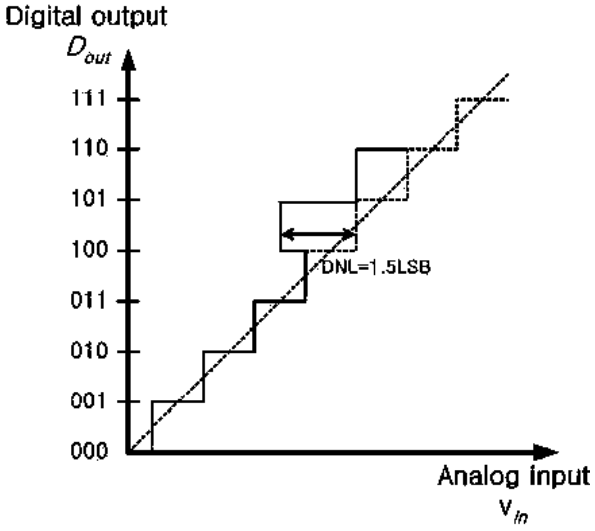


Figure 2.7 Symbol (a) DNL error: no missing codes (b) missing codes

2.5.2 Integral Non Linearity (INL)

INL is defined as the integral of the DNL errors, so good INL guarantees good DNL. INL error is described as the deviation, in LSB or percent of full-scale range, of an actual transfer function from a straight line. An INL error of ±2 LSB in a 12 bit ADC means the maximum non linearity error may be off by

2/4096 or 0.05%. The INL error magnitude then depends directly on the position chosen for this straight line. Two common methods “best straight-line INL” and “end-point INL” are popular to measure the INL errors as shown in Figure 2.8.

Best straight-line INL provides information about the offset and gain error plus the position of the transfer function. It can be determined from the least mean square (LMS) method, and this line is the closest approximation to the ADC’s actual transfer function.

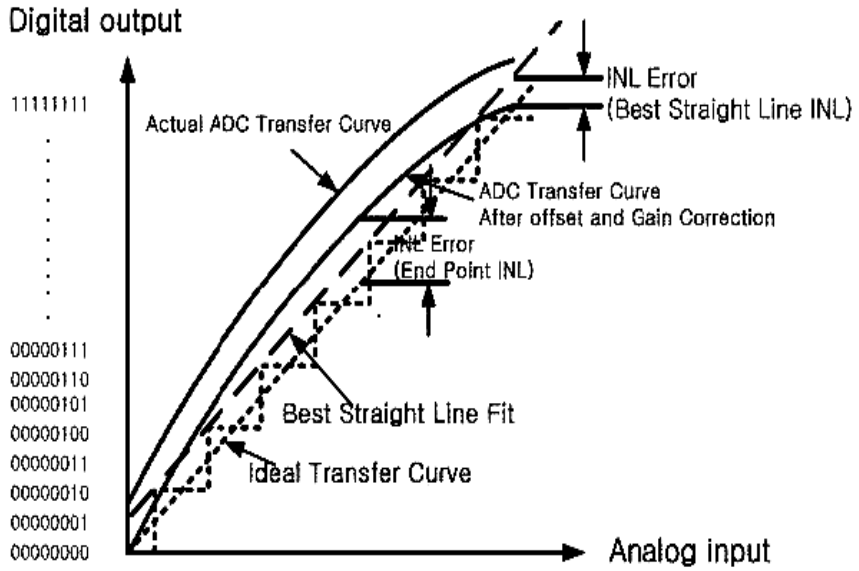


Figure 2.8 Best straight- Line and End-point Fit [25]

The exact position of the line is not clearly defined, but this approach yields the best repeatability [25], and it serves as a true representation of linearity. End-point INL passes the straight line through end points of the converter’s transfer function, thereby defining a precise position for the line. Thus, the straight line for an N-bit ADC is defined by its zero and its full scale outputs or its full scale negative and full scale positive outputs.

The best straight-line approach is generally preferred, because it produces better results. The INL specification is measured after both static offset and gain errors have been nullified, and can be described as follows

$$INL = \left[\frac{(V_D - V_{Zero})}{V_{LSB}} - D \right], \quad \text{where} \quad 0 < D < 2^N - 1 \tag{2.2}$$

$$V_{LSB} = \frac{V_{FullScale} - V_{Zero}}{2^N - 1} \tag{2.3}$$

VD is the analog value represented by the digital output code D, N is the ADC's resolution, V_{Zero} is the minimum analog input corresponding to an all-zero output code, and V_{LSB} is the ideal spacing for two adjacent output codes.

2.5.3 Sources of Errors in Pipeline Analog-to-Digital Converters

There are three major error sources in a pipeline ADC. The first one is the gain error which is introduced by finite opamp gain. This can be removed by adjusting the gain of the opamp. The second error is the offset voltage of the opamp. This error requires some special techniques to remove. The last error is from capacitor mismatch and this can be cancelled by digital calibration techniques [25].

The gain error: mx, is defined as the full-scale error: y, minus the offset error: b, (mx = y – b) . Full-scale error is measured at the last ADC transition on the transfer-function curve and compared against the ideal ADC transfer function. Gain error is easily corrected with a linear function y = (m1/m2) (x), where m1 is the slope of the ideal transfer function and m2 is the slope of the

measured transfer function as shown in Figure 2.9. In order to remove the offset error the x and y axes of the transfer function are shifted so that the negative full-scale point aligns with the zero point of a system. This technique removes the offset error. The gain error is removed by rotating the transfer function about the 'new' zero point. The gain-error specification may or may not include errors contributed by the ADC's voltage reference.

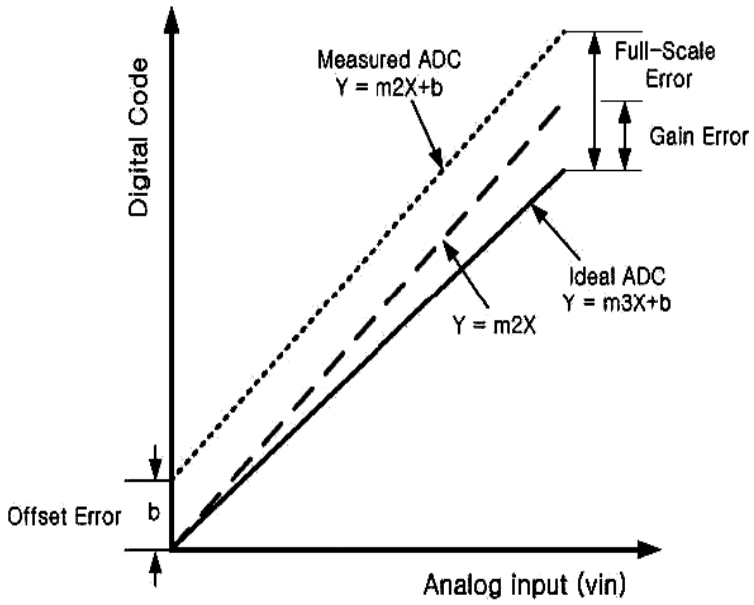


Figure 2.9: Offset, Gain, and Full-Scale Errors [25]

In the electrical specifications, it is important to check for the gain error if is tested, and to determine whether it is performed with an internal or external reference. Typically, the gain error is much worse when an on-chip reference is used [26]. Figure 2.10 shows the effect of finite opamp gain error. Because of finite opamp gain, there is an error voltage at the input of opamp. From Equation (2.6), the error term ($A_0\beta$) makes the slope of the residue plot less

than two or more than two, so the residue voltage may be less than or greater than the full range of the converter.

$$(C_s + C_f) \cdot V_{in} = C_s(0 + \frac{V_{out}}{A_0}) + C_f(V_{out} + \frac{V_{out}}{A_0}) \tag{2.4}$$

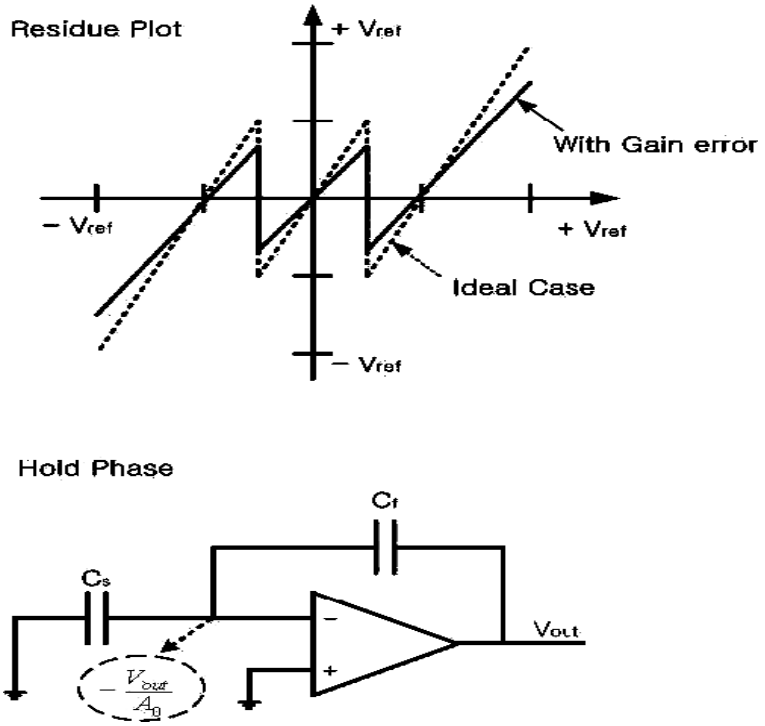


Figure 2.10 Residue Plot of a 1.5 bit Pipeline Stage with Finite Gain Error [26]

$$V_{out} = \frac{C_f + C_s}{C_f + \frac{1}{A_0(C_s + C_f)}} V_{in} = (1 + \frac{C_s}{C_f}) \frac{1}{1 + \frac{1}{A_0 \beta}} V_{in} \tag{2.5}$$

$$= (1 + \frac{C_s}{C_f})(1 - \frac{1}{A_0 \beta}) V_{in} \tag{2.6}$$

As shown in Figure 2.11, the offset of opamp introduces a constant error, or a shift, at the output of pipeline stage.

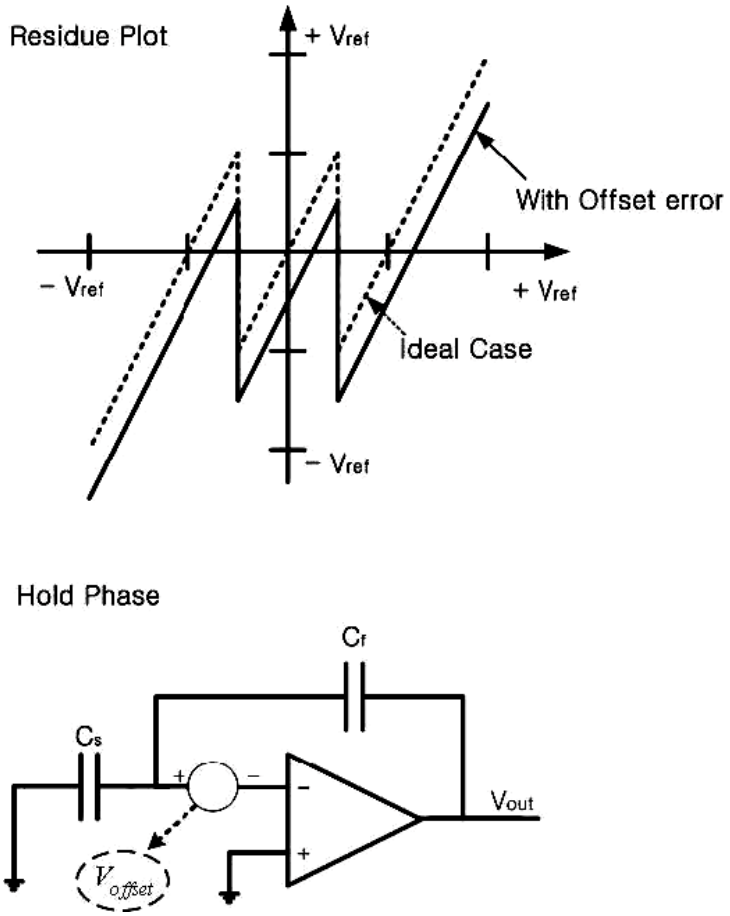


Figure 2.11 Residue Plot of a 1.5 bit Pipeline Stage with Operational Amplifier Offset [26]

From Equation (2.7), this error voltage is represented by Equation (2.8)

$$0 = C_s(0 - V_{offset}) + C_f(V_{error} - V_{offset}) \tag{2.7}$$

$$V_{error} = (1 + \frac{C_s}{C_f})V_{offset} \tag{2.8}$$

To reduce the offset error, the input transistors are often kept quite big, which usually takes a large area. If a 1.5 bit stage is used in the pipeline, this error will be corrected by the later stages. The major cause of gain and offset error is capacitor mismatch, so matched capacitors or precision capacitor ratios have been used extensively for many years. There are several mismatch error sources in MOS capacitors. The major error source consists of long range, gradient related system errors, which are strongly correlated for all capacitors on the same chip. These can be kept to a minimum by using unit capacitor layout techniques with a common centroid geometry [27][19].

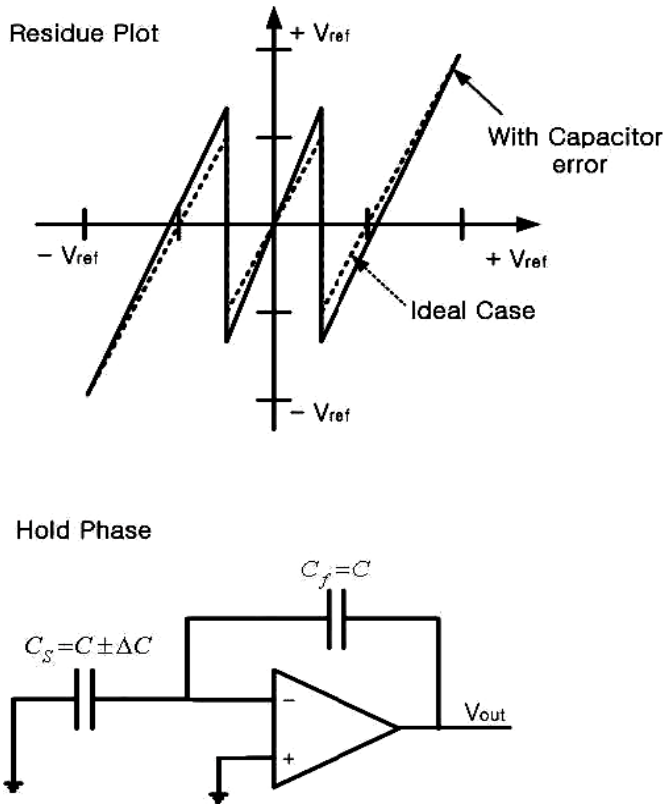


Figure 2.12 Residue Plot of 1.5 bit Pipeline Stage with Capacitor Mismatch [26]

Figure 2.12 shows the effect of capacitor mismatch. Because of process variations, capacitor mismatches always exist. Capacitor mismatch changes the

slope of the residue plot to a value different than two.

$$V_{out} = (1 + \frac{C_s}{C_f})V_{in} = (2 \pm \frac{\Delta C}{C})V_{in} \quad (2.9)$$

2.6 Dynamic Performance

Dynamic performance includes dynamic linearity, noise and distortion. The following measures are used to characterize the dynamic performance of an ADC. Signal-to-Noise Ratio (SNR) is the ratio of the signal power to the total noise power at the output of ADC with full-scale sinusoidal input. It can be calculated by Equation (2.10), with an N-point FFT of a signal [28].

$$SNR(dB) = Signal\ Peak(dB) - Noise\ Floor(dB) - 10\ logN \quad (2.10)$$

$$SNR(dB) = 6.02N + 1.76dB \quad (2.11)$$

Figure 2.13 shows the related graph.

Signal-to-Noise + Distortion Ratio (SNDR) is the ratio of the signal power to the total noise and harmonic power at the output of ADC with full-scale sinusoidal input. Dynamic Range (DR) is the range of input signal amplitudes within which the desired output can be obtained, that is, it is the input power range for which the SNR is greater than 0 dB. Spurious Free Dynamic Range (SFDR) is the ratio of the signal power to the largest spurious component within a certain frequency band. It is important for telecommunication applications. The Effective Number Of Bits (ENOB) is calculated with the following equation:

$$ENOB = \frac{(SNDR - 1.76)dB}{6.02dB} \tag{2.12}$$

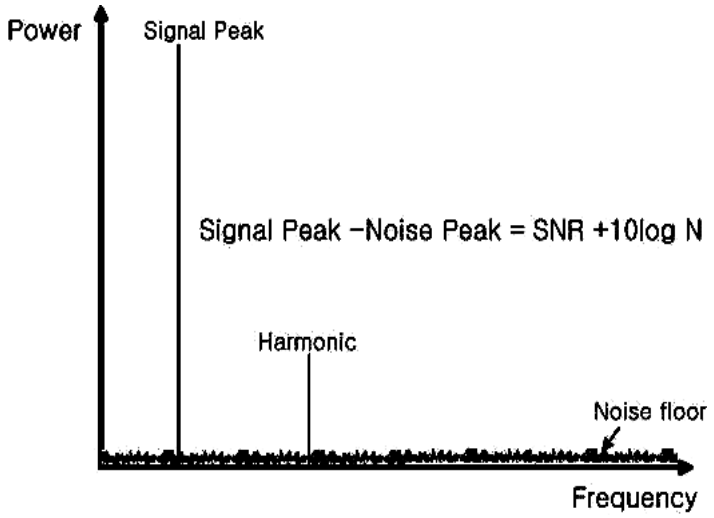


Figure 2.13 Procedure for Computing SNR from an N point FFT [28]

2.7 HID Lamp introduction in automotive industry

High Intensive Discharge is a technique for lighting and is based on the arc built within two electrodes. Recently, there has been an emerging demand to replace the conventional halogen headlamps with the newly introduced small-wattage metal halide HID lamps [43][44].

Compared to the conventional halogen headlamps, HID lamps offer 5 times better lumen efficacy as shown in Figure 2.14 and table 2.1, better color rendering, better focusing capability, and longer life (5000 hours vs. 1500 hours). These superior performances soon make them popular in some high-end cars. However, HID lamps have a specific issue in ballast design. These lamps need very complex controller due to their special transient