DESIGN AND IMPLEMENTATION OF UP-CONVERSION MIXER AND LC-QUADRATURE OSCILLATOR FOR IEEE 802.11a WLAN TRANSMITTER APPLICATION UTILIZING 0.18 μm CMOS TECHNOLOGY

by

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DECLARATION

I hereby declare that the work in this thesis is my own except for quotations and summaries which have been duly acknowledged.

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TABLE OF CONTENTS

CHAPTER SIX : QUADRATURE VOLTAGE CONTROLLED OSCILLATOR DESIGN

CHAPTER SEVEN : MEASUREMENT RESULTS

CHAPTER EIGHT : CONCLUSIONS AND FUTURE WORK

APPENDICES

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
A-MOS	Accumulation Metal Oxide Semiconductor
ASITIC	Analysis and Simulation of Inductors and Transformers for IC's
BGR	Bandgap Reference
BiCMOS	Bipolar-Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BPSK	Binary Phase Shift Keying
CAD	Computer Aided Design
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary to Absolute Temperature
DAC	Digital to Analog Converter
DFT	Design for Test
DSSS	Direct Sequence Spread Spectrum
DSBSC	Double Sideband Suppressed Carrier
DUT	Device Under Test
EM	Electro-Magnetic
EVM	Error Vector Magnitude
FCC	Federal Communication Commission
FFT	Fast Fourier Transform
FSK	Frequency Shift Keying
GaAs	Gallium Arsenide
GMD	Geometric Mean Distance
GSM	Global System for Mobile Communications

GSG	Ground Signal Ground
IC	Integrated Circuit
IF	Intermediate Frequency
IM	Intermodulation
I/O	Input-Output
IIP_3	Input Third Order Intercept Point
IP_2	Input Second Order Intercept Point
I/Q	In phase-Quadrature phase
ISM	Industrial, Scientific and Medical
ISI	Intersymbol Interference
KCL	Kirchoff Current Law
KVL	Kirchoff Voltage Law
LAN	Local Area Network
LC	Inductor-Capacitor
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Lower Sideband
MCM	Multi Carrier Modulation
MOS	Metal Oxide Semiconductor
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PGS	Patterned Ground Shield
PSK	Phase Shift Keying
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature

PVT	Process-Voltage-Temperature
PWL	Piecewise Linear
SNR	Signal to Noise Ratio
Q	Quality Factor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QVCO	Quadrature Voltage Controlled Oscillator
PTAT	Proportional to Absolute Temperature
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SAW	Surface Acoustic Wave
SCM	Single Carrier Modulation
SDR	Software Defined Radio
SIPC-QVCO	Source Injection Parallel Coupled QVCO
SNR	Signal to Noise Ratio
SoC	System on Chip
SSB	Single Sideband
TC	Temperature Coefficient
Tx	Transmitter
USB	Upper Sideband
U-NII	Unlicensed National Information Infrastructure
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
WLAN	Wireless Local Area Network
XDB	Gain Compression

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REKABENTUK DAN IMPLIMENTASI PENCAMPUR PENUKAR ATAS DAN PENGAYUN LC KUADRATUR, UNTUK APLIKASI PENGHANTAR IEEE 802.11a, WLAN MENGGUNAKAN TEKNOLOGI CMOS 0.18 μm

ABSTRAK

Perlumbaan implementasi litar terkamil radio, dengan kos yang rendah telah menggalakkan penggunaan teknologi CMOS. Disertasi ini memberikan rekabentuk pencampur penukar atas mengadaptasi topologi penyalir arus dengan pembekalan sumber voltan rendah dalam konfigurasi litar terlipat dan kompensasi titik pincang. Adaptasi teknik litar ini berupaya meningkatkan kelelurusan dan keberkesanan pensuisan bahagian penyalir arus dan kuad pensuisan pMOS di samping mengecapi piawaian penghantar dua langkah 5.15 – 5.35 GHz, IEEE 802.11a WLAN. Analisis yang mendalam serta rekabentuk tertingkat pengayun kuadratur terkawal voltan (QVCO), punca suntikan gandingan selari (SIPC) telah di bandingkan dengan pengayun kuadratur terkawal voltan, LC biasa, yang di implementasi berdasarkan peringkat gandingan silang pMOS. Rekabentuk, implementasi dan pengujian peringkat pelengkap SIPC LC-QVCO dengan integrasi litar penimbal gandingan silang salir terbuka 50 Ω seterusnya diperkenalkan mengecapi piawaian yang ditetapkan. Litar rujukan sela jalur (BGR) dengan voltan rujukan di simulasi pada 1.246 V, rangkaian litar rintangan berpemberat dan varaktor MOS mod susutan selari dengan pengaruh tindan berpilin perisai diri membentuk tangki penyalun LC, direkabentuk untuk di integrasikan dengan litar pencampur penukar atasan dan litar pengayun LC kuadratur dalam teknologi piawai CMOS 0.18 μm, 6 logam, 1 polisilikon. Topologi pencampur penukar atasan yang telah di integrasikan dengan rangkaian pincang pampasan, memberikan kelelurusan yang di simulasi pada 12.57 dBm, di sisi penganggu masukan saluran bersebelahan ketiga $\left(\mathrm{IIP}_3\right)$ dan memberikan 6.62 dBm julat dinamik masukan $\left(\mathrm{IP}_{1\mathrm{dB}}\right)$ pada 3.5 GHz frekuensi pengayun tempatan (LO) dan 10 – 500 MHz frekuensi

jalur dasar. Litar terkamil pencampur penukar atasan melesapkan 5.58 mW kuasa secara tersendiri di peringkat simulasi. Disertai dengan penyalir sambungan dawai dan pengaruh beban, litar pencampur penukar atasan memperlihatkan kuasa keluaran -65.57 dBm dengan masukan -22 dBm pada input BB dan -10 dBm pada input LO di peringkat pengukuran. Rangkaian pincang masukan ke peringkat penyalir arus dalam litar pencampur penukar atasan memerhatikan perubahan voltan pincang, V_b menghampiri 4 mV dalam julat suhu $-40\,^{\circ}C$ hingga $80\,^{\circ}C$ dengan pelesapan kuasa 0.986 mW di peringkat simulasi. Pengayun kuadratur terkawal voltan punca suntikan gandingan selari (SIPC-QVCO), pelengkap dan terganding tunggal pMOS masing-masing memberikan -113.22 dBc/Hz dan -111.43 dBc/Hz hingar fasa di peringkat simulasi pada 1 MHz frekuensi offset. Pelesapan kuasa dalam konfigurasi pengayun pelengkap dan terganding tunggal pMOS masing-masing adalah 17.73 mW dan 15.42 mW dengan 6.5 % dan 32.5 % julat penyelarasan terkawal pada 1.8 V sumber voltan di peringkat simulasi. Litar pengayun SIPC-QVCO telah diuji pada 2.67 GHz dengan pengukuran kemerosotan penyelerasan sebanyak 35 %. Tangki penyalun LC memberikan 32 % penyelarasan varaktor dengan 5.8 penghampiran faktor mutu, Q_{tank} pada 3.5 GHz frekuensi pusat. Pengujian tersendiri litar sela jalur, sepuluh konfigurasi pengaruh tindan berpilin, litar pencampur penukar atasan dan pengayun SIPC LC-QVCO pelengkap telah di laksanakan melalui teknik kuaran wafer dan pemuatan ke atas PCB.

DESIGN AND IMPLEMENTATION OF UP-CONVERSION MIXER AND LC-QUADRATURE OSCILLATOR FOR IEEE 802.11a WLAN TRANSMITTER APPLICATION UTILIZING 0.18 μm CMOS TECHNOLOGY

ABSTRACT

The drive for cost reduction has led to the use of CMOS technology for highly integrated radios. This work proposes a low voltage, folded, bias point compensation integrated CMOS active mixer with current draining adaptation to enhance the linearity and switching efficiency of the transconductor and pMOS based switching quad stage accommodating 5.15 GHz to 5.35 GHz, IEEE 802.11a WLAN two step up-conversion transmitter standards. An enhanced investigation and design of a source injection parallel coupled (SIPC) quadrature voltage controlled oscillator (QVCO) in comparison of the conventional LC-QVCO realized in pMOS based cross coupled switching stage is also presented. The design, implementation and characterization of the complementary stage SIPC LC-QVCO with integrated 50 Ω cross coupled open drain buffer, is subsequently proposed adapting the highlighted wireless standard. Implemented in 0.18 μm, 6 metal, 1 poly, 1.8 V standard CMOS technology and catering to the need of integration in the proposed up-conversion mixer and SIPC-QVCO topology, a low voltage high precision bandgap reference (BGR) circuit with a reference voltage simulated at 1.246 V, a regulated resistive weighted bias network and an integrated depletion mode MOS varactor accommodating a parallel combination of an on chip self shielding stacked spiral inductor forming an LC tank resonator, is presented. The compensated bias network integrated up-conversion mixer topology exhibit a comparable simulated linearity of 12.57 dBm with the accompanying simulated third order adjacent interferer $(\mathrm{IIP_3})$ and an input dynamic range $(\mathrm{IP_{1dB}})$ of 6.62 dBm at 3.5 GHz of LO frequency, with 10 – 500 MHz of input baseband frequency. The corresponding standalone up-conversion mixer topology

independently dissipates 5.58 mW of simulated power. Accompanied with bondwire and parasitic load degradation, the standalone architecture measures an output power of -65.57 dBm at the up-converted sideband, with -22 dBm and -10 dBm of input baseband (BB) and local oscillator (LO) power, respectively. The input bias network to the transconductor stage of the proposed up-conversion mixer observes a simulated bias voltage, V_b variation of approximately 4 mV over the temperature range of $-40\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$ while dissipating 0.986 mW of simulated power. The complementary and single coupled pMOS based SIPC LC-QVCO topology indicates a simulated phase noise performance of -113.22 dBc/Hz and -111.43 dBc/Hz at an offset frequency of 1 MHz, respectively. The respective simulated power dissipation in the complementary and single coupled pMOS stage is indicated to be 17.73 mW and 15.42 mW with accompanying 6.5 % and 32.5 % of simulated tuning range at 1.8 V of supply voltage. The proposed complementary based SIPC-QVCO architecture measures an oscillation at 2.67 GHz, with a tuning range degradation of 35 %. The integrating LC resonator tank exhibits, approximately 32 % of simulated independent varactor tuning with approximately 5.8, tank quality factor Q_{tank} at 3.5 GHz of center frequency. In this work a voltage precision bandgap reference, ten different independent stacked spiral inductor, an up-conversion mixer and a complementary SIPC-QVCO architecture were designed and characterized independently.

CHAPTER 1
INTRODUCTION

1.0 Overview

Starting from the discovery of transistors sixty years ago by John Bardeen and Walter Brattain on the fourth floor of Building 1 at Bell Labs in Murray Hill, NJ (Brinkman *et al*., 1997), the complementary metal oxide semiconductor (CMOS) technology had evolved as depicted by Moore's Law in dimension shrink orientated by the decrease in price-per-performance for digital architecture (Annema *et al*., 2005).

To ensure sufficient life time and power consumption the advancement of CMOS technology is accompanied by lowering the supply voltages, which is beneficial for digital circuit and not so for analog circuit, because the signal headroom becomes too small to design circuits with sufficient signal integrity at reasonable power supply. Supply voltage reduction from 5 V in the nineties down to less than 1 V today, scales the transistor down to 0.1 μm and beyond, which introduces much variations in device characteristic, such as the threshold voltage and drain current, due to nonuniformity and random factors in processing. Such variation is denoted as MOS transistor mismatch (Zhang *et al*., 2001).

Architecture exploiting mixed-signal systems such as frequency synthesizers, digital to analog converter (DAC) and analog to digital converter (ADC), often integrated with analog circuitry such as amplifiers, input-output (I/O), radio frequency (RF) front ends and many more. In the case of realizing a system on chip (SoC) solution, the analog blocks must cope with the CMOS advancement in digital circuit, where the scaling of CMOS technology promises gigabit integration (Kenington, 2005).

Advancements in wireless technology have largely been driven by the desire for lower cost, low power dissipation, low voltage headroom consumption and low nonlinearity solutions in building high performance RF circuits in silicon, particularly CMOS (Guan and Hajimiri, 2004). However the quest for higher data rate, network capacity, transmit range and multi standard radio solution has driven the CMOS process in high operating frequency band, further exploiting the transit frequency, f_T of the transistor and paving room in the realization of bulky on-chip passive devices, thus eliminating the need for costly discrete components integration, (Weldon *et al*., 2001).

The circuits for the front-end radio frequency (RF) signal processing are typically implemented in silicon Bipolar, bipolar-complementary metal oxide semiconductor (BiCMOS), or in gallium arsenide (GaAs); whereas, these technologies offer better analog circuit performance in comparison to lossy silicon substrate which makes the design of high quality factor reactive components difficult (Niknejad, 1998), they are more expensive and unsuited for the implementation of high density digital functions. From the economic point of view the realization of mobile terminals in a single chip and with low power consumption is very desirable, but a fully integrated single chip realization is only feasible if the analog RF circuits are realized in the same integrated circuit (IC) technology as the digital circuits (Rofougaran *et al*., 1996). Therefore, much research is conducted to evaluate the implementation of a full transceiver using standard CMOS technology. The design architecture of the analog RF signal processing circuits in a standard CMOS technology has a growing concern of performance as the translinear behavior of the bipolar transistor does not translates into the transconductance behavior of the CMOS transistors in adapting the conventional architecture of bipolar circuitry.

The rectification of the IEEE 80.11 standard for wireless local area networks (WLAN) in 1997 (Zhang, 2005), has resulted in an impressive growth of multi standards

(IEEE 802.11a/b/g) system. The proposed research is carried out in order to realize a fully integrated RF front-end balanced modulator transmitter blocks in compliance to IEEE 802.11a WLAN applications in deep submicron 0.18 μm standard CMOS technology. The integrating blocks are namely the integrated up-conversion mixer comprised of folded four quadrant multiplier, quadrature voltage controlled oscillator (QVCO), where the integration encapsulates the balanced modulator architecture feeding into a class A power amplifier (PA), exploiting the phase and amplitude modulation scheme utilized.

1.1 Objectives

The proposed research is carried out in effort of realizing a two step transmitter functional blocks (Zhang *et al*., 2003) in compliance with IEEE 802.11a, WLAN application realized in 0.18 μm, 6 metal, 1 poly standard CMOS process. The two step up-conversion transmitter alleviates injection pulling from the output of the PA (Razavi, 1998) and relaxes the tight constraint of error vector magnitude (EVM) of the I (in phase) and Q (quadrature phase) matching, (Kenington, 2005).

A highly linear, low voltage, high switching efficiency and low power dissipation integrated mixer topology is proposed exploiting a fully differential folded architecture in the effort of relaxing, voltage headroom consumption, on-chip bulky de-coupling devices (Manku and Shin, 1998) and even order harmonic distortion, which may be problematic in applications containing an amplitude-modulation component (Yamaji, 1998). In this work a fully differential architecture of a double sideband (DSB) mixer, with current draining feature is adapted (Koh *et al*., 2004), which serves as a core building block for the single sideband (SSB) modulator. The conventional stacked Gilbert cell mixer is to be avoided, due to the difficulty in operation at such low voltage owing to the stacking of devices (Wang, 1998). The realized integrated topology is able to suppress the effects of this limitation and produces a highly linear response at the

output, compensated to the process, voltage and temperature (PVT) variation, increasing the robustness of the designed circuit. The regulated network exhibits decreased temperature dependency with improved matching. The integrated error amplifier based regulated dc biasing circuit (Harish *et al.*, 2004) and the accurate poly interdigitated weighted resistor generates the reference biasing voltage from the constant bandgap precision output (Mok and Leung, 2004). Thus, the integrated mixer gates are biased at a constant voltage value regardless of temperature or process skews.

In an attempt to reduce the cost per unit area of the designed RF CMOS block on lossy silicon (Si) substrate, bulky passive components such as on chip planar inductor is essential. The planar inductor finds its way to various applications which includes narrow band matching, degeneration and LC resonator realization. The performance dependency on the geometric variation of the on chip passive components is analyzed, optimizing for the highlighted application. Performance enhancement techniques such as pattern ground shielding (PGS), (Talwalkar, 2003) and stacked self shielding is exploited to improve the quality factor (Q_L) of the planar inductor. The tuning percentage of various MOS based varactor is also analyzed in a LC resonator integration (Andreani and Mattison, 2000).

An improved pMOS based source injection parallel coupled quadrature voltage controlled oscillator (SIPC-QVCO) architecture with superior phase noise performance, low amplitude error and high tuning range is explored with regard to the conventional realization, catered towards the proposed IEEE 802.11a two step up-conversion oscillation frequency (Ramiah and Zulkifli, 2007). The SIPC-QVCO is to provide an extended voltage swing with scalable voltage supply. The SIPC-QVCO is to be operated in the range of 3 GHz to 4 GHz with high percentage of tuning, utilizing on-chip depletion mode pMOS based varactor (Andreani and Mattison, 2000). The SIPC-

QVCO is to provide an output power of –10 dBm to 0 dBm in order to hard switch the switching quad of the designed mixer topology (Rogers and Plett, 2003). The effect of dimension ratio of the parallel coupling transistor to the switching transistor is analyzed in the quadrature voltage controlled oscillator architecture with the integration of on-chip LC tuning tank.

1.2 Contributions

This thesis orientates in the design evolution, optimization and comparison of RF building blocks of the transmitter balanced modulator consisting the up-conversion mixer and SIPC based LC-QVCO topology, accommodating for IEEE 802.11a WLAN application. Seven contributions to this field of research had been highlighted, with the last four being the primary accomplishment.

(i) The design and characterization of low voltage precision bandgap reference circuit is proposed accommodating the integration of poly resistor with low temperature coefficient and enhanced matching property. The circuit results in 2.7 mV of simulated reference voltage variation in the temperature span of $-40\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$. The characterization measures a variation of 2.83 % at a temperature span of $35\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$

(ii) Simulation investigation of the tuning performance of eight different types of MOS varactor ranging from depletion, inversion and accumulation mode of operation with the tuning input applied at the gate and diffusion alternately were initiated. The importance of $\mathrm{C_{max}}/\mathrm{C_{min}}$ ratio is highlighted in the selection of an appropriate varactor for the LC-QVCO resonator integration.

(iii) Simulation investigation on the effect of dimensional geometric variation of the on-chip spiral inductors to the inductance, L, quality factor, Q_L and self resonant frequency, f_{sr} is reported. The characterization on the effect of non-PGS and

underlying PGS integration to the independent spiral inductor samples was initialized.

(iv) A 9.31 mW, 3.5 GHz, -2.09 dBm of input adjacent linearity $(\mathrm{IIP_3})$ and -9.82 dBm of input 1 dB compression point $(\mathrm{IP_{1dB}})$, folded low voltage current draining up-conversion mixer was simulated and realized in 0.18 μm, 6 metal, 1 poly standard CMOS process. The proposed design exhibits high switching efficiency and high linearity with the adaptation of the desirable current draining feature. An integrated CMFB bias current control compensates the architecture over bias point variations. The integration pMOS based input switching quad is adapted benefiting direct dc coupling and enhanced isolation at 3.5 GHz of LO frequency. The mixer measures an output power of -65.57 dBm at the up-converted sideband, with -22 dBm and -10 dBm of input baseband (BB) and local oscillator (LO) power, respectively. The LO-RF and LO-BB isolation measures to be 54 dB and 36 dB respectively, whereas the BB-RF isolation measures to approximate 63 dB.

(v) A 6.84 mW, 3.5 GHz of LO frequency, 12.57 dBm of input adjacent linearity $(\mathrm{IIP_3})$ and 6.63 dBm of input 1 dB compression point $(\mathrm{IP_{1dB}})$, low voltage current draining folded, regulated bias integrated up-conversion mixer topology was simulated and implemented in 0.18 μm standard CMOS technology. Adapting the beneficial features of the standalone architecture, in this design the on-chip integration of the regulated bias network reduces the temperature dependence over the range of $-40\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$. The proposed design was simulated and cross compared with recent reported architectures.

(vi) The effect of scaling ratio between the coupling transistor and switching transistor to the amplitude and phase noise degradation is investigated through simulation verification. The effect of scaling ratio K was extracted respective to the proposed pMOS based single coupled SIPC LC-QVCO in comparison with

the conventional single coupled parallel LC-QVCO topology, at 3.5 GHz of oscillating frequency.

(vii) A -113.2 dBc/Hz of phase noise at an offset frequency of 1 MHz with 6.5 % of tuning range at the center frequency of 3.5 GHz complementary SIPC LC-QVCO architecture with integrated 50 Ω open drain buffer is simulated and proposed, accommodating the phase noise relaxation technique. The circuit is implemented and characterized consuming an active chip area of $2.19\,\mathrm{mm}^2$ in 0.18 μm standard CMOS technology. The proposed architecture measures to oscillate at 2.67 GHz with a tuning range of 180 MHz, via wafer probing.

1.3 Thesis Outline

This thesis describes the design and analysis of low voltage CMOS integrated building blocks utilized in two step up conversion transmitter front end, comprising of up-conversion mixer topology and quadrature voltage controlled oscillator architecture, in compliance with IEEE 802.11a standard for the UNII band from 5.15 to 5.35 GHz.

Chapter 2 describes the IEEE 802.11a criterion, highlighted for both in door and out door application. The selective frequency fading tolerant multicarrier modulation approach, enhanced to orthogonal frequency division multiplexing (OFDM) is explained in brief. The conventional direct up-conversion transmitter and the subsequent frequency planning for the realization of two step up-conversion transmitter is proposed with a forecast of performance.

In Chapter 3, the design and analysis of low voltage PVT compensated state of the art circuits, comprising folded cascode operational amplifiers, bandgap reference circuit and error amplifier based voltage regulator, are presented. The voltage regulator integrated with input bandgap precision circuit and a weighted resistive feedback array

is designed to provide process skew and temperature variation error less than 5 mV, of output biasing voltage accommodating the needs of the designed RF building blocks, mainly the realized up conversion mixer topology.

In achieving high level of integration in analog RFIC, on chip spiral inductors and MOS varactors are explored in Chapter 4, accommodating for tunability, matching and shunt-series peaking on silicon. On chip passive components integration introduces less noise, consumes less power and have a wider bandwidth and linear operating range than the respective active equivalent. Chapter 4 reviews the design of an on-chip MOS varactor and on-chip planar spiral inductors adopting the needs of the degeneration and resonator tuning, in the up conversion mixer topology and the quadrature voltage controlled oscillator (QVCO) topology, respectively. Issues such as skin effect and substrate effect on planar spiral inductors with physical lumped models will be addressed. The enhancement technique of the spiral inductor Q_L factor on lossy silicon would also be reviewed, accompanied by extensive simulation analysis.

The detailed circuit design and analysis of the proposed folded up-conversion mixer, suitable for low voltage application, followed by the integration with the PVT compensated biasing network and linearity enhancing inductive degeneration are described in Chapter 5. In Chapter 6, the design and analysis of the reliable implementation of an on-chip high Q_L stacked rectangular inductors and depletion mode pMOS based varactor forming the LC resonator, integrated with the proposed low phase noise source injection parallel coupled quadrature voltage controlled oscillator (SIPC-QVCO) in comparison to the conventional LC-QVCO counterpart is presented. The equivalent experimental result of the PVT compensated biasing network, on chip passive devices and the test bench set up of the integrated up-conversion mixer, together with the SIPC-QVCO topology is discussed in Chapter 7. The conclusions and future work recommendations are presented in Chapter 8.

CHAPTER 2
LITERATURE REVIEW

2.0 IEEE 802.11a Criterion

Interference problem lies in the regulations for transmit power level in the 2.4 GHz industrial, scientific and medical (ISM) band. In accordance to federal communication commission (FCC) 15.247 rules, in the band of 2.40 GHz to 2.48 GHz, it is stated that both frequency hopping spread spectrum (FHSS) and direct sequence spread spectrum (DSSS), potentially have a maximum peak output power of 1 W. This drawback leads to the interference of narrowband FHSS device with a wideband DSSS device (Bing, 2002). This situation is of a grave concern of interference in the unlicensed channel.

In contrary to the regulation for the unlicensed national information infrastructure (U-NII), a 5 GHz of application had been expertly crafted. Table 2.1 shows the IEEE standards with the corresponding output power levels laid out by the regulatory bodies for different parts of the 5 GHz spectrum and in comparison with IEEE 802.11b, outlined in United States (Bing, 2002). The range of performance of 5 GHz 802.11a systems is evaluated in terms of data link rate and throughput associated with the adapted modulation scheme.

Table 2.1: Approved IEEE standards (valid only in US per FCC regulations)

Standards	**802.11a**				**802.11b**
Date approved	Sept. 1999				Sept. 1999
Frequency (GHz)	5.15–5.25	5.25–5.35	5.470–5.725	5.725–5.825	2.4–2.4835
Output power (mW)	50	250	NA	1000	1-100
	Outdoor/Indoor			Outdoor	Outdoor/Indoor
Date rate (Mbps)	6, 9, 12, 18, 24, 36, 48, 54				1, 2, 5.5, 11
Modulation Type	OFDM				DSSS

The FCC in United States and other regulatory international bodies tend to control the use of RF spectrum and limit the power of devices. The IEEE 80.211a standard, which is based on OFDM modulation, provides nearly five times the data rate and as much as ten times the overall system capacity as currently available 802.11b wireless LAN system. The 802.11a standards operates in 5 GHz UNII band, which provides a total available signal bandwidth of 300 MHz, as compared to the 85 MHz available for 802.11b.

The 802.11b wireless LAN standard attempts to deliver maximum performance within the limits set by these bodies. Low output power, limits 802.11b wireless LAN transmission to short effective ranges, measured in hundreds of yards. The full set of data rates for 802.11b wireless LANs is 11, 5.5, 2 and 1 Mbps, where higher data rates rely on more complex spectrum spreading techniques, where the network throughput diminishes with distance and interference (Hara, 2003). The DSSS refers to one particular approach to packing more data into a given piece of RF spectrum (more data in channel).

The outlined regulations for 802.11a provides higher throughput with increased data rate up to 54 Mbps throughout the coverage area. Being spectrally clean and wide, the upper unlicensed national information infrastructure (U-NII) band from 5.725 to 5.825 GHz is best suited for outdoor fixed broadband wireless access devices, which typically requires much higher power levels to reach longer distance. The lower 200 MHz band (5.15-5.35 GHz band) will serve indoor/in building as well as outdoor wireless LANs better (Bing, 2002). The orthogonal frequency division multiplexing (OFDM) modulation or multiplexing scheme refers to a special form of multicarrier modulation (MCM), where a single data stream is transmitted over a number of lower rate subcarriers.

2.0.1 Multicarrier Approach

MCM is the principle of transmitting data by dividing input stream into several symbol stream, each of which has a much lower symbol rate and by using these substreams to modulate several subcarriers. The transmitted signal can be degraded with a combination of effects of attenuation, reflection and diffraction (Bing, 2002). The parallelism introduced by OFDM benefits the transmitted symbol with less susceptibility to selective frequency fading, as illustrated in Figure 2.1 (Hara, 2003), where f_1, f_2, f_3 and f_N, denotes the respective frequency of the Nth subcarrier.

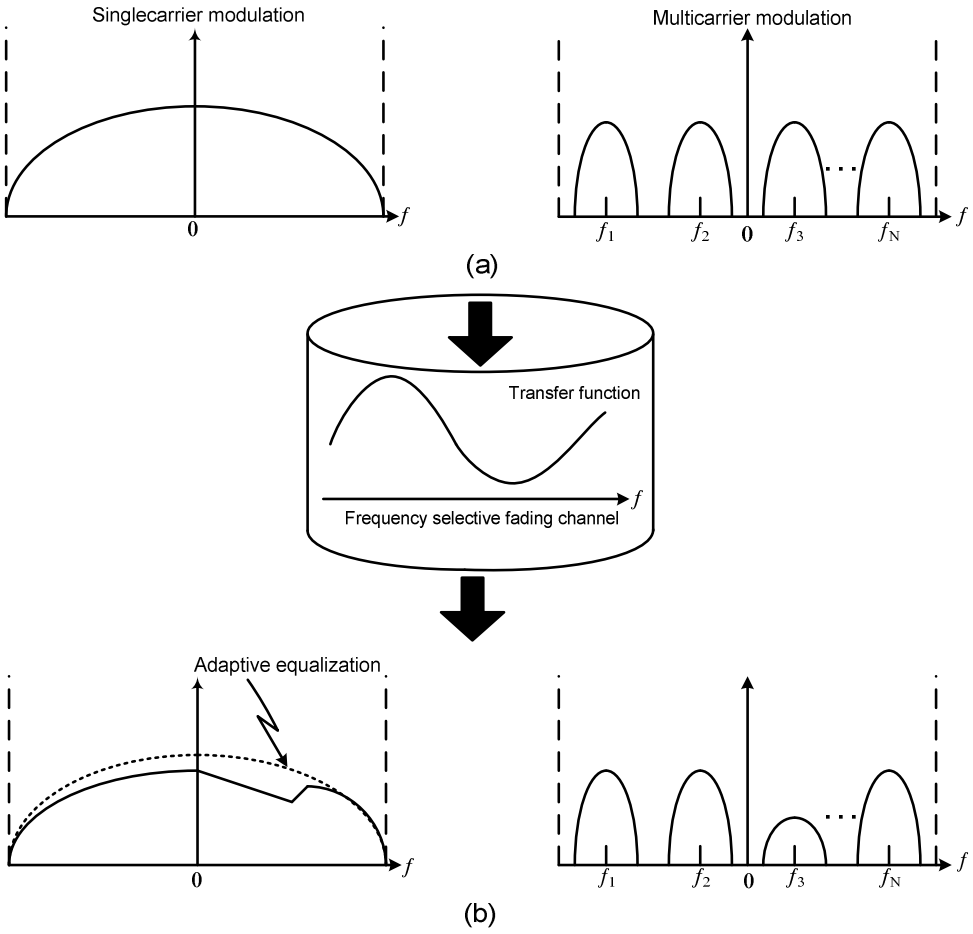


Figure 2.1: Comparison of single carrier modulation (SCM) and MCM immunity towards channel interference with the respective (a) frequency spectra of transmitted signals, (b) frequency spectra of received signals.

Suppose that data is being transmitted using only a single carrier, if the channel introduces interference at this frequency, as described in Figure 2.1, the entire transmission can fail and a complicated adaptive equalization would be needed. This scenario will have a lesser effect on a multicarrier system, because only a few of the subcarriers would be affected. It is clear that MCM is effective and robust in wireless channels namely, to combat frequency selective fading, where MCM requires no equalization (Hara, 2003).

Unwanted echoes or multipath fading resulting from the arrival of transmitted signal at different times, signal strengths and power are due to reflection of a transmitted wave by local scatters such as houses, buildings, and man made structures, or natural objects such as forest surrounding a mobile unit. As the reflected signals arrive at different times, as a function of distance between the transmitter and reflectors, the received symbol can potentially be corrupted by echoes of previous symbols. This effect is defined as intersymbol interference (ISI), where higher bit rates are more vulnerable to ISI (Hara, 2003).

OFDM's parallelism finds a way to mitigate the ISI solution, by increasing the transmission interval of N different subcarriers splitting a high rate data stream into a number of lower rate streams by a factor of N, where each stream being sent using independent carrier frequency. Because the symbol duration increases for the lower rate parallel subcarriers, the relative amount of dispersion or signal spreading in time caused by multipath delay spread is decreased. This means that each subcarrier is now N times more multipath and ISI tolerant. In terms of IEEE 802.11a standard, N is equal to 52 (Bing, 2002). ISI is further eliminated almost completely by introducing a guard interval in each OFDM symbol, where the OFDM signal is cyclically extended to avoid intersubcarrier interference.

2.0.2 Orthogonal Frequency Division Multiplexing (OFDM)

The name of “OFDM” appeared in the U.S. Patent No.3 issued in 1970 (Hara and Prasad, 2003 and Hara, 2003). In an OFDM transmitter data sent for each subcarrier is encoded by a certain modulation scheme. The modulation scheme usually used is either phase shift keying (PSK), where the data is represented as different phase offsets of a signal or quadrature amplitude modulation (QAM), where data is represented by changing both amplitude and phase. Data rate corresponding to 6 and 9, 12 and 8, 24 and 36, 48 and 54 Mbps are represented by binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16 quadrature amplitude shift keying (16 QAM) and 64 quadrature amplitude shift keying (64 QAM), modulation scheme respectively (Schiller, 2000).

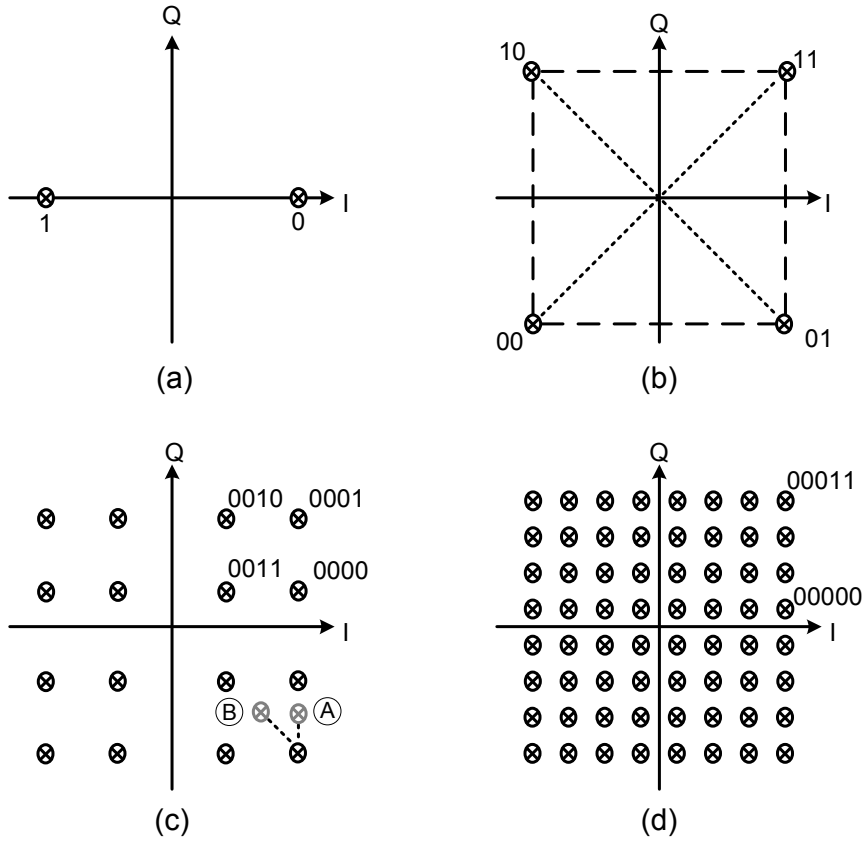
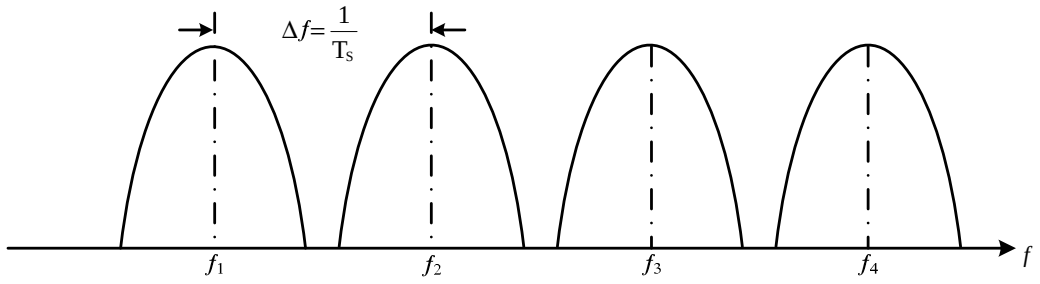


Figure 2.2: Phase domain constellation plot of (a) BPSK, (b) QPSK, (c) 16 QAM, (d) 64 QAM.

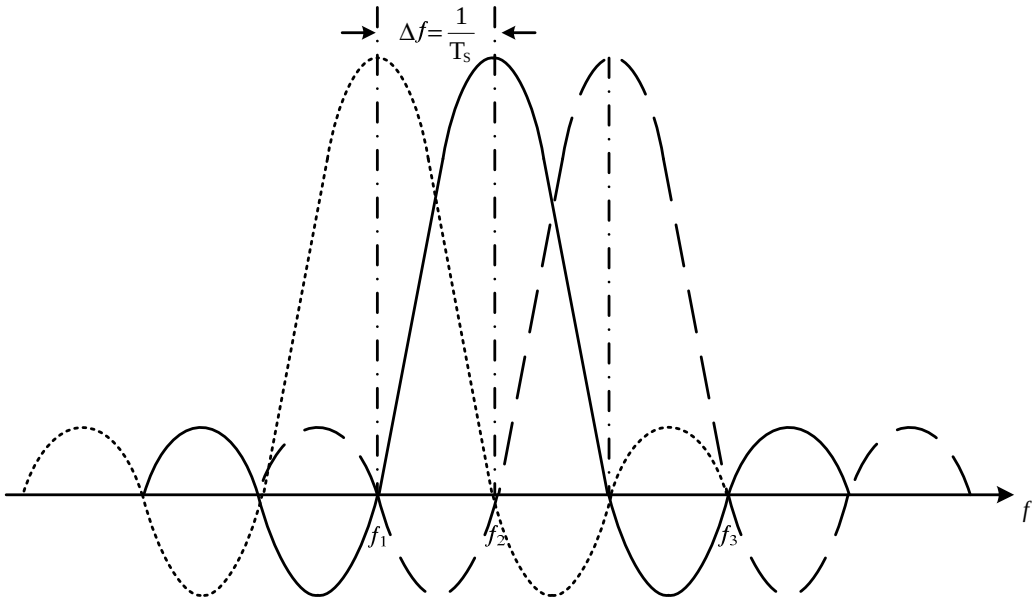
Figure 2.2 describes the phase domain representation of the highlighted modulation schemes. Higher bit rates is achieved for the same bandwidth by coding two bits into one phase shift as illustrated in the QPSK modulation in comparable with BPSK modulation. Error vector magnitude (EVM) indication wholly based on the constellation plot indicates the performance of linearity and phase noise of the system. In the case of constellation shift to state A, as described in Figure 2.2(c), magnitude error dominates, whereas a shift in state B, as described in Figure 2.2(c), indicates a domination of both magnitude and phase error (Zhang *et al*., 2003). The more constellation points are used in the phase domain, the harder it is to separate the incurred error (Schiller, 2000).

The orthogonality comes from the precise relationship between the subcarriers that make up one OFDM symbol. Figure 2.3 compares the frequency spectra of the classical MCM, employing nonoverlapped band limited orthogonal signal as described in Figure 2.3(a), with the frequency spectra of the OFDM signal, as described in Figure 2.3(b). The classical MCM, matches the use of analog subcarrier oscillators and filters, but it requires much wider bandwidth.

The frequency domain representation of each subcarrier in the OFDM spectrum is represented by a sinc function which are widely spread and overlapped, resulting in an efficient use of the frequency spectrum. One property of this sinc function is that the peak at its center frequency occurs to the zero at all integer multiples of this frequency (Bing, 2002). The OFDM receiver can effectively demodulate each subcarrier because, at the peaks of each of these sinc functions, the contributions from other subcarrier sinc functions are zero. From Figure 2.3, f_1, f_2, f_3 and f_4, corresponds to the number of subcarriers respectively, whereas the symbol duration of the subsequent subcarrier level is defined as $\mathrm{T_S}$, where $\Delta f = 1/\mathrm{T_S}$.



(a)



(b)

Figure 2.3: Comparison of frequency spectra for a given bandwidth usage with (a) nonoverlapped band limited orthogonal signals (MCM), (b) overlapped time-limited orthogonal signals (MCM), where orthogonality is achieved when the peak of each subcarrier spectrum occurs at the nulls of all other subcarriers.

2.1 Single Step Up-Conversion Transmitter Architecture

Transmitter perform three primary functions; modulation, frequency translation and power amplification. The direct upconversion transmitter as illustrated in Figure 2.4, is attractive because of the simplicity of the signal path, the in-phase (I) and

quadrature (Q) baseband digital signals first passes through a digital to analog converter (DAC) and then filtered by a low pass filter (LPF) to remove the alias at the sampling frequency prior to the upconversion. Defining the I and Q input signal to the up converter topology as $A_b \sin \omega_{BB} t$ and $A_b \cos \omega_{BB} t$ respectively, where A_b corresponds to input baseband amplitude and ω_{BB} denotes the input baseband frequency. Frequency translation to a fixed RF frequency is then performed by the I/Q mixers after which the signal is summed and up converted, resulting in $-2A' \sin(\omega_c + \omega_{BB})t$, where the input local oscillator (LO) signal is defined as $A_c \sin \omega_c t$ and A' is the product multiplication of A_b and carrier amplitude A_c, with the corresponding carrier frequency of ω_c. Channel tuning is typically performed with a single RF channel-select frequency synthesizer. In particular, integrating a low-phase noise RF channel-select frequency synthesizer using low quality factor components would be difficult for narrow-band cellular standards such as Global System for Mobile Communications (GSM). This would lead to the use of a discrete voltage controlled oscillator (VCO) tank circuit to meet the required phase-noise performance with reasonable power consumption.

The signal then passes through a RF filter to suppress LO harmonics, which may violate the spectral mask requirements and cause distortions to the PA. The desired output power level is achieved by providing gain with a discrete PA. Finally, a discrete bandpass filter removes energy transmitted outside of the desired band.

The intermediate frequency (IF) filtering requirements can be relaxed if the intermediate frequency is selected such that none of the LO harmonics fall directly in the transmit or receive band where emission specification is usually the most stringent. Furthermore, increasing the IF will push the image band further away from the desired signal allowing more image rejection by RF filters. Finally, a differential signal path can

suppress the even-order harmonics, further relaxing the filtering requirements. Moreover, the IF filter may be eliminated all together with a direct up-conversion transmitter as shown in Figure 2.4.

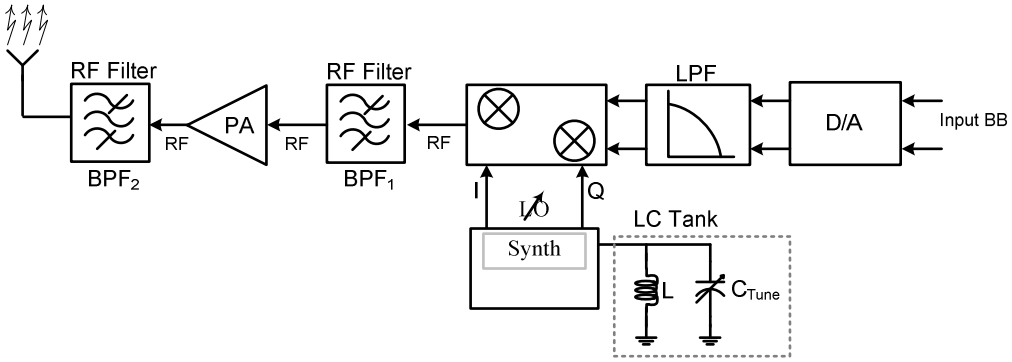


Figure 2.4: Conventional direct conversion transmit path.

The single step or direct conversion transmitter (Kundert, 1999) uses an I/Q modulator and performs frequency translation in one step. Since no IF exist, an IF filter is not required in this architecture. This design further lowers the requirements of the bandpass filter before the PA, which reduces unwanted harmonics and noise from the up-conversion process. The inclusion of this filter may allow a lower performance RF filter, which attenuates all energy outside the transmit band to be used. If, however, the bandpass filter before the PA is removed to achieve higher integration, a higher performance RF filter may be required after the PA. This requirement may lead to a larger insertion loss through the RF filter and reduces the effective efficiency of the PA by lowering the output power at the antenna for a given input power.

Thus a tradeoff exists between integration and power consumption. The bandpass filter before the PA may be integrated, but the performance of on-chip RF bandpass filters is limited by the low quality factor components (Abidi, 1999); hence, there is a need of an off-chip discrete bulky component. Therefore, because more

filtering is required by the RF front end filter after the PA, power consumption increases. Minimizing the spurious tones and noise created by the up-conversion is therefore necessary to reduce power consumption. Aside from the need for discrete components, the direct upconversion transmitter suffers from some well-known problems. First, the local oscillator (LO) feedthrough is relatively large because of the high frequency used in the I/Q modulator. Secondly, the LO pulling which occurs due to the transmitted signal running at the same frequency as the LO, contributes severely to the degradation of the direct conversion architecture, (Razavi, 1998).

2.2 System Review

The spectral efficiency of a 802.11a standard requirement results in a complicated transceiver design with strict tolerance on the radio performance. The use of 64-QAM modulation maintains a signal-to-noise ratio (SNR) of 30 dB, which is much higher than that required by the Bluetooth FSK modulation scheme and 802.11b, QPSK modulation scheme (Zargari *et al*., 2002). The high SNR requirement reflects to a stringent phase noise performance for the frequency synthesizer and tight I/Q phase and amplitude matching constraints for the transmitter and receiver.

OFDM, which is highly desirable due to its tolerance to multipath interference and ISI, complicates the transceiver design. In a case where each of the 52 subcarriers of the OFDM signal is represented by a single sinewave, such that the composite waveform in the time domain will have large peaks and valley, with each subcarrier is exactly an integer number of cycles in a given T time interval (Bing, 2002). In other words within one OFDM symbol, each subcarrier frequency is an integer multiple of a base frequency, as illustrated in Figure 2.5, where for illustration simplicity the phase offsets of the subcarriers are shown to be the same.

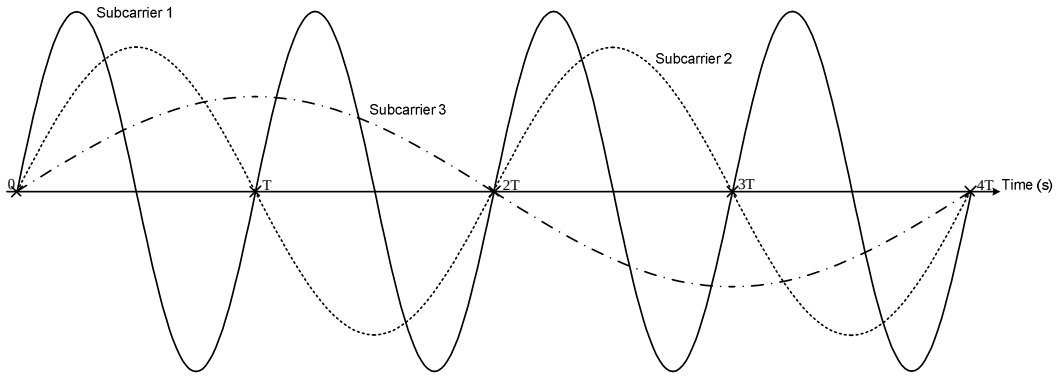


Figure 2.5: An example of 3 subcarriers transmitted in 1 OFDM symbol.

If 52 subcarriers are represented in time and the peak of one of the carrier is 52 times larger that of another single sinewave, the peak to average ratio will be $10\log(52) \cong 17\ \mathrm{dB}$ (Zargari *et al*., 2002). Hence, the transceiver should be able to accommodate signals whose peak amplitudes are 17 dB larger than the average signal, which in turn sets a stringent requirement for a large power backoff in the transmitter and wide dynamic range in the transmitter and receiver.

2.2.1 Frequency Planning

Figure 2.6 illustrates the proposed LO frequency generation scheme, consisting a QVCO based on $-g_m$, cross coupled LC resonators, operating at two thirds of the LO frequency, generating both in phase (I) and quadrature phase (Q) differential signals (Zhang *et al*., 2003). In this case LO frequency is set to be 5.25 GHz, corresponding to the 5.15-5.35 GHz of 802.11a UNII band with a maximum output power of 250 mW. A divide by two circuit consisting current mode logic (CML) based D-latch forms the dynamic frequency division network (Wang, 2000). As the QVCO operates at two thirds of the LO frequency, this scheme can effectively avoid frequency pulling effect from the output of the PA to the LO signal and reduce LO-RF interaction, increasing the isolation (Razavi, 1998).

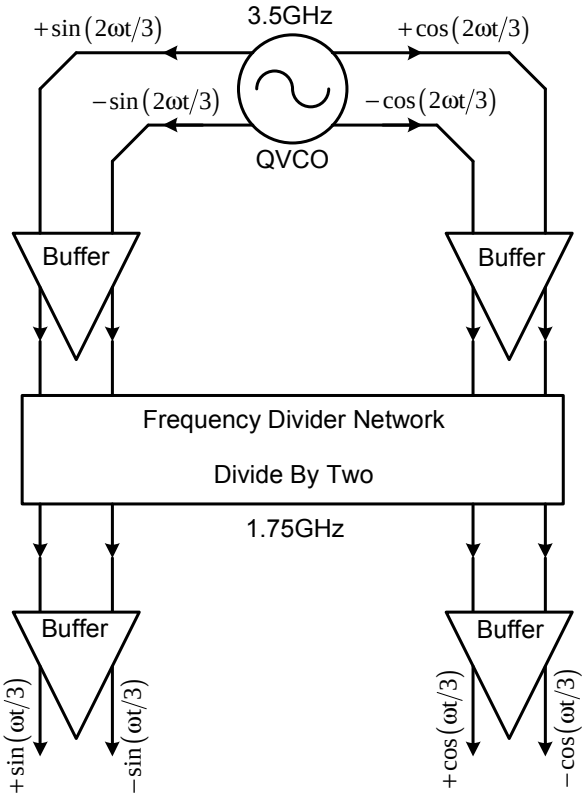


Figure 2.6: Proposed frequency planning for IEEE 802.11a transmitter topology.

2.2.2 Two Step Up-Conversion Transmitter

The proposed frequency planning scheme plays an important role in the architecture construction of the overall system. The super heterodyne architecture requires the integration off-chip surface acoustic filter (SAW). As the direct conversion suffer from drawbacks such as local oscillator frequency pulling, flicker noise and poor quadrature matching which is unsuited for the new generation of multicarrier based standards (Zargari, 2002), a modified two-step up-conversion architecture is proposed. The proposed architecture, together with the signal flow characteristic is described in Figure 2.7. The market of power amplifier (PA) for 5 GHz WLANs is currently dominated by state of the GaAs or silicon germanium (SiGe) fabrication technologies (Italia *et al*., 2005).

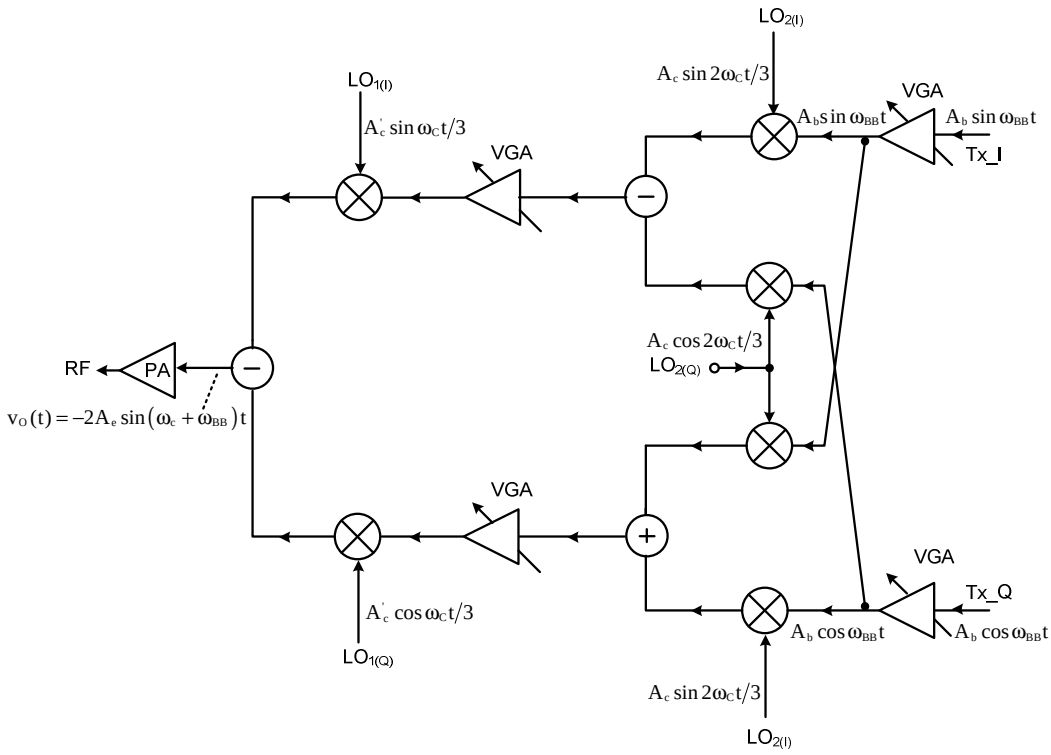


Figure 2.1: Two step up-conversion transmitter architecture.

Given the input local oscillator signal as, $\mathrm{LO_2} = \mathrm{A_c^{'}} \sin 2\omega_c t/3$ and $\mathrm{LO_1} = \mathrm{A_c} \sin \omega_c t/3$ respectively, where $2\omega_c/3$ denotes the local oscillator or the carrier frequency. Considering the input baseband signal as $\mathrm{A_b} \sin \omega_{BB} t$, where ω_{BB} denotes the input frequency and neglecting the gain introduced by variable gain amplifiers (VGA) for simplicity, the output RF signal is given by:

$$\mathrm{v_o}(t) = -2\mathrm{A_e} \sin\left(\omega_C + \omega_{BB}\right) t\,, \tag{1.1}$$

where $\mathrm{A_e} = \mathrm{A'_c} \times \mathrm{A_c} \times \mathrm{A_b}$, the negative signs indicates a phase reversal in the output signal. An in depth derivation of the signal flow characteristic for Figure 2.7 is given in Appendix A.

A basic description on forecast results of the system performance is as in Table 2.2, (Zargari *et al*., 2002, Zhang *et al*., 2003, Zhang *et al*., 2005 and Maeda *et*

al., 2006). Operating in the frequency ranges of 5.15 to 5.35 GHz, corresponding to an equivalent two step up-conversion in a frequency range of 3.43 to 3.57 GHz, the transmitter is estimated to dissipate less than 198 mW of power. With an output dynamic range of at least 5 dBm, output linearity is estimated to at least 15 dBm. The LO phase noise is estimated to be less than -110 dBc/Hz at 1 MHz of offset frequency, to relax the in band spurs at the output, further reducing the integration of high Q off chip filters. The SoC is economically integrated and realized in 0.18 μm, 6 metal, 1 poly standard CMOS technology.

Table 2.2: Forecast result of the IEEE 802.11a transmitter performance

Quantity	**Expected results**
Supply Voltage	1.8 Volt
Current Consumption	<110 mA
RF Frequency	10 MHz-500 MHz
LO Frequency	3.5 GHz, 1.75 GHz
Tx max output power	>-5 dBm (EVM<-33 dB)
LO integrated Phase Noise	<-110 dBc/Hz
Tx Output P_{1dB} @ 5 GHz	>5 dBm
Tx OIP_3 @ 5 GHz	>15 dBm
Realized in 0.18 μm , 1 poly 6 metal standard CMOS technology	

CHAPTER 3
LOW VOLTAGE HIGH PRECISION REFERENCE CIRCUIT DESIGN

3.0 Introduction

While digital circuits benefits greatly from high transconductance of short-channel MOS transistors, analog circuits performance are limited by low voltage gain, higher gate capacitance and even gate leakage. In compliance to Moore's Law, where the number of transistors on chip basically doubles every two years, the digital density has been moving up for 0.18 μm to 0.13 μm and 90 nm, pushes up to 65 nm and 45 nm, limiting the voltage headroom consumption of the analog design. Low supply voltage headroom reduces the signal dynamic range at the output (Gulati and Lee, 1998). The low supply voltage headroom of the core transistor often necessitates specialized design technique in designing high precision CMOS voltage reference with no external components (Dehgani and Atarodi, 2003).

This work circumvents the need for an accurate on-chip voltage reference circuit insensitive to temperature, power supply and load variations, comprising a low voltage lateral pnp based bandgap reference circuit and regulated error amplifier based voltage reference circuit (Harish *et al*., 2004). Apart from several reported voltage reference circuits, bandgap voltage is the most popular approach due to its accuracy, reliability and compatibility with CMOS technologies. The regulated error amplifier based voltage reference circuit allows simultaneous setting of the dc levels of the voltage at the gate of the input RF device and ensure their equality over PVT variation (Leung and Mok, 2001).

This chapter starts with review on design and evolution of low voltage operational amplifier, in Section 3.1. The design methodology and circuit implementation of the proposed bandgap reference and the integrated regulated

voltage reference circuit is subsequently reviewed in Section 3.2 and 3.3, respectively. The simulation results are discussed in Section 3.4.

3.1 CMOS Operational Amplifier

With lower supply voltage, the biasing of the amplifiers becomes more critical as a small variation of the bias point essentially cut the dynamic range, hence a mechanisms to precisely control bias points are of importance. In the case of a noise limited circuit, supply voltage headroom limitation results in a need for a high power dissipation design, in order to raise the signal above the noise floor (Razavi, 2001). Amplifiers are characterized by two aspects, the input range and the output range. In a feedback configuration the inputs get driven together to virtual ground, resulting in a fairly small input range. At the output, in a scenario of driving a subsequent stage of circuit at the amplifier's output, a certain range of dc biasing is required. Thus amplifiers are very much affected by the supply voltage scaling. Figure 3.1 illustrates the basic nMOS and pMOS based input differential pair used as an amplifier.

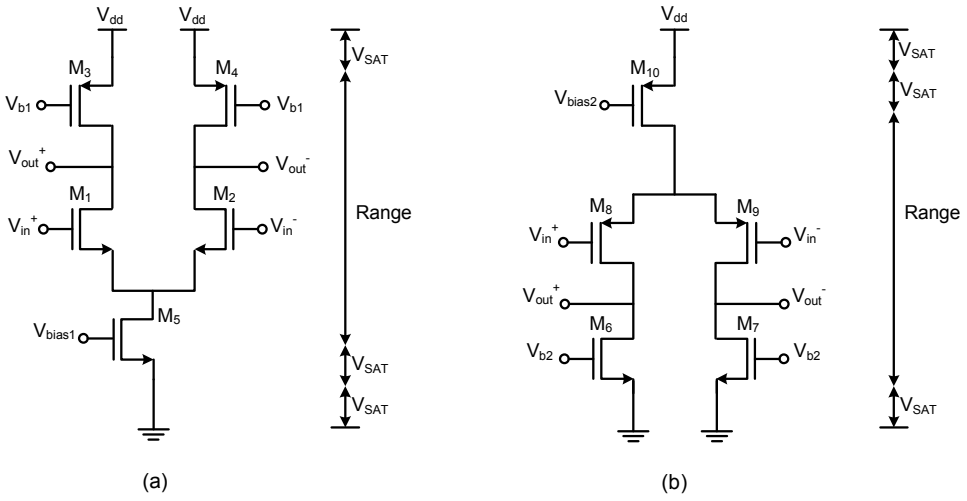


Figure 3.1: Differential pair amplifier with input transistor: (a) nMOS , (b) pMOS.

The nMOS tail current source in Figure 3.1(a) needs to be biased in saturation, thus $2V_{SAT}$ is needed by the differential pair and the tail current source, hence the