DESIGN AND DEVELOPMENT OF UNIPOLAR SPWM SWITCHING PULSES FOR SINGLE PHASE FULL BRIDGE INVERTER APPLICATION

BAHARUDDIN BIN ISMAIL

UNIVERSITI SAINS MALAYSIA

2008

DESIGN AND DEVELOPMENT OF UNIPOLAR SPWM SWITCHING PULSES FOR SINGLE PHASE FULL BRIDGE INVERTER APPLICATION

by

BAHARUDDIN BIN ISMAIL

Thesis submitted in fulfilment of the requirements
for the degree of
Master of Science

May 2008

ACKNOWLEDGEMENTS

First and foremost, " Syukur Alhamdulillah" to Allah, the Most Gracious and Most Merciful forensuring myself to be healthy to carry out my study and to complete this thesis. Secondly, I would like to take this opportunity to gratefully thank to Dr. Soib Bin Taib that has spent his precious time to give me the advice, guidance, discussion and direction on this project. Without his cooperation and substantiation for this project, it would have been impossible.

Last but not least, I wish to give my highest appreciation, gratitude and love to my wife Yusnita bt. Khalid, my children, Nurul Ain Maisarah, Nurul Nadia and Akmal Muhaimin , my parents; Ismail bin Saad and Tom bt Hashim, my sisters and my brothers for the support and motivation and for the encouragement, patience and prayers, which enable the project to be completed as required. I also would like to express heartfelt thanks to my friends at UniMAP and USM for their guidance and helped in completion of this project.

May God bless them all.

Wassalam

TABLE OF CONTENTS

Acknowledgements……....ii
Table of Contents……...iii
List of Tables……..vi
List of Figures……....vii
List of Symbols…….xiii
List of Abbreviations……xv
Abstrak……..xvi
Abstract……xvii

CHAPTER 1 - INTRODUCTION

1.0 Background……1
1.1 Problem Statement…….2
1.2 Objective of the project…….4
1.3 Methodology……..5
1.4 Thesis Outline……5

CHAPTER 2 - SINGLE PHASE INVERTER AND ITS SWITCHING SCHEME

2.0 Introduction…….7
2.1 Inverter……....7
2.2 Single Phase Inverter Topology……..9
2.2.1 Half Bridge Inverter……..9
2.2.2 Full Bridge Inverter……...10
2.3 Pulse Width Modulation (PWM) Scheme……11
2.3.1 Natural Sampling……...12
2.3.2 Regular Sampling PWM……...14
2.3.2.1 Symmetrical Sampling PWM……...15
2.3.2.2 Asymmetrical Sampling PWM…….16

2.4 PWM Switching Technique…….. 17
2.4.1 PWM with Bipolar Voltage Switching…… 18
2.4.2 PWM with Unipolar Voltage Switching…….. 19
2.5 Review of Previous Methods…….21
2.6 Summary……23

CHAPTER 3 - DESIGN OF SWITCHING PULSES FOR SINGLE PHASE INVERTER

3.0 Introduction……24
3.1 Inverter Switching Strategy and Its Operation……...24
3.2 Designing the SPWM Switching Pulses……27
3.3 The Gating Signals Technique……...28
3.3.1 Comparing the Reference Waveform and Triangular Waveform…….28
3.3.2 Volt-second Concept…….29
3.4 Calculated Value for Switching Pulses……..35
3.5 Summary……48

CHAPTER 4 - DEVELOPMENT SOFTWARE AND HARDWARE FOR PROTOTYPE SINGLE PHASE INVERTER

4.0 Introduction……49
4.1 AT89S52 Atmel Microcontroller……...49
4.2 Designing the SPWM Switching Pulses with Microcontroller……..50
4.3 Software Development……...51
4.3.1 Assembler……..54
4.3.2 ISP Programmer……....54
4.4 Hardware Development……..56
4.4.1 Switching Element…….....57
4.4.2 Gate Driver……57
4.4.3 Low-pass Filter……..59
4.4.4 Transformer……...60
4.5 Summary…….61

CHAPTER 5 - RESULT AND DISCUSSION

5.0 Introduction……..... 62

5.1 SPWM Output Waveform……... 62

5.2 Amplitude modulation ratio versus THD…….... 96

5.3 Inverter Performance Test……99

5.3.1 Voltage and Current Output Waveform……....100

5.3.2 Total Harmonic Distortion (THD)……....102

5.3.3 Inverter Efficiency Measuring……..104

5.3.4 Dead Time…….....106

5.4 Summary……....108

CHAPTER SIX - CONCLUSIONS

6.0 Conclusion…….109

6.1 The Research Contributions……..110

6.2 Future Work Enhancement……111

BIBLIOGRAPHY…….....112

APPENDICES

Appendix A- The Switching Pulses Angles for Triangular Waveform 1 kHz until 5 kHz

Appendix B- Software Programming for SPWM Switching Pulses Using AT89S52

LIST OF PUBLICATIONS

LIST OF TABLES

Page

Table 3.1	The switching period for triangular carrier waveform 1 kHz	**35**
Table 3.2	The switching period for triangular carrier waveform 2 kHz	**36**
Table 3.3	The switching period for triangular carrier waveform 3 kHz	**38**
Table 3.4	The switching period for triangular carrier waveform 4 kHz	**41**
Table 3.5	The switching period for triangular carrier waveform 5 kHz	**44**
Table 4.1	Specification of MOSFET IRFP 250	**57**
Table 4.2	Specification for transformer	**60**

LIST OF FIGURES

Page

Figure 1.1	The research methodology	**5**
Figure 2.1	Half bridge circuit topology and its output example	**10**
Figure 2.2	Full bridge circuit topology and its output example	**11**
Figure 2.3	The basic concept of natural sampling PWM	**12**
Figure 2.4	Natural sampling pulse width modulation (half cycle)	**13**
Figure 2.5	Symmetrical regular PWM	**16**
Figure 2.6	Asymmetrical regular PWM	**17**
Figure 2.7	Bipolar PWM generator	**18**
Figure 2.8	SPWM with Bipolar voltage switching a) comparison between reference waveform and triangular waveform b) Gating pulses for S1 and S4 c) Gating pulses for S2 and S3 d) Output waveform	**19**
Figure 2.9	Unipolar PWM generator	**20**
Figure 2.10	SPWM with Unipolar voltage switching a) comparison between reference waveform and triangular waveform b) Gating pulses for S1 and S4 c) Gating pulses for S2 and S3 d) Output waveform	**21**
Figure 3.1	Flowchart design of switching pulses	**24**
Figure 3.2	Single phase inverter and its control strategy	**25**
Figure 3.3	Steady state operation for positive half cycle	**26**
Figure 3.4	Steady state operation for negative half cycle	**26**
Figure 3.5	Unipolar output waveform	**26**
Figure 3.6	Technique for producing SPWM switching pulses	**27**
Figure 3.7	Concept of comparing reference waveform and triangular Waveform (half cycle)	**28**
Figure 3.8	Volt-second equation concept for pulse determine	**29**
Figure 3.9	Pulse width modulation with volt-second concept for k^{th} PWM pulse	**30**
Figure 4.1	Pin configurations for AT89S52 Atmel microcontroller	**50**
Figure 4.2	Steps to create a program	**52**

Figure 4.3	Flowchart of SPWM signal generation	**53**
Figure 4.4	Command prompt window	**54**
Figure 4.5	Main screen view of the ISP programmer	**55**
Figure 4.6	Configuration of prototype inverter	**56**
Figure 4.7	Gate driver circuit	**58**
Figure 4.8	LC low-pass filter	**59**
Figure 4.9	Prototype of the single phase inverter	**61**
Figure 5.1	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =1 kHz with m_a =0.1	**63**
Figure 5.2	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =1 kHz with m_a =0.1	**63**
Figure 5.3	Measured of the smallest pulse for $f_{carrier}$ =1 kHz with m_a =0.1	**64**
Figure 5.4	Measured of the biggest pulse for $f_{carrier}$ =1 kHz with m_a =0.1	**64**
Figure 5.5	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =1 kHz with m_a =0.5	**65**
Figure 5.6	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =1 kHz with m_a =0.5	**65**
Figure 5.7	Measured of the smallest pulse for $f_{carrier}$ =1 kHz with m_a =0.5	**66**
Figure 5.8	Measured of the biggest pulse for $f_{carrier}$ =1 kHz with m_a =0.5	**66**
Figure 5.9	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =1 kHz with m_a =1	**67**
Figure 5.10	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =1 kHz with m_a =1	**67**
Figure 5.11	Measured of the smallest pulse for $f_{carrier}$ =1 kHz with m_a =1	**68**
Figure 5.12	Measured of the biggest pulse for $f_{carrier}$ =1 kHz with m_a =1	**68**
Figure 5.13	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =2 kHz with m_a =0.1	**69**

Figure 5.14	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =2 kHz with m_a =0.1	**69**
Figure 5.15	Measured of the smallest pulse for $f_{carrier}$ =2 kHz with m_a =0.1	**70**
Figure 5.16	Measured of the biggest pulse for $f_{carrier}$ =2 kHz with m_a =0.1	**70**
Figure 5.17	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =2 kHz with m_a =0.5	**71**
Figure 5.18	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =2 kHz with m_a =0.5	**71**
Figure 5.19	Measured of the smallest pulse for $f_{carrier}$ =2 kHz with m_a =0.5	**72**
Figure 5.20	Measured of the biggest pulse for $f_{carrier}$ =2 kHz with m_a =0.5	**72**
Figure 5.21	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =2 kHz with m_a =1	**73**
Figure 5.22	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =2 kHz with m_a =1	**73**
Figure 5.23	Measured of the smallest pulse for $f_{carrier}$ =2 kHz with m_a =1	**74**
Figure 5.24	Measured of the biggest pulse for $f_{carrier}$ =2 kHz with m_a =1	**74**
Figure 5.25	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =3 kHz with m_a =0.1	**75**
Figure 5.26	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =3 kHz with m_a =0.1	**75**
Figure 5.27	Measured of the smallest pulse for $f_{carrier}$ =3 kHz with m_a =0.1	**76**
Figure 5.28	Measured of the biggest pulse for $f_{carrier}$ =3 kHz with m_a =0.1	**76**
Figure 5.29	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =3 kHz with m_a =0.5	**77**
Figure 5.30	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =3 kHz with m_a =0.5	**77**
Figure 5.31	Measured of the smallest pulse for $f_{carrier}$ =3 kHz with m_a =0.5	**78**
Figure 5.32	Measured of the biggest pulse for $f_{carrier}$ =3 kHz with m_a =0.5	**78**

Figure 5.33 Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =3 kHz with m_a =1 **79**

Figure 5.34 Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =3 kHz with m_a =1 **79**

Figure 5.35 Measured of the smallest pulse for $f_{carrier}$ =3 kHz with m_a =1 **80**

Figure 5.36 Measured of the biggest pulse for $f_{carrier}$ =3 kHz with m_a =1 **80**

Figure 5.37 Simulated waveform for SPWM 1 and SPWM 2 after gate driver For $f_{carrier}$ =4 kHz with m_a =0.1 **81**

Figure 5.38 Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =4 kHz with m_a =0.1 **81**

Figure 5.39 Measured of the smallest pulse for $f_{carrier}$ =4 kHz with m_a =0.1 **82**

Figure 5.40 Measured of the biggest pulse for $f_{carrier}$ =4 kHz with m_a =0.1 **82**

Figure 5.41 Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =4 kHz with m_a =0.5 **83**

Figure 5.42 Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =4 kHz with m_a =0.5 **83**

Figure 5.43 Measured of the smallest pulse for $f_{carrier}$ =4 kHz with m_a =0.5 **84**

Figure 5.44 Measured of the biggest pulse for $f_{carrier}$ =4 kHz with m_a =0.5 **84**

Figure 5.45 Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =4 kHz with m_a =1 **85**

Figure 5.46 Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =4 kHz with m_a =1 **85**

Figure 5.47 Measured of the smallest pulse for $f_{carrier}$ =4 kHz with m_a =1 **86**

Figure 5.48 Measured of the biggest pulse for $f_{carrier}$ =4 kHz with m_a =1 **86**

Figure 5.49 Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =5 kHz with m_a =0.1 **87**

Figure 5.50 Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =5 kHz with m_a =0.1 **87**

Figure 5.51 Measured of the smallest pulse for $f_{carrier}$ =5 kHz with m_a =0.1 **88**

Figure 5.52	Measured of the biggest pulse for $f_{carrier}$ =5 kHz with m_a =0.1	**88**
Figure 5.53	Simulated waveform for SPWM 1 and SPWM 2 after gate driver for $f_{carrier}$ =5 kHz with m_a =0.5	**89**
Figure 5.54	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =5 kHz with m_a =0.5	**89**
Figure 5.55	Measured of the smallest pulse for $f_{carrier}$ =5 kHz with m_a =0.5	**90**
Figure 5.56	Measured of the biggest pulse for $f_{carrier}$ =5 kHz with m_a =0.5	**90**
Figure 5.57	Simulated waveform for SPWM 1 and SPWM 2 after gate driver For $f_{carrier}$ =5 kHz with m_a =1	**91**
Figure 5.58	Experimental waveform for SPWM 1 and SPWM 2 for $f_{carrier}$ =5 kHz with m_a =1	**91**
Figure 5.59	Measured of the smallest pulse for $f_{carrier}$ =5 kHz with m_a =1	**92**
Figure 5.60	Measured of the biggest pulse for $f_{carrier}$ =5 kHz with m_a =1	**92**
Figure 5.61	The summarize of the calculated and measured for the smallest and biggest pulse for $f_{carrier}$ 1 kHz	**93**
Figure 5.62	The summarize of the calculated and measured for the smallest and biggest pulse for $f_{carrier}$ 2 kHz	**94**
Figure 5.63	The summarize of the calculated and measured for the smallest and biggest pulse for $f_{carrier}$ 3 kHz	**94**
Figure 5.64	The summarize of the calculated and measured for the smallest and biggest pulse for $f_{carrier}$ 4 kHz	**95**
Figure 5.65	The summarize of the calculated and measured for the smallest and biggest pulse for $f_{carrier}$ 5 kHz	**95**
Figure 5.66	Circuit without filter	**96**
Figure 5.67	Circuit with filter	**96**
Figure 5.68	Amplitude modulation ratio versus total harmonic distortion (without filter)	**98**
Figure 5.69	Amplitude modulation ratio versus total harmonic distortion (with filter)	**98**
Figure 5.70	Amplitude modulation ratio versus dead time period	**99**

Figure 5.71	Overall test setup hardware for single phase full bridge inverter	**100**
Figure 5.72	Simulated and experimental result for voltage and current output Without filter before transformer with R=200Ω loads	**101**
Figure 5.73	Simulated and experimental result for voltage and current output after filter and transformer with 300W load	**102**
Figure 5.74	The output power versus percentage THD	**103**
Figure 5.75	Harmonic spectrum for voltage and current output when prototype work at 300W	**104**
Figure 5.76	Circuit for measuring the efficiency of the prototype	**105**
Figure 5.77	The efficiency of the prototype versus output power	**106**
Figure 5.78	Dead time period measurement	**107**
Figure 5.79	Percentage dead time increment versus THD	**108**

LIST OF SYMBOLS

		Page
T	Period	**9**
S1	Switch 1	**10**
S2	Switch 2	**10**
V_{dc}	DC voltage	**10**
S3	Switch 3	**10**
S4	Switch 4	**10**
V_r	Amplitude voltage reference	**13**
V_c	Amplitude voltage carrier	**13**
mf	Frequency modulation ratio	**13**
$f_{carrier}$	Triangular carrier waveform frequency	**13**
$f_{reference}$	Fundamental waveform frequency	**13**
m_a	Amplitude modulation ratio	**14**
$t\omega_k$	Pulse width for k sampling time	**16**
$-V_r$	Inverse amplitude voltage reference	**19**
gS1	Gating signal for switch 1	**27**
gS2	Gating signal for switch 2	**27**
gS3	Gating signal for switch 3	**27**
gS4	Gating signal for switch 4	**27**
t_{on}	Time on	**28**
t_{off}	Time off	**28**
A_{s1}	Left side volt-second area	**29**
A_{s2}	Right side volt-second area	**29**
$\overline{V_k}$	Average voltage for k^{th} PWM left side	**31**

$\overline{V_{k+1}}$	Average voltage for k^{th} PWM right side	**31**
δ_k	Pulse area for left side	**31**
δ_{k+1}	Pulse area for right side	**31**
β_k	Parameter that control the average voltage for left side	**31**
β_{k+1}	Parameter that control the average voltage for right side	**31**
δ_0	Half period PWM pulse for left and right side	**31**
V_m	Amplitude voltage	**31**
α_n	Angle for carrier frequency	**31**
α_k	Instant switching angle left side	**33**
α_{k+1}	Instant switching angle right side	**33**
I	Input current	**57**

LIST OF ABBREVIATIONS

Page

AC	Alternating Current	**1**
DC	Direct Current	**1**
BJT	Bipolar Junction Transistor	**1**
MOSFET	Metal Oxide Semiconductor Field Effect Transistor	**1**
SPWM	Sinusoidal Pulse Width Modulation	**2**
SIMCAD	Simulation of computer aided design	**4**
PWM	Pulse width modulation	**5**
kHz	kilo hertz	**6**
VSI	Voltage source inverter	**7**
CSI	Current source inverter	**7**
IGBT	Insulated gate bipolar junction transistor	**8**
THD	Total harmonic distortion	**8**
DSP	Digital Signal Processing	**49**
FPGA	Field Programmable Gate Array	**111**

REKABENTUK DAN PEMBANGUNAN DENYUT PENSUISAN SPWM UNIPOLAR UNTUK KEGUNAAN PENYONGSANG SATU FASA TETIMBANG PENUH

ABSTRAK

Tesis ini menerangkan rekabentuk dan pembangunan denyut pensuisan SPWM unipolar yang dibangunkan secara kaedah digital untuk penyongsang satu fasa tetimbang penuh. Satu strategi kawalan pensuisan diusulkan untuk digunakan pada penyongsang satu fasa. Kelebihan utama strategi kawalan pensuisan ini adalah ia tidak memerlukan litar tambahan untuk penjanaan masa mati (dead time) bagi suis penyongsang. Melalui teknik tersebut, satu persamaan untuk menentukan sudut denyut PWM diterbitkan dan kiraan sudut denyut pensuisan dilakukan. Denyut pensuisan dengan frekuensi gelombang pembawa 1 kHz hingga 5 kHz dengan nisbah pemodulatan amplitud antara 0.1 hingga 1 dikira berdasarkan persamaan yang diterbitkan. Mikropengawal jenis Atmel AT89S52 digunakan untuk menjana denyut pensuisan tersebut. Penyongsang satu fasa tetimbang penuh berkadaran 300W dibina untuk menguji keberkesanan denyut pensuisan yang dijana melalui mikropengawal. Pengukuran bagi denyut yang terkecil dan terbesar bagi setiap frekuensi pembawa diukur bagi memastikan ia mengikut nilai kiraan. Melalui ujikaji, didapati bahawa denyut pensuisan dengan gelombang pembawa berfrekuensi 5 kHz dengan nisbah pemodulatan amplitud 1 mempunyai profil jumlah herotan harmonik yang rendah iaitu 2.3% dan masa mati yang lebih baik berbanding dengan denyut pensuisan yang lain. Denyut pensuisan tersebut digunakan untuk menguji prestasi penyongsang satu fasa tetimbang penuh yang dibina. Keputusan ekperimen menunjukkan bahawa jumlah herotan harmonik (THD) bagi gelombang arus keluaran adalah kurang daripada 3% dan kecekapan penyongsang pula adalah sekitar 89% pada beban rintangan 300W. Pengujian kesan masa mati terhadap jumlah herotan harmonik juga dilakukan dan didapati bahawa jumlah herotan harmonik masih lagi di paras 3% walaupun tempoh masa mati ditingkatkan sebanyak seratus peratus.

DESIGN AND DEVELOPMENT OF UNIPOLAR SPWM SWITCHING PULSES FOR SINGLE PHASE FULL BRIDGE INVERTER APPLICATION

ABSTRACT

In this thesis, a design and development of unipolar SPWM switching pulses with digital technique for single phase full bridge inverter is presented. A switching strategy was proposed to be used for full bridge single phase inverter. The main advantage of this strategy is that it does not required additional circuit to generated inverter's dead time. In this technique, the PWM equation was develop and the switching pulse was calculated. The PWM switching pulses with carrier frequency range from 1 kHz to 5 kHz and the amplitude modulation ratio range from 0.1 until 1 were calculated based on the equations derived. The AT89S52 Atmel microcontroller was used to program the switching pulses. The single phase full bridge inverter rated 300W has been developed in order to test the switching pulses generated by microcontroller. The measurement of the smallest and biggest pulse for each carrier frequency has been done in order to make sure the pulses follow the calculated value. Based on the experiment, the switching pulse with carrier frequency of 5 kHz and amplitude modulation ratio of 1 produced THD value of 2.3% and better dead time period. This switching pulse is used to test the single phase full bridge inverter performance. The result shows that the THD of the output current is less than 3% and the efficiency was found to be 89% for 300W pure resistive load. The effect of dead time was also tested and the THD was found to be less than 3% even though the dead time period is increased by 100%.

CHAPTER 1
INTRODUCTION

1.0 Background

The application of semiconductor devices in electric power field has been steadily increasing with the passage of time. Power semiconductor devices constitute the heart of the modern power electronics, and are being extensively used in power electronic converters in the form of a matrix of on or off switches, and help to convert power from one form to another. There are four basic conversion functions that normally can be implemented such as AC to AC, AC to DC, DC to AC and DC to DC.

Inverter is one of the converter families which are called DC to AC converter. It converts DC power to AC power to a symmetric AC output voltage at desired magnitude and frequency (Ahmed, 1999). Inverter is widely used in industrial applications such as variable speed AC motor drives, induction heating, standby power supplies and uninterruptible power supplies. The DC power input of inverter is obtained from the existing power supply network. It can be a battery, photovoltaic, wind energy, fuel cell or other DC sources.

One of the switching mode power conversion is inverter had been discussed and new techniques of switching strategies was implemented in circuit designed. All switching strategies mostly concentrate in term of reducing the power losses, reduce the total harmonic distortion and increasing the efficiencies of the inverter. For the purpose, many researchers have been studying and analyzing types of switches that can be used in inverter. The power semiconductor devices such as the diode, thyristor, triac and power transistor are widely used in power applications as switching devices (Cyril, 1993). Two types of power transistors used for switching devices are Bipolar Junction Transistor (BJT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Both

of power transistors have a different characteristic where, MOSFET have faster switching speed and BJT have higher capability (Hua , 1995). The important criteria of power transistors in circuit applications also depend on the parameters of rating, conduction losses, switching losses, switching times, control strategy and finally are cost (Cyril, 1993).

SPWM or sinusoidal pulse width modulation is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the on and off of the power switches (Ismail , 2006a). The pulse width modulation inverter has been the main choice in power electronic for decades, because of its circuit simplicity and rugged control scheme (Bellar et al., 1998). SPWM switching technique is commonly used in industrial applications (Ismail , 2006b) (Rashid, 2004). SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of this pulses are modulated in order to obtain inverter output voltage control and to reduce its harmonic content. Sinusoidal pulse width modulation or SPWM is the most common method in motor control and inverter application. Conventionally, to generate the signal, triangle wave as a carrier signal is compared with the sinusoidal wave, whose frequency is the desired frequency.

The proposed method used in this design is to replace the conventional method with the use of Atmel microcontroller. The use of the microcontroller brings flexibility to change the real-time control algorithms without further changes in hardware. It will reduce the overall cost and has a small size of control circuit for the single phase full bridge inverter.

1.1 Problem Statement

Inverter is one of power conversion device that widely used in the world to convert DC input voltage to AC output voltage. The output voltage waveforms of ideal inverters should be

sinusoidal. However, the waveform of practical inverter is non-sinusoidal and contains harmonics. Then, for this project, it should get closer sinusoidal waveform within +- 5% harmonics contains. Harmonic contents in inverter output depends more to number of pulses per cycle. As an example, square wave switching method will produce more harmonic contents in inverter output compared to pulse width modulation switching technique. This is due to number of pulses per cycle of pulse width modulation can be modified on the frequency of triangular carrier waveform. The frequency of triangular waveform can be modified from lower frequency to higher frequency. If higher frequency is used, the number of pulses per cycle also increased and at the same time it will reduce the harmonic contents of the inverter.

In switching losses problem, the number of pulses per cycle also affected. The use of high switching technique will contribute to the high power losses and it also needs to take care on the inverter switching design. The following factors are to be considered in order to meet the requirement.

i. Cost of equipment
ii. Size of filter
iii. Total harmonic distortion
iv. Power loss in switching elements

In order to fulfill the requirement, the new switching technique had been analyzed and recommended in this thesis, namely SPWM which is generated by Atmel microcontroller. The various frequency triangular carriers with different amplitude modulation ratio SPWM signal had been programmed and tested in single phase inverter circuit in order to find the best switching signal.

1.2 Objective of the project

The aim of this research is mainly to design and develop the SPWM switching pulse for single phase full bridge inverter application. The main objectives of this research can be summarized as:

i. To design and implement switching strategy for inverter application, which are simple, reliable, low cost and high efficiency

ii. To use the power electronics simulation software, SIMCAD or PeSIM version 4.1 to simulate the designed circuits with variety switching conditions to obtain optimum performance

iii. To develop Sinusoidal Pulse Width Modulation switching pulses with Unipolar Voltage Switching using Atmel microcontroller.

iv. To develop a complete prototype of inverter with 300W power rating for photovoltaic application

v. To compare and analyze the simulated results and the prototype inverter unit.

1.3 Methodology

The flowchart as shown in Figure 1.1 indicates the methodology process used in this research which consist of five main stages.

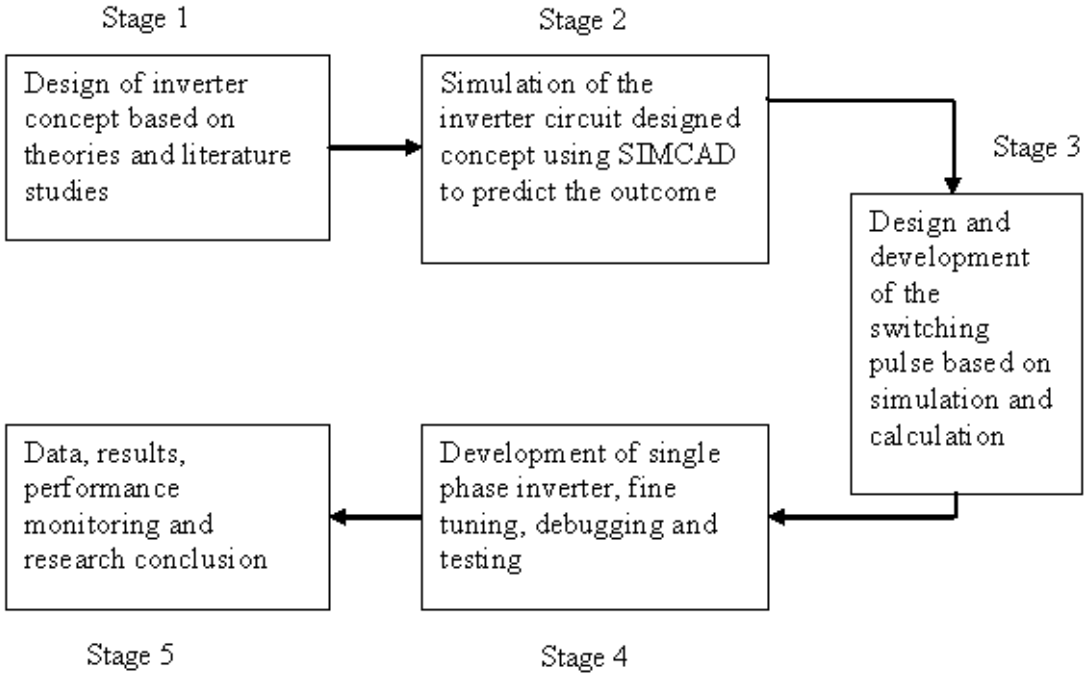

Figure 1.1: The research methodology

1.4 Thesis Outline

This thesis consists of six chapters, including this chapter and appendices.

Chapter 1 introduces the background of the research, problem statement, objective of the project, methodology and the overall thesis outline.

Chapter 2 discusses on the operation of a single phase inverter, pulse width modulation (PWM) scheme including natural sampling, regular symmetrical, asymmetrical sampling and PWM switching scheme including bipolar voltage switching and unipolar voltage switching scheme. In this chapter also, review of the previous methods for single phase inverter will discuss.

Chapter 3 it will discuss on the design of switching pulses for single phase inverter, including inverter switching strategy and its operation, designing the SPWM switching pulses for digital technique implementation and results of the calculated pulse for carrier frequency from 1 kHz to 5 kHz with amplitude modulation ratio from 0.1 to 1.

Chapter 4 will discuss on the design software and hardware for prototype single phase inverter. It is involved software and hardware development. The flow of the software development for switching pulses is given detail in this chapter. It is including AT89S52 Atmel microcontroller, designing the switching pulses with microcontroller, software development, assembler and ISP programmer. In this chapter also, hardware development prototype for single phase inverter is clearly described. It is including switching element, gate driver, low-pass filter and transformer.

In Chapter 5 experimental and simulation results are compared to verify the usefulness of the switching pulses and single phase inverter. Finally, conclusion and a suggestion will be presented in Chapter 6.

CHAPTER 2
SINGLE PHASE INVERTER AND ITS SWITCHING SCHEME

2.0 Introduction

In this chapter, types of inverter, inverter topology and its operation will be reviewed. The concept of Pulse Width Modulation (PWM) technique on single phase inverter is described and it covered different types of PWM strategies which were applied in inverter circuit.

2.1 Inverter

Inverters can be found in a variety of forms, including half bridge or full bridge, single phase or three phase, current source (CSI) or voltage source (VSI) and two-level or multilevel. The single phase voltage-source inverters can be further divided into three general categories, pulse width modulation type, square wave type (also known as six step inverters) and single phase inverters with voltage cancellation.

In pulse width modulated (PWM) inverters, the input DC voltage is essentially constant in magnitude and the AC output voltage has controlled magnitude and frequency. Therefore the inverter must control the magnitude and the frequency of the output voltage. This is achieved by PWM of the inverter switches and hence such inverters are called PWM inverters.

For square-wave inverters, the input DC voltage is controlled in order to adjust the magnitude of the output AC voltage. Therefore the inverter has to control only the frequency of the output voltage. The output AC voltage has a waveform similar to a square-wave.

In single phase inverter with voltage cancellation, it is possible to control the magnitude and the frequency of the inverter output voltage with a constant DC input voltage for a different switch

mode that is not pulse width modulated. The inverter output voltage waveform is similar to square wave. This technique works only with single-phase inverters.

As mentioned earlier, all inverters can be operated by controlled turn-on and turn-off semiconductor devices such as BJT, MOSFET, IGBT and others. Modern inverters used IGBT as the main power control devices (Mohan, 2003) but MOSFET is also used especially for lower voltage, power ratings and application that required high efficiency and high switching frequency.

The output voltage waveform of ideal inverters should be sinusoidal but in reality, the waveforms of inverters are non sinusoidal and contain certain harmonics. The typical definition for a harmonic is a sinusoidal voltage and currents at frequencies that are integer multiples of the main generated (or fundamental) frequency (Arrillaga, 2003). Harmonic distortion levels can be characterized by the complete harmonic spectrum with magnitudes and phase angles of each individual harmonic component (Lee, 1999). It is also common to use a single quantity that is known as Total Harmonic Distortion (THD) (Sankaran, 2001). It is measure of the magnitude of harmonic distortion. For current, the distortion values must be referred to a constant base (e.g the rated load current or demand current) rather than the fundamental component. This provides a constant reference while the fundamental can vary over a wide range. The problem of the harmonics in low voltage distribution systems is considered important. Harmonics now represent a major design consideration in power electronic applications.

In (Rashid, 2004), the harmonics contents in output voltage of inverter can be minimized significantly by switching techniques. Nowadays the best switching technique is still under investigation but pulse-width modulated (PWM) is chosen as a switching technique purposely to reduce the harmonics in inverter output.

2.2 Single Phase Inverter Topology

There are two circuit topologies commonly used in single phase inverter circuit. Half bridge and full bridge configuration are the main topologies used in low and high power applications. For certain low power application, the half bridge may suffice but the full bridge is more convenient for adjustment of the output voltage by pulse width modulation techniques (Mohan, 2003).

2.2.1 Half Bridge Inverter

The power circuit topology and output example for half bridge inverter is shown in Figure 2.1. The inverter circuit consists of two controlled static switching elements. The switching elements can be transistor, MOSFET, IGBT and extra. The switching elements are labeled S1 and S2 and each of switches has an anti-parallel diode. It is evident from the presence of the diodes that the switching devices S1 and S2 need not have the capability to block the reverse voltages. If the switching element is power MOSFET, there may not be a need to use the anti-parallel diodes because the devices structure has an anti-parallel diode (Joseph, 1995).

The basis operation of half bridge inverter can be divided into two operations. If switch S1 turned on for period of $\frac{T}{2}$, the instantaneous output voltage across the load equal to $\frac{V_{dc}}{2}$. If switch S2 turned on for period of $\frac{T}{2}$ to T, the instantaneous output voltage $\frac{-V_{dc}}{2}$ will appear (Rashid, 2004). The switching strategy for switch S1 and switch S2 must be designed to make sure both switches not turn on at the same time. If that happens, it is equivalent to a short circuit across the DC input, resulting in excessive current and possible damage to the switching elements (Joseph, 1995).

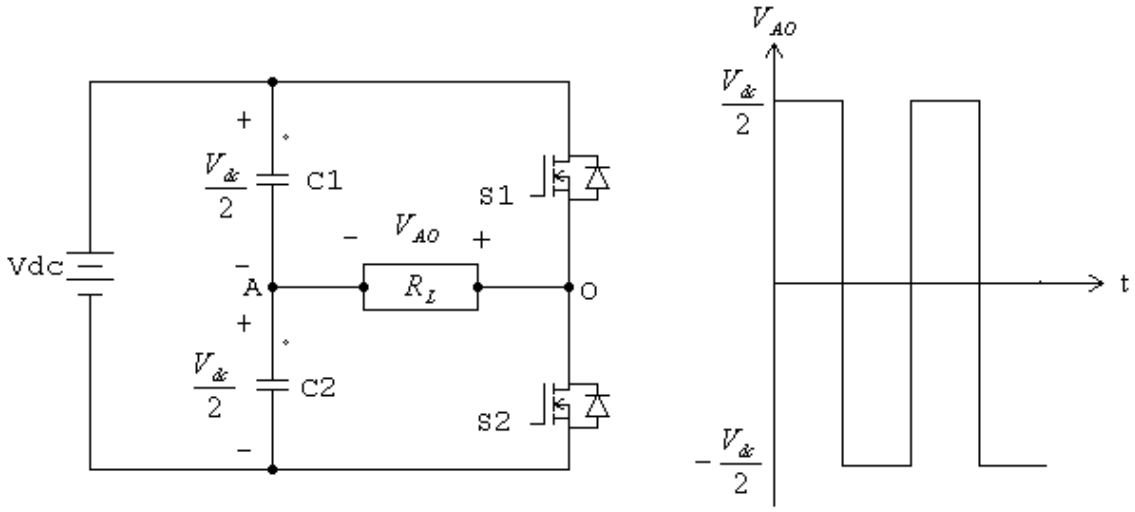

Figure 2.1: Half bridge circuit topology and its output example

2.2.2 Full Bridge Inverter

A single phase full bridge inverter circuit and its output example are shown in Figure 2.2. It consists of four switching elements and it is used in higher power ratings application. The four switches are labeled as S1, S2, S3 and S4. The operations of single phase full bridge inverter can be divided into two conditions. Normally the switches S1 and S4 are turned on and kept on for one half period and S2 and S3 are turned off. At this condition, the output voltage across the load is equal to V_{dc}. When S2 and S3 are turned on, the switches S1 and switches S4 are turned off, then at this time the output voltage is equal to $-V_{dc}$. The output voltage will change alternately from positive half period and negative half period. Same like in half bridge inverter, to prevent short circuit across DC supply occurred, the switches S1 and S4 must be in 'on' state while S2 and S3 must be in 'off' state. In order to prevent short circuit occurred, dead time mechanism has been used in gate driver circuit (David , 1997).

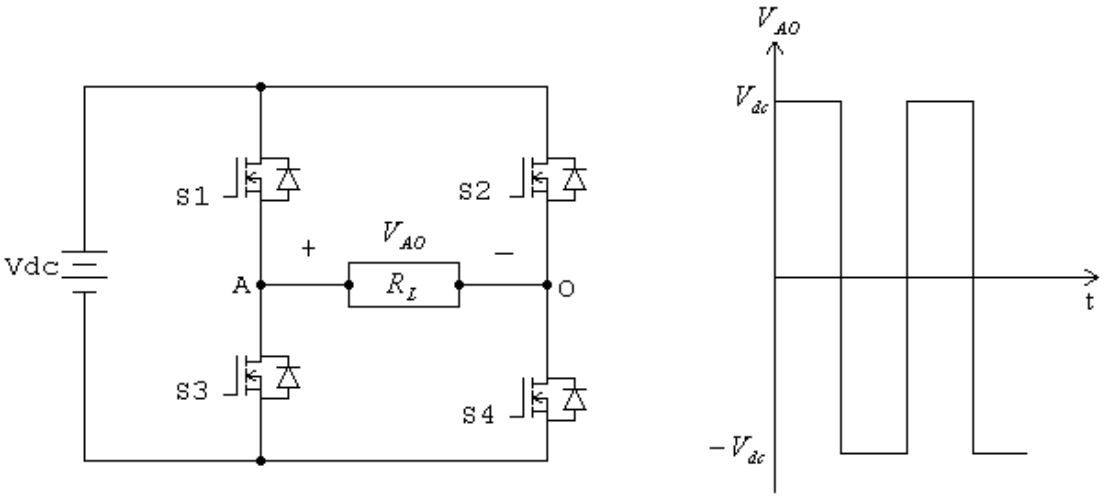

Figure 2.2: Full bridge inverter topology and its output example

2.3 Pulse Width Modulation (PWM) Scheme

Historically, pulse width modulation (PWM) switching strategy development has been largely prompted by the changes in technology that have occurred over the past 30 years. It started with the natural-sampled PWM analogue technique (Mekhlief, 1999) in early 60s, followed by the regular-sampled PWM digital techniques (Holtz, 1992) in the early 70s, through to the microprocessor-based harmonic elimination and optimized PWM techniques in the mid and late 70s and more recently the new optimal PWM strategies in the 1980s (Luo, 1996) (Holtz, 1994). It has been shown that since natural-sampled PWM techniques are essentially analogue, these are inappropriate for discrete digital hardware or microprocessor software implementation. The heart of any PWM converter scheme is undoubtedly the switching strategy used to generate the switching edges of PWM control waveform (DaSilva , 1992) (Mekhlief , 2000).

The reason for using PWM techniques is that they provide voltage and current wave shaping customized to the specific needs of the applications under consideration (Escalante, 1995). By using PWM techniques, the frequency spectra of input waveforms can be changed such that the major non-fundamental components are at relatively high frequency and also to reduce the

switching stress imposed on the power switching devices (Zmood,1998). Most PWM is generated by comparing a reference waveform with a triangular carrier waveform signal (Pekik , 1995) (Ismail , 2007). However, the reference waveform may come in various shapes to suit the converter topology, such as sine wave and distorted sine wave. A sinusoidal waveform signal is used for PWM in DC to AC converter where it is used to shape the output AC voltage to be close to a sine wave.

2.3.1 Natural Sampling

The principle of natural sampling PWM is based on the comparison real time of sine wave waveform (reference waveform) with a triangular carrier waveform. Figure 2.3 shows the basic concept comparison between reference waveform and carrier waveform and Figure 2.4 shows natural sampling pulse width modulation. A high frequency triangular carrier waveform V_c is compared with a sinusoidal reference waveform V_r of the desired frequency. The PWM signal is high when the magnitude of sinusoidal wave is higher than the triangular wave otherwise it is low.

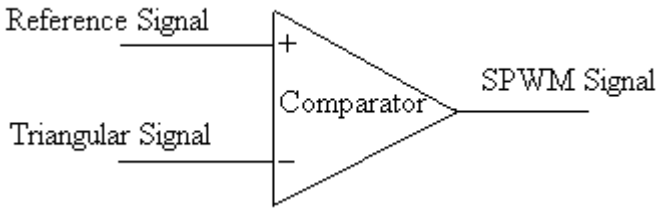

Figure 2.3: The basic concept of natural sampling PWM

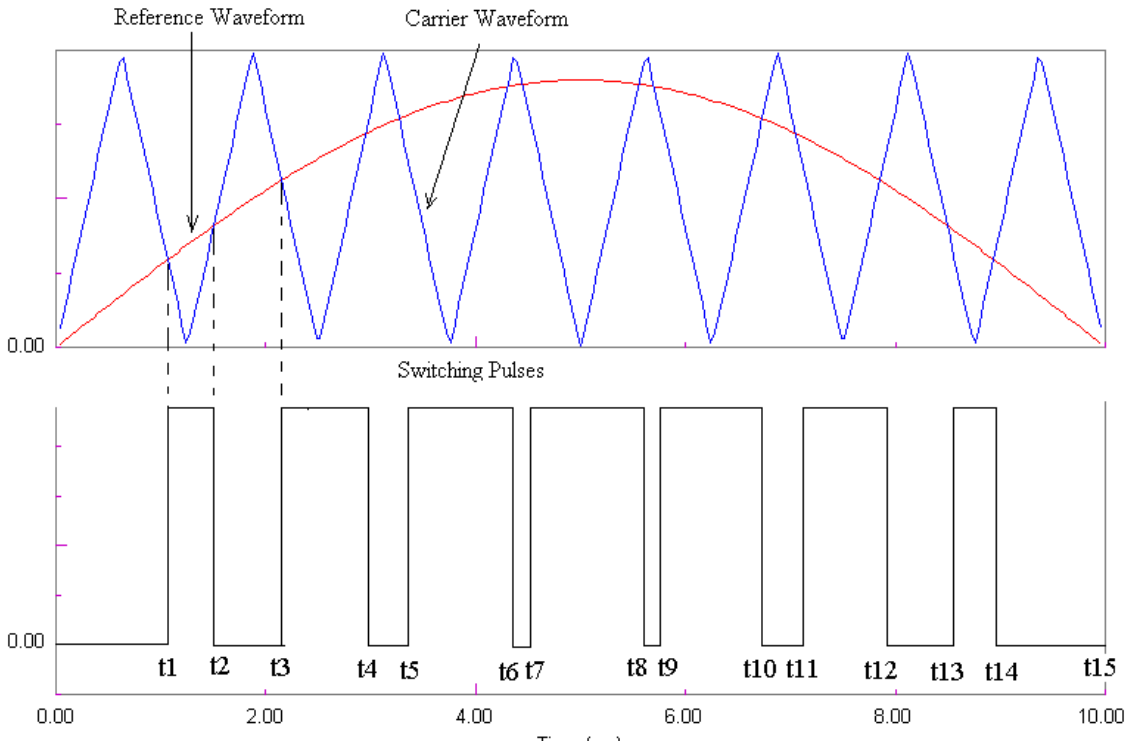

Figure 2.4: Natural sampling pulse width modulation (half cycle)

The reference signal V_r is used to modulate the switch duty ratio and has a frequency $f_{reference}$, which is the desired fundamental frequency of the inverter voltage output. Meanwhile the triangular carrier waveform V_c is at a switching frequency $f_{carrier}$ which establishes the frequency with which the inverters are switched. The frequency modulation ratio *mf* is defined as the ratio of the frequencies of the triangular carrier waveform and the reference signals which is written as

$$mf = \frac{f_{carrier}}{f_{reference}} = \frac{f_{tri}}{f_{\sin}} \tag{2.1}$$

Where;

$f_{carrier} = f_{tri}$ =Triangular carrier waveform frequency

$f_{reference} = f_{\sin}$ = Fundamental waveform frequency

The amplitude modulation ratio m_a is defined as the ratio of the amplitude of the reference and carrier signals and is given by

$$m_a = \frac{V_{m,\,reference}}{V_{m,\,carrier}} = \frac{V_{m,\,\sin}}{V_{m,\,carrier}} \tag{2.2}$$

Where;

$V_{m,reference} = V_{m,\sin}$ = Peak amplitude of reference waveform

$V_{m,carrier}$ = Peak amplitude of triangular carrier waveform

The amplitude of the PWM of the fundamental frequency output is controlled by m_a . This is significant for an unregulated DC voltage because the value of m_a can be adjusted to compensate the variations in the DC voltage, thus producing a constant amplitude output. When m_a is greater than 1 or over modulation, the amplitude of the output increases with m_a , but not linear.

2.3.2 Regular sampling PWM

One major limitation with natural sampling PWM is the difficulty of its implementation in a digital modulation system, because the intersection between the reference waveform and the triangular waveform is defined by a transcendental equation and is complex to calculate. An analogue circuit possesses the advantages of a low cost with a fast dynamic response, but suffers from a complex circuitry to generate complex PWM, limited function ability and difficulty to perform in circuit modifications (Mekhlief , 1999). To overcome this limitation the modern popular alternative is to implement the modulation system using a regular sampling PWM strategy. This technique was introduced to provide a more flexible way of designing the system. The system offers simple circuitry, software control and flexibility in adaptation to various applications. The two most

common regular sampling techniques are regular symmetrical and asymmetrical sampling (Ledwich, 1991).

2.3.2.1 Symmetrical sampling PWM

In regular sampling technique, the reference waveform is sampled at regularly spaced intervals. Normally, the sampling take places at the triangular waveform peaks. With one sample per carrier cycle the output is a double edge modulated waveform, which is symmetrical with respect to the centre point between the two consecutive samples. The modulation process is termed symmetrical modulation because the intersection of adjacent sides of the triangular carrier waveform with the stepped sine wave, about the non-sampled carrier peak, is equidistant about the carrier peak. Figure 2.5 illustrating the general features of symmetrical sampling PWM.

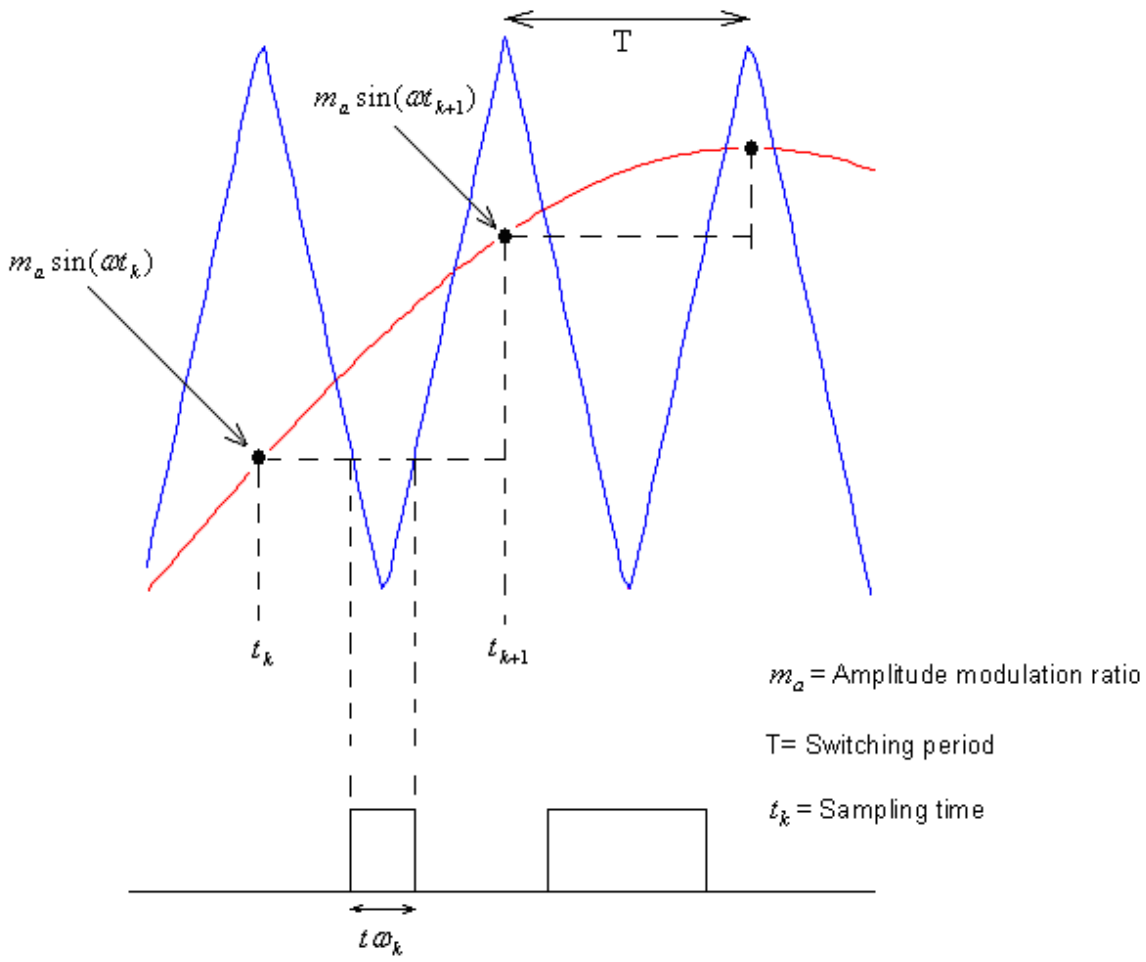

Figure 2.5 : Symmetrical regular PWM

2.3.2.2 Asymmetrical Sampling PWM

The asymmetrical modulation is produced when the triangular carrier waveform is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency. Each side of the triangular carrier waveform about a sampling point, intersect the stepped waveform at different step level (DaSilva , 1992). The resultant pulse width is asymmetrical about the sampling point as illustrate in Figure 2.6 . By using this technique the dynamic response can be improve and produces less harmonic distortion of the load current.

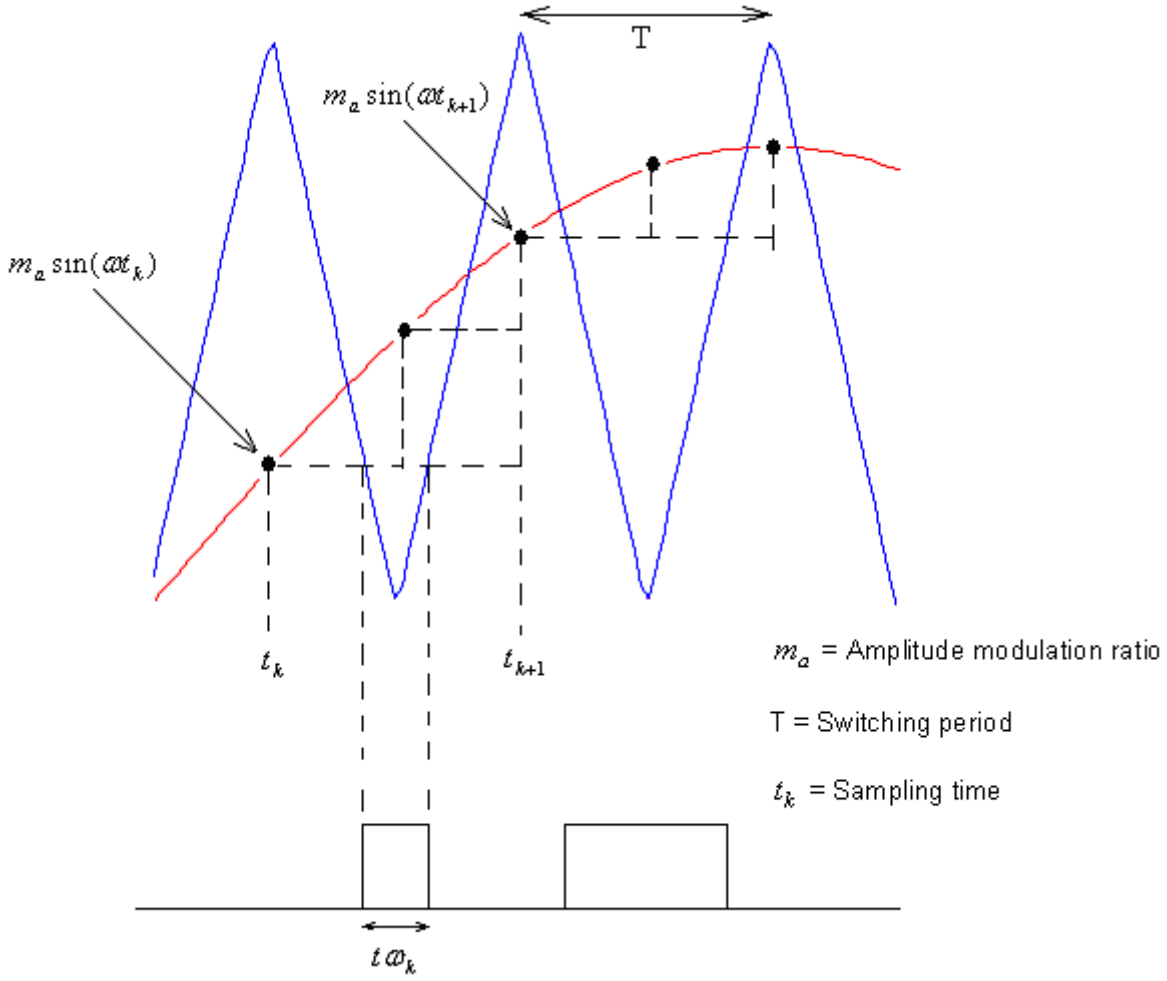

Figure 2.6: Asymmetrical regular PWM

2.4 PWM Switching Technique

The PWM switching can be divided into two switching scheme which are PWM with Bipolar voltage switching and PWM with Unipolar voltage switching (Mohan, 2003) (Daniel , 1997) (David , 1997).

2.4.1 PWM with Bipolar Voltage Switching

The basic idea to produce PWM Bipolar voltage switching signal is shown in Figure 2.7. It comprises of a comparator used to compare between the reference voltage waveform V_r with the triangular carrier signal V_c and produces the bipolar switching signal. If this scheme is applied to the full bridge single phase inverter as shown in Figure 2.2, all the switch S1, S2, S3 and S4 are turned on and off at the same time. The output of leg A is equal and opposite to the output of leg B. The output voltage is determined by comparing the reference signal, V_r and the triangular carrier signal, V_c.

Comparison between these two signals and the resulting output waveform are clearly illustrated in Figure 2.8.

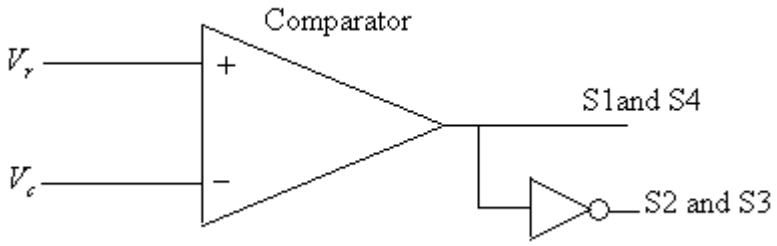

Figure 2.7: Bipolar PWM generator

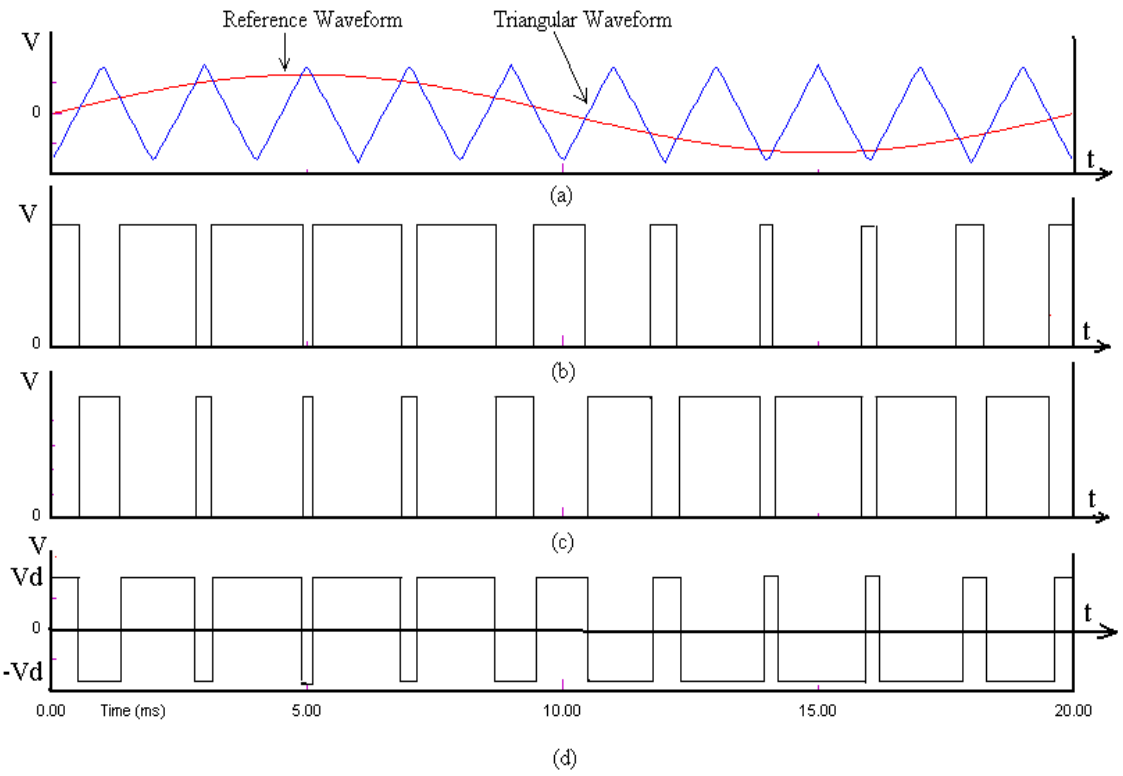

Figure 2.8: SPWM with Bipolar voltage switching (a) Comparison between reference waveform and triangular waveform (b) Gating pulses for S1 and S4 (c) Gating pulses for S2 and S3 (d) Output waveform

2.4.2 PWM with Unipolar Voltage Switching

In this scheme, the triangular carrier waveform is compared with two reference signals which are positive and negative signal. The basic idea to produce SPWM with Unipolar voltage switching is shown in Figure 2.9. The different between the Bipolar SPWM generators is that the generator uses another comparator to compare between the inverse reference waveform $-V_r$. The process of comparing these two signals to produce the Unipolar voltage switching signal is graphically illustrated in Figure 2.10. In Unipolar voltage switching the output voltage switches between 0 and V_{dc}, or between 0 and $-V_{dc}$. This is in contrast to the Bipolar switching strategy in which the output swings between V_{dc} and $-V_{dc}$. As a result, the change in output voltage at each

switching event is halved in the Unipolar case from 2Vdc to Vdc. The effective switching frequency is seen by the load is doubled and the voltage pulse amplitude is halved. Due to this, the harmonic content of the output voltage waveform is reduced compared to Bipolar switching. In Unipolar voltage switching scheme also, the amplitude of the significant harmonics and its sidebands is much lower for all modulation indexes thus making filtering easier, and with its size being significantly smaller (David , 1997).

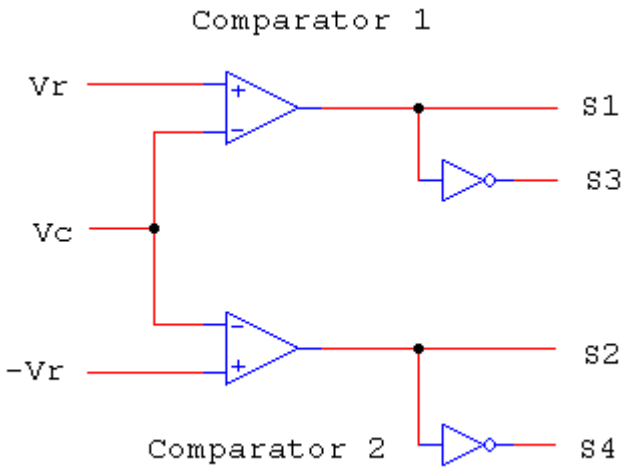

Figure 2.9: Unipolar PWM generator

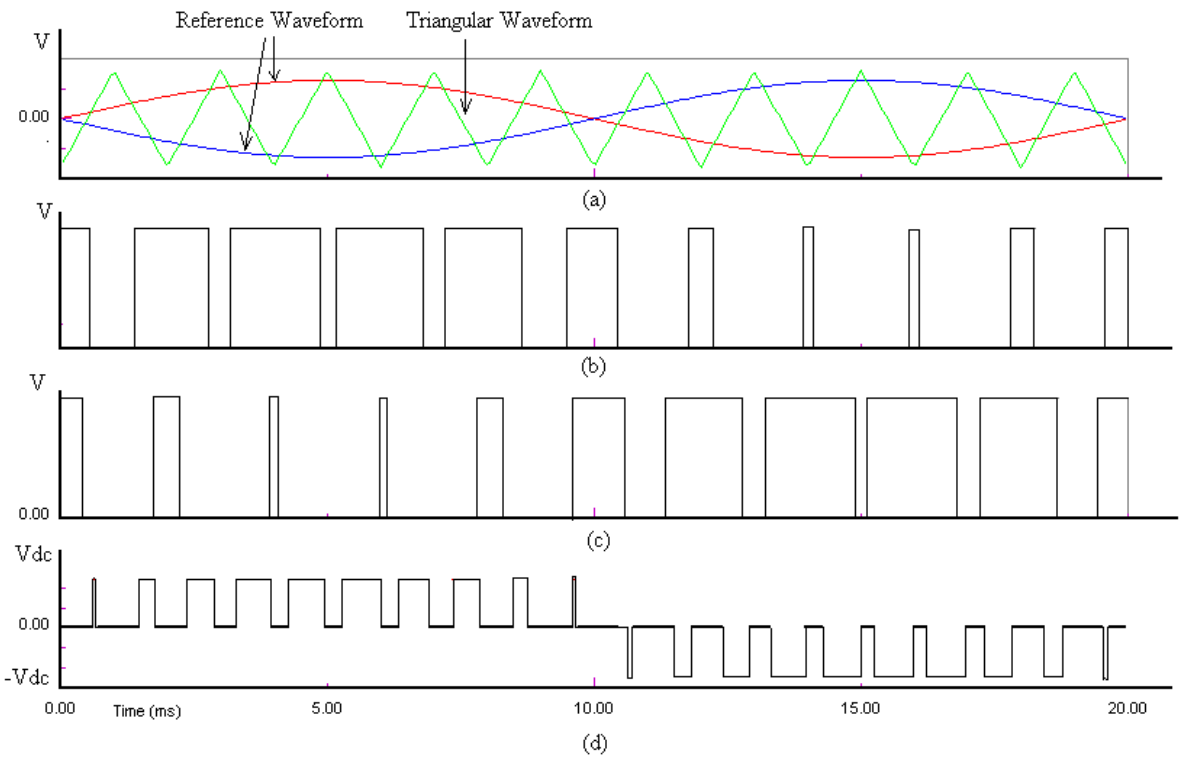

Figure 2.10: SPWM with Unipolar voltage switching (a) Comparison between reference waveform and triangular waveform (b) Gating pulses for S1 and S4 (c) Gating pulses for S2 and S3 (d) Output waveform

2.5 Review of Previous Methods

The developments of a single phase inverter growth year by year as the technologies keep changing rapidly. All electronic devices is smaller, therefore the efficiency of power supply used in electronic devices should be improved from time to time. Most of the researcher especially those are experts in single phase inverter have studied and analyzed the performance of parameter like harmonic, power losses and efficiencies of the single phase inverter. The different switching techniques and switching elements were used in single phase inverter also considered when inverters become the best power supply for converting DC power to AC power. Based on studied, PWM techniques is a common method used in single phase inverter circuit.

Taniguchi (1988) in his paper describe PWM technique for power MOSFET inverter. PWM method can move unwanted frequency components to a higher frequency region, i.e., the sidebands of a carrier frequency. Thus the output waveform of a PWM inverter is generally improves by using a high ratio between the carrier frequency and the output fundamental frequency.

Khanniche (1991) in his paper describe a novel switching strategy of a single phase microcontroller UPS system. The quality of the inverter output voltage waveform is dictated by the adopted switching method and the available switching devices in terms of speed and cost. One of the requirements in this application is the significant reduction in the hardware while achieving a high quality output regulated voltage. With his proposed method, only one passive component is used to obtain a pure sinusoidal voltage waveform. The method used is three level improved PWM switching techniques, where the switching angles are computed on line and in real time using the 16-bit single chip microcontroller. The results were confirmed that the inverter efficiency is 80%.

Dimitriu (2003) in his paper described a control with microcontroller for PWM single phase inverter. The control principles for a PWM single phase inverter are using the capabilities of 80C552 microcontroller. The powerful T2 timer gives its useful feature in this application. The carrier frequency used is 5 kHz. The result has confirmed the high quality of the control based on microcontroller techniques.

Meksarik (2005) developed a new switching strategy based on the SPWM technique combines with low frequency 50 Hz signal. The results were confirmed that the inverter could produce voltage and current waveform purely sinusoidal with THD less than 3%. The switching losses have been significantly reduced and the efficiency has been achieved up to 90%.

2.6 Summary

General discussion on the inverter operation and its switching scheme has been made throughout this chapter. Natural sampling and regular sampling is two PWM switching scheme. Nowadays regular sampling PWM is the popular technique to be implemented in digital technique. SPWM with Unipolar voltage switching scheme has better harmonic profile compare to Bipolar voltage switching. Because of that, SPWM with Unipolar voltage switching will use as a switching scheme for the single phase inverter.

CHAPTER 3
DESIGN OF SWITCHING PULSES FOR SINGLE PHASE INVERTER

3.0 Introduction

In this chapter, the design of the switching pulses for the single phase full bridge inverter is described clearly. Figure 3.1 shows the flowchart design of switching pulses for single phase inverter. This project can be divided into three main parts. The first part is inverter switching strategy and its operation. The second part is development of the SPWM switching pulses equation by using volt-second concept. The third part is calculating the SPWM switching pulses based on the development equation.

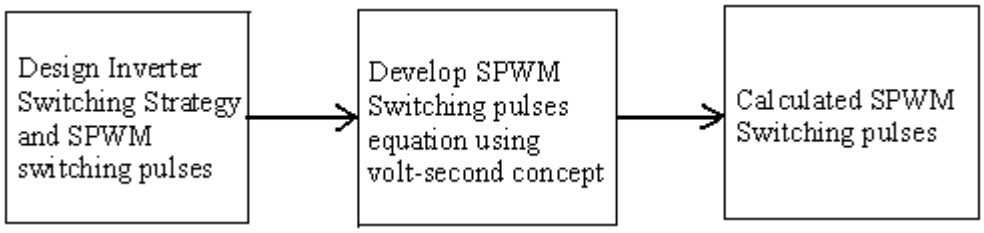

Figure 3.1: Flowchart design of switching pulses

3.1 Inverter Switching Strategy and its Operation

The basic single phase full bridge inverter topology with the control strategy is shown in Figure 3.2. The control strategy is performed in such away a pair (S1 and S4) of switches is turn on during another pair (S2 and S3) is turn off. In this application, when a pair (S2 and S3) turn on the other pair (S1 and S4) is automatically turn off. The sequences of on and off of the switches occurred continuously and sequentially. This produces an alternating output voltage across the load.

In this design an Unipolar SPWM voltage switching scheme (Ismail, 2006b) (Mihalache , 2002) (Mohan, 2003) is selected because this method offers the advantage of effectively doubling the switching frequency of the inverter voltage, thus making the output filter smaller, cheaper and