UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang 1990/91

Oktober /November 1990

EET 207 - Pemikroproses dan Peralatan Digit

Masa : [3 jam]

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi 4 muka surat beserta LAMPIRAN (3 muka surat) bercetak dan ENAM (6) soalan sebelum anda memulakan peperiksaan ini.

Jawab LIMA (5) soalan.

Agihan markah bagi setiap soalan diberikan di sut sebelah kanan sebagai peratusan daripada markah keseluruhan yang diperuntukkan bagi soalan berkenaan.

Jawab kesemua soalan di dalam Bahasa Malaysia.

...2/-

1. Dua bait ingatan dikhaskan untuk menyimpan nilai 16 bit. Nilai ini diguna untuk membilang berapa kali suatu peristiwa luaran telah berlaku. BIL dan BIL + 1 adalah alamat yang digunakan untuk nilai 16 bit ini. Suatu lazim khidmat sampukan di alamat 38H akan meningkatkan kandungan BIL setiap kali ianya dipanggil.

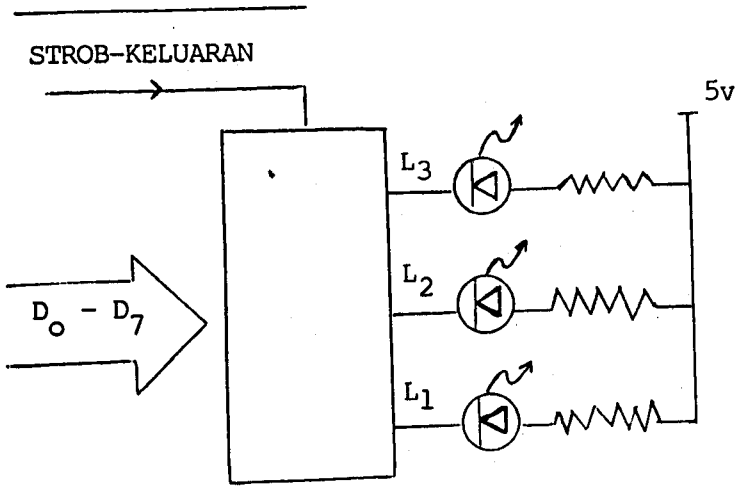
   Tulis lazim khidmat sampukan ini. (50%)

   Hasilkan perkakasan luaran untuk menyampuk 8085A dan memberi nilai vektor 38 H secara terus. Cuma guna masukan sampukan INTR.

   (50%)

2. Rajah 1 menunjukkan satu liang keluaran sistem 8085 yang dipandukan oleh hablur 2 MHz. Lampu L3 yang disambungkan kepada bit 2 hendak dikelipkan dengan kadar 20 Hz (nisbah tanda ke ruang adalah sama). Keadaan lampu-lampu lain mestilah tidak berubah. Tulis satu aturcara bahasa penghimpun 8085A untuk melaksanakan ini.

   (80%)



Rajah 1

Jika satu masa tunggu dimasukkan ke dalam setiap kitaran mesin apakah akibat di atas pemasaan.

(20%)

3. Pemikroproses 8085A mengguna talian AD_0 - AD_7 untuk membawa alamat dan data. Untuk mengasingkan komponen alamat dan data satu selak 8212 digunakan. Tunjukkan litar.

(50%)

Selak 8212 boleh digunakan sebagai liang masukan. Katakan satu liang masukan yang beralamat OFEH dikehendaki. Tunjukkan litar liang masukan ini termasuk dengan litar menyahkod alamat.

(50%)

4. Perkakasan penukar A/D boleh dihasilkan dari satu liang keluaran, satu liang masukan, penukar D/A dan pembanding. Tunjukkan rajah blok untuk sistem ini.

(50%)

Tuliskan aturcara bahasa penghimpun 8085A untuk penukar A/D dengan mengguna kaedah pembilang.

(50%)

5. Suruhan-suruhan pemikroproses 8085A boleh dikumpulkan dalam lima kumpulan. Nyatakan kumpulan-kumpulan ini dan terangkan fungsi setiap kumpulan suruhan.

(25%)

Satu jadual lompat diguna untuk menyimpan alamat masukan kepada enambelas sublazim. Nilai di antara 0 hingga 15 dalam penumpuk memilih lazim yang hendak dilaksanakan. Tulis satu aturcara dalam bahasa penghimpun 8085A untuk melakukan ini. Satu keadaan ralat akan dikembalikan dengan memasang bendera pembawa sekiranya nilai dalam penumpuk <0 atau >15.

(75%)

6. Terangkan bagaimana perpindahan data dilaksanakan dengan kawalan capaian ingatan cara langsung (DMA).

(30%)

Satu liang keluaran yang mengguna jabat salam hendak dilaksanakan.

Hasilkan litar untuk liang tersebut.

(35%)

Berikan aturcara bahasa penghimpun 8085A yang dapat menghantar data menerusi liang di atas dengan kaedah tinjauan.

(35%)

- oooOooo -

LAMPIRAN A

intel

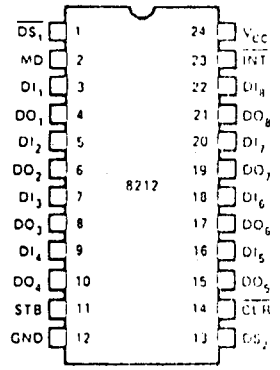
8212
8-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25mA Max.
- Three State Outputs
- Outputs Sink 15mA
- 3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

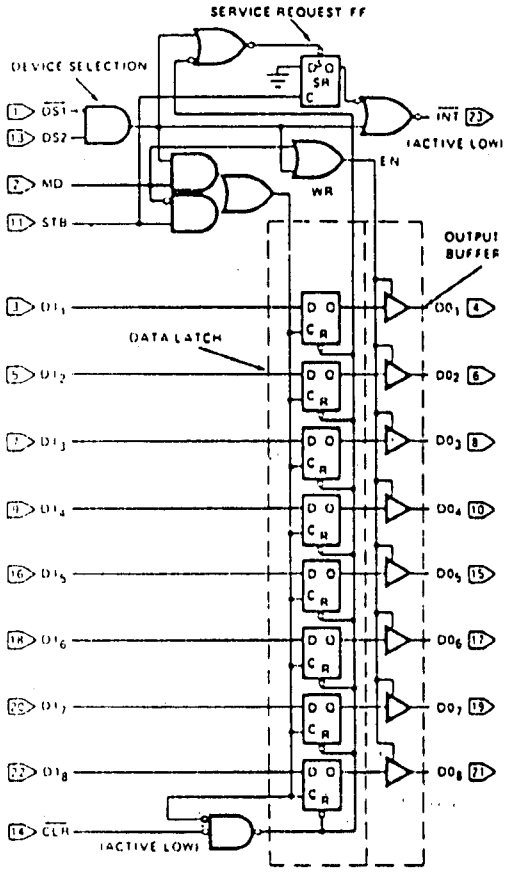
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$, DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



LAMPIRAN B

INSTRUCTION TIMINGS

Mnemonic	Description	Clock(2) Cycles
MOVE, LOAD, AND STORE		
MOV r1 r2	Move register to register	4
MOV M,r	Move register to memory	7
MOV r,M	Move memory to register	7
MVI r	Move immediate register	7
MVI M	Move immediate memory	10
LXI B	Load immediate register Pair B & C	10
LXI D	Load immediate register Pair D & E	10
LXI H	Load immediate register Pair H & L	10
LXI SP	Load immediate stack pointer	10
STAX B	Store A indirect	7
STAX D	Store A indirect	7
LDAX B	Load A indirect	7
LDAX D	Load A indirect	7
STA	Store A direct	13
LDA	Load A direct	13
SHLD	Store H & L direct	16
LHLD	Load H & L direct	16
XCHG	Exchange D & E, H & L Registers	4
STACK OPS		
PUSH B	Push register Pair B & C on stack	12
PUSH D	Push register Pair D & E on stack	12
PUSH H	Push register Pair H & L on stack	12
PUSH PSW	Push A and Flags on stack	12
POP B	Pop register Pair B & C off stack	10
POP D	Pop register Pair D & E off stack	10
POP H	Pop register Pair H & L off stack	10
POP PSW	Pop A and Flags off stack	10
XTHL	Exchange top of stack, H & L	16
SPHL	H & L to stack pointer	6
JUMP		
JMP	Jump unconditional	10
JC	Jump on carry	7/10
JNC	Jump on no carry	7/10
JZ	Jump on zero	7/10
JNZ	Jump on no zero	7/10
JP	Jump on positive	7/10
JM	Jump on minus	7/10
JPE	Jump on parity even	7/10
JPO	Jump on parity odd	7/10
PCHL	H & L to program counter	6
CALL		
CALL	Call unconditional	18
CC	Call on carry	9/18
CNC	Call on no carry	9/18
CZ	Call on zero	9/18
CNZ	Call on no zero	9/18
CP	Call on positive	9/18
CM	Call on minus	9/18
CPE	Call on parity even	9/18
CPO	Call on parity odd	9/18
RETURN		
RET	Return	10
RC	Return on carry	6/12
RNC	Return on no carry	6/12
RZ	Return on zero	6/12
RNZ	Return on no zero	6/12
RP	Return on positive	6/12
RM	Return on minus	6/12
RPE	Return on parity even	6/12
RPO	Return on parity odd	6/12
RESTART		
RST	Restart	12
INPUT/OUTPUT		
IN	Input	10
OUT	Output	10
INCREMENT AND DECREMENT		
INR r	Increment register	4
DCR r	Decrement register	4
INR M	Increment memory	10
DCR M	Decrement memory	10
INX B	Increment B & C registers	6
INX D	Increment D & E registers	6
INX H	Increment H & L registers	6
INX SP	Increment stack pointer	6
DCX B	Decrement B & C	6
DCX D	Decrement D & E	6
DCX H	Decrement H & L	6
DCX SP	Decrement stack pointer	6
ADD		
ADD r	Add register to A	4
ADC r	Add register to A with carry	4
ADD M	Add memory to A	7
ADC M	Add memory to A with carry	7
ADI	Add immediate to A	7
ACI	Add immediate to A with carry	7
DAD B	Add B & C to H & L	10
DAD D	Add D & E to H & L	10
DAD H	Add H & L to H & L	10
DAD SP	Add stack pointer to H & L	10
SUBTRACT		
SUB r	Subtract register from A	4
SBB r	Subtract register from A with borrow	4
SUB M	Subtract memory from A	7
SBB M	Subtract memory from A with borrow	7
SUI	Subtract immediate from A	7
SBI	Subtract immediate from A with borrow	7
LOGICAL		
ANA r	And register with A	4
XRA r	Exclusive OR register with A	4
ORA r	OR register with A	4
CMP r	Compare register with A	4
ANA M	And memory with A	7
XRA M	Exclusive OR memory with A	7
ORA M	OR memory with A	7
CMP M	Compare memory with A	7
ANI	And immediate with A	7
XRI	Exclusive OR immediate with A	7
ORI	OR immediate with A	7
CPI	Compare immediate with A	7
ROTATE		
RLC	Rotate A left	4
RRC	Rotate A right	4
RAL	Rotate A left through carry	4
RAR	Rotate A right through carry	4
SPECIALS		
CMA	Complement A	4
STC	Set carry	4
CMC	Complement carry	4
DAA	Decimal adjust A	4
CONTROL		
EI	Enable Interrupts	4
DI	Disable Interrupt	4
NOP	No-operation	4
HLT	Halt	5
NEW 8085A INSTRUCTIONS		
RIM	Read Interrupt Mask	4
SIM	Set Interrupt Mask	4

NOTES: 1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

LAMPIRAN C

HEXADECIMAL CODING CHART

DATA TRANSFER GROUP

Move

MOV	A,A	7F
	A,B	78
	A,C	79
	A,D	7A
	A,E	7B
	A,H	7C
	A,L	7D
	A,M	7E
MOV	B,A	47
	B,B	40
	B,C	41
	B,D	42
	B,E	43
	B,H	44
	B,L	45
	B,M	46
MOV	C,A	4F
	C,B	48
	C,C	49
	C,D	4A
	C,E	4B
	C,H	4C
	C,L	4D
	C,M	4E
MOV	D,A	57
	D,B	50
	D,C	51
	D,D	52
	D,E	53
	D,H	54
	D,L	55
	D,M	56

Move (cont)

MOV	E,A	5F
	E,B	58
	E,C	59
	E,D	5A
	E,E	5B
	E,H	5C
	E,L	5D
	E,M	5E
MOV	H,A	67
	H,B	60
	H,C	61
	H,D	62
	H,E	63
	H,H	64
	H,L	65
	H,M	66
MOV	L,A	6F
	L,B	68
	L,C	69
	L,D	6A
	L,E	6B
	L,H	6C
	L,L	6D
	L,M	6E
MOV	M,A	77
	M,B	70
	M,C	71
	M,D	72
	M,E	73
	M,H	74
	M,L	75
XCHG		EB

Move Immediate

MVI	A, byte	3E
	B, byte	06
	C, byte	0E
	D, byte	16
	E, byte	1E
	H, byte	26
	L, byte	2E
	M, byte	36

Load Immediate

LXI	B, dble	01
	D, dble	11
	H, dble	21
	SP, dble	31

Load/Store

LDAX B	0A
LDAX D	1A
LHLD adr	2A
LDA adr	3A
STAX B	02
STAX D	12
SHLD adr	22
STA adr	32

byte = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity. (Second byte of 2-byte instructions).

dble = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity. (Second and Third bytes of 3-byte instructions).

adr = 16-bit address (Second and Third bytes of 3-byte instructions).

ARITHMETIC AND LOGICAL GROUP

Add

ADD	A	87
	B	80
	C	81
	D	82
	E	83
	H	84
	L	85
	M	86
ADC	A	8F
	B	88
	C	89
	D	8A
	E	8B
	H	8C
	L	8D
	M	8E

Subtract

SUB	A	97
	B	90
	C	91
	D	92
	E	93
	H	94
	L	95
	M	96
SBB	A	9F
	B	98
	C	99
	D	9A
	E	9B
	H	9C
	L	9D
	M	9E

Double Add

DAD	B	09
	D	19
	H	29
	SP	39

Increment

INR	A	3C
	B	04
	C	0C
	D	14
	E	1C
	H	24
	L	2C
	M	34
INX	B	03
	D	13
	H	23
	SP	33

Decrement

DCR	A	3D
	B	05
	C	0D
	D	15
	E	1D
	H	25
	L	2D
	M	35
DCX	B	0B
	D	1B
	H	2B
	SP	3B

Specials

DAA	27
CMA	2F
STC	37
CMC	3F

Rotate

RLC	07
RRC	0F
RAL	17
RAR	1F

Logical

ANA	A	A7
	B	A0
	C	A1
	D	A2
	E	A3
	H	A4
	L	A5
	M	A6
XRA	A	AF
	B	A8
	C	A9
	D	AA
	E	AB
	H	AC
	L	AD
	M	AE
ORA	A	B7
	B	B0
	C	B1
	D	B2
	E	B3
	H	B4
	L	B5
	M	B6
CMP	A	BF
	B	B8
	C	B9
	D	BA
	E	BB
	H	BC
	L	BD
	M	BE

Arith & Logical Immediate

ADI byte	C6
ACI byte	CE
SUI byte	D6
SBI byte	DE
ANI byte	E6
XRI byte	EE
ORI byte	F6
CPI byte	FE

BRANCH CONTROL GROUP

Jump

JMP adr	C3
JNZ adr	C2
JZ adr	CA
JNC adr	D2
JC adr	DA
JPO adr	E2
JPE adr	EA
JP adr	F2
JM adr	FA
PCHL	E9

Call

CALL adr	CD
CNZ adr	C4
CZ adr	CC
CNC adr	D4
CC adr	DC
CPO adr	E4
CPE adr	EC
CP adr	F4
CM adr	FC

Return

RET	C9
RNZ	C0
RZ	C8
RNC	D0
RC	D8
RPO	E0
RPE	E8
RP	F0
RM	F8

Restart

RST	0	C7
	1	CF
	2	D7
	3	DF
	4	E7
	5	EF
	6	F7
	7	FF

I/O AND MACHINE CONTROL

Stack Ops

PUSH	B	C5
	D	D5
	H	E5
	PSW	F5
POP	B	C1
	D	D1
	H	E1
	PSW	F1
XTHL		E3
SPHL		F9

Input/Output

OUT byte	D3
IN byte	DB

Control

DI	F3
EI	FB
NOP	00
HLT	76

New Instructions (8085 Only)

RIM	20
SIM	30