UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Pertama
Sidang Akademik 1994/95

Oktober/November 1994

CSY401 - Senibina Komputer

Masa: [3 jam]

ARAHAN KEPADA CALON:

- Sila pastikan bahawa kertas peperiksaan ini mengandungi **EMPAT** muka surat yang bercetak sebelum anda memulakan peperiksaan ini.
- Jawab **SEMUA** soalan. Anda boleh memilih untuk menjawab **SEBAHAGIAN** daripada soalan di dalam Bahasa Inggeris atau menjawab keseluruhan soalan di dalam Bahasa Malaysia.

ENGLISH VERSION OF THE QUESTION PAPER

Answer **ALL** questions, all the algorithms must be described briefly, description has to demonstrate main ideas of the algorithms only.

1. (a) Give the definition/notion of the following:

   (i) The structure of a simple computer and short description of its components.

   (ii) Number systems, decimal, binary, octal and hexadecimal number systems.

   (15/100)

   (b) Give the following algorithm and transformations:

   (i) Conversion of decimal into binary.

   (ii) Conversion of decimal into hexadecimal.

   (15/100)

   (c) Give the definition and describe the following notions and algorithms:

   (i) Notion of (r-1)'s complement.

   (ii) Fixed-point representation.

   (iii) Algorithms of numbers addition and subtraction.

   (iv) Floating-point representation.

   (20/100)

   (d) Transform the decimal number 274.75 into:

   (i) The binary number.

   (ii) The signed fixed-point representation.

   (iii) Its floating-point representation.

   (15/100)

   (e) Give the notion of interrupt system and describe its components.

   (i) General notion of an interrupt system.

   (10/100)

   (ii) List the hardware units to support an interrupt processing.

   (10/100)

   (iii) General algorithm of interrupt processing.

   (15/100)

2. (a) List and describe briefly three requirements to memory system management.

(15/100)

(b) Give the following algorithms/notions:

(i) Mathematical memory.

(ii) Paging, direct mapping algorithms of effective address calculation.

(iii) Segmentation, main algorithm of effective address calculation.

(30/100)

(c) Given that the segment size is 64K bytes, how does this be reflected in the structure of a good program?

(15/100)

(d) The notion of cache memory and algorithms for its management.

(i) Give general notion of cache memory.

(5/100)

(ii) List the arguments to use cache memory.

(10/100)

(iii) Give the direct mapping algorithm of cache memory management.

(10/100)

(iv) Assume the volume of a cache memory is 1024K words and direct mapping is used. There are two matrices A and B, each contains 20 x 20 elements. Give a flow-chart of matrices multiplication algorithm C = A x B and a scheme of main memory allocation to use cache memory in the most effective way to speedup a program. Two main memory pages can be used, each page contains 1024K words.

(15/100)

3. (a) The following are the general classification of multiprocessor systems. Give the definition and examples of each system.

(i) SISD systems.

(ii) SIMD systems.

(iii) MIMD systems.

(10/100)

(b) Give the definitions of the following architectures (main ideas). How can a speedup of computation is reached?

(i) Pipeline architecture multiprocessors.

(ii) Shared memory multiprocessors.

(iii) Distributed memory multiprocessors.

(iv) VLIW architecture multiprocessors.

(10/100)

(c) Identify potential data dependency hazard in the following code:

```
MOV AX,[100]
ADD AX,BX
MOV CX,1
MUL CX,AX
```

given a five-stage pipeline:

->fetch_instr.->decode->fetch_operand->execite_instr.->Store

(20/100)

(d) What is the average instruction processing time (number of clocks, one stage of pipeline is finished for 1 clock) of a five-stage instruction pipeline if conditional branch instruction occurs as follows:

third instruction,
tenth instruction.

Pipeline must be cleared after a branch instruction has been decoded.

(30/100)

(e) Develop the programs realizing the following algorithms:

(i) Polynoms multiplication on shared memory multiprocessor.

(ii) Scalar product of two vectors on VLIW multiprocessor.

(30/100)

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