# UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session of 2005/2006

November 2005

## EBB 526/3 - Electronic Packaging

Time : 3 hours

Please make sure that this examination paper consists of SEVEN printed pages before you begin with the exam.

This paper is made up of SEVEN questions.

Answer any FIVE questions. If a candidate answers more than five questions, only the first five answered will be examined and awarded marks.

Answer to any question must start on a new page.

All questions should be answered in English.

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1. [a] Describe (by using schematic diagram) polymers used in Flip Chip & Wire Bond packages.

(20 marks)

[b] What are the desired quality characteristics for underfill? State also the reasons for each characteristic.

(20 marks)

[c] What is underfill and their roles? Give typical components in CUF formulation and their functions.

(20 marks)

[d] Explain on why we need to optimize the filler loading in CUF? Discuss the effect of filler loading, size and shape on the mechanical properties of underfill.

(40 marks)

2. [a] Air at 20°C blows over a hot plate 50 by 75 cm maintained at 250°C. The convection heat transfer coefficient is 25 $W/m^2K$. Calculate the heat transfer.

(20 marks)

[b] An electric current is passed through a wire 1 mm in diameter and 10 cm long. The wire is submerged in liquid water at atmospheric pressure, and current is increased until the water boils. For this situation, h = 5000 $W/m^2K$ and water temperature will be 100°C. How much electric power must be supplied to the wire to maintain the wire surface at 114°C.

(30 marks)

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[c] In the diagram, die temperature is 82°C, IHS is 75°C, Heat Sink base temperature is 69°C, ambient temperature is 17°C. The die has a surface area of 1.2 $cm^2$ and generates 50W of power. Assuming one directional conduction heat transfer from the die to the heat sink, calculate the following:

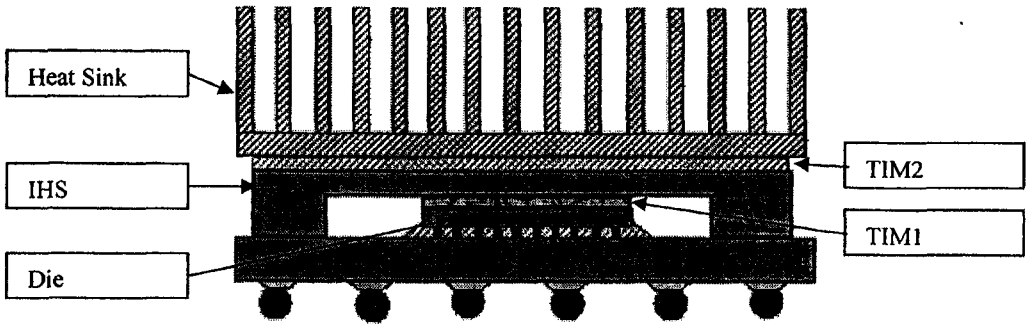
(i) Thermal impedance, Rjc of TIM 1

(ii) Thermal resistance, Θ-cs of TIM2

(iii) Heat sink performance, Θ-sa

(iv) Total thermal resistance of the whole assembly

(50 marks)

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3. [a] Four elements are involved in solder joint formation, namely flux, solder material, metal surface and heat. Flux plays very critical facilitation role to ensure proper solder joint formation:

(i) Sketch a typical solder reflow profile and explain the main 4 characteristics.

(ii) What is flux? Describe the 4 main component of flux and their functions.

(30 marks)

[b] In real life, electronic components are subjected to electrical, thermal and mechanical stresses. The solder interconnect and wire-bond interconnect must be able to withstand all the stresses during its entire life span. If not properly designed, the solder interconnect may fail due to creep, fatigue or solder joint brittle fracture.

(i) Describe what is the conditions for causing fatigue failure in solder interconnect.

(ii) Describe what is solder creep and conditions for causing solder creep failure.

(iii) With aid of sketches, describe two types of solder joint brittle fracture failures.

(70 marks)

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4. [a] What are the key criteria for polymer/epoxies to be used as TIM in electronic packages?

List 3 types of TIM and their advantages/disadvantages.

(40 marks)

[b] Why the bondline Thickness (BLT) is important in TIM? What contributes to its limitation to PTIM?

(25 marks)

[c] Use the knowledge that you learnt from Underfill and Mold Compound, explain how the polymer TIM will degrade and why it is a concern in the TIM development?

(35 marks)

5. There are 2 key packaging technologies that are commonly used today. One is the wirebonding package and the second one is the flip chip package.

(a) Select ONLY one of package technology and define a typical process flow for the package. Next, briefly describe the purpose of each process step for selected packaging technology.

(70 marks)

(b) Now, imagine you are the Director of the package development group for a multi-million dollars silicon chip corporation. You were told there are new Products A and B that require new packaging. Now, identify the best packaging technology that you would recommend for the assembly of the products. Please also explain why you would select the particular package for the different products.

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(I) Product A:

(i) Die size of 3 x 3 $mm^2$ and 3 mils thick.
(ii) Organic substrate size of 5 x 5 $mm^2$ and 0.5 mm thick
(iii) Total I/O = 1000
(iv) High frequency application = 10 Gigahertz
(v) Require second level interconnect using ball attach.

(II) Product B:

(i) Die size of 10 x 10 mm and 30 mils thick
(ii) Organic substrate size of 27 x 27 $mm^2$ and 0.8 mm thick.
(iii) Total I/O = 300
(iv) Low frequency application <200 MegaHertz
(v) Requiring second level interconnect using ball attach

(30 marks)

6. [a] Draw and label the construction of organic flup chip substrate and discuss the manufacturing process flow to manufacture an organic substrate.

(50 marks)

[b] Describe the core material of an organic substrate, in terms of its function, materials, defects and properties.

(30 marks)

[c] Briefly discuss the important properties of substrate materials.

(20 marks)

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7. [a] As future of microprocessor and network processors run at increase clock speeds, significant challenges are imposed on the performance of the package technology. Explain three challenges involve in electronic packaging technology and provide the solution to these challenges.

(30 marks)

[b] With the help of schematic diagram, label the materials used in general flip chip package and explain why these materials are being chosen?

(30 marks)

[c] Explain the differences between ceramic and organic packaging?

(20 marks)

[d] What is the reflow process in die preparation module? Explain method used in reflow process and list down the issue and challenges for this process.

(20 marks)

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