INVESTIGATION OF RADIO FREQUENCY MAGNETRON SPUTTERED THULIUM OXIDE PASSIVATION LAYER ON SILICON AND 4H-SILICON CARBIDE SUBSTRATES

DENG JUNCHEN

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by

DENG JUNCHEN

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DECLARATION

I hereby declare that this thesis, submitted to Universiti Sains Malaysia as partial fulfilment of the requirement for the Doctor of Philosophy, has not been submitted to any other Universities or Institutions for any degrees. I also declare that the work described herein is based on my original work, except for quotations and citations that have been duly acknowledged.

Deng Junchen

Date: 27/08/2025

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LIST OF ABBREVIATIONS

AC	Alternating Current
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ArOAr	Argon-Oxygen-Argon
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
CBO	Conduction Band Offset
DC	Direct Current
EDX	Energy Dispersive X-ray Spectroscopy
FESEM	Field Emission Scanning Electron Microscopy
FET	Field Effect Transistors
FG	Forming Gas
FGOFG	Forming Gas-Oxygen-Forming Gas
GIXRD	Grazing Incidence X-Ray Diffraction
ICDD	International Centre for Diffraction Data
IL	Interfacial Layer
I-V	Current-Voltage
J-E	Current Density-Electric Field
KM	Kubelka-Munk
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal-Oxide-Semiconductor
NON	Nitrogen-Oxygen-Nitrogen
PECVD	Plasma Enhanced Chemical Vapor Deposition
PL	Passivation Layer

RCA	Radio Corporation America
RF	Radio Frequency
RMS	Root-Mean-Square
RTP	Rapid Thermal Process
SIMS	Secondary Ion Mass Spectroscopy
STD	Slow Trap Density
UV-Vis	Ultraviolet-Visible
VBO	Valence Band Offset
XPS	X-ray Photoelectron Spectroscopy
XRR	X-ray Reflectivity

LIST OF SYOMBLS

a	Lattice Parameter
C	Capacitance
C_{ox}	Oxide Capacitance
d	Interplanar Spacing
D	Crystallite Size
k	Dielectric Constant
D_{it}	Interface Trap Density
E_B	Breakdown Field
E_F	Fermi Level
G	Conductance
q	Electronic Charge
Q_{eff}	Effective Oxide Charge
Q_f	Oxide Fixed Charges
Q_m	Mobile Ionic Charge
Q_{ot}	Oxide Trapped Charge
T_{hkl}	Coefficient or Texture
t_{ox}	Oxide Thickness
V_{FB}	Flat Band Voltage
V_o	Oxygen Vacancies
V_g	Gate Voltage
ΔV_{FB}	Flat Band Voltage Shift
θ	Diffraction Angles
ε	Microstrain
ε_0	Free space Permittivity

PENYIASATAN LAPISAN PEMPASIFAN OKSIDA TULIUM YANG DIPERCIK MAGNETRON FREKUENSI RADIO KE ATAS SUBSTRAT SILIKON DAN 4H-SILIKON KARBIDA

ABSTRAK

Tulium oksida (Tm_2O_3) telah dimendapkan atas substrat silikon (Si) dan 4H-silikon karbida (SiC) menggunakan teknik percikan magnetron frekuensi radio (RF) yang berfungsi sebagai lapisan pempasifan berpemalar dielektrik tinggi (k) untuk menangani batasan prestasi peranti logam-oksida-semikonduktor (MOS) kuasa. Batasan ini timbul daripada lapisan pempasifan silikon dioksida (SiO_2) ber-k rendah dan jurang jalur sempit Si. Kajian awal Tm_2O_3 sebagai lapisan pempasifan untuk kapasitor MOS berasaskan Si telah dijalankan dalam persekitaran penyepuhlindapan yang menggabungkan nitrogen-oksigen-nitrogen (NON) pada suhu 500, 600, 700, dan 800°C. Keputusan menunjukkan bahawa ion nitrogen telah dimasukkan ke dalam lapisan pempasifan Tm_2O_3 semasa proses penyepuhlindapan yang mewujudkan lapisan halangan resapan pada antaramuka. Perkara ini menghalang pembentukan lapisan antaramuka, mempamerkan nilai k tertinggi iaitu 16.0 dengan cas oksida berkesan (Q_{eff}; 4.89×10^{12} cm^{-2}) dan ketumpatan perangkap antaramuka (D_{it}) yang agak tinggi pada 700°C. Kajian lanjut telah dijalankan untuk lapisan pempasifan Tm_2O_3 yang menjalani penyepuhlindapan pasca pemendapan pada 700°C dalam persekitaran yang berbeza (NON, gas pembentuk-oksigen-gas pembentuk (FGOFG) dan argon-oksigen-argon (ArOAr)). Keputusan menunjukkan bahawa kehadiran hidrogen dan nitrogen dalam persekitaran gas pembentuk membolehkan lapisan pempasifan Tm_2O_3 mencapai nilai k yang tinggi (16.8), medan pecah tinggi (E_B, 4.03 MV/cm), Q_{eff} rendah (1.32×10^{12} cm^{-2}), dan D_{it} pada paras yang boleh diterima. Kajian

susulan mengenai kesan penyepuhlindapan FGOFG pada suhu 500, 600, 700, dan 800°C seterusnya mengesahkan bahawa penyepuhlindapan FGOFG pada 700°C adalah keadaan optimum untuk lapisan pempasifan Tm_2O_3 pada Si. Kebolehgunaan Tm_2O_3 sebagai lapisan pempasifan untuk substrat 4H-SiC telah dikaji dalam persekitaran optimum (FGOFG) pada 600, 700, 800, dan 900°C. Lapisan pempasifan Tm_2O_3 yang disepuhlindap pada 800°C dalam persekitaran FGOFG mempamerkan prestasi optimum yang dicirikan oleh nilai *k* paling tinggi (12.2), STD paling rendah (1.09×10^{12} cm^{-2}), D_{it} pada paras yang boleh diterima, dan E_B paling tinggi (3.86 MV/cm). Akhirnya, prestasi lapisan pempasifan Tm_2O_3 pada substrat 4H-SiC telah ditambahbaik lagi menggunakan prosedur penyepuhlindapan dwi peringkat novel, yang merangkumi pemprosesan terma pantas (RTP) pada 600, 700, 800, dan 900°C, diikuti dengan penyepuhlindapan biasa yang optimum (800°C dalam FGOFG). Penemuan mendedahkan bahawa RTP pada 900°C berkesan dalam mengehadkan pembentukan lapisan antaramuka dan menghapuskan perangkap. Hal ini dibuktikan dengan perolehan nilai *k* tertinggi (13.3), Q_{eff} terendah (1.87×10^{12} cm^{-2}), arus bocor terendah, E_B tertinggi (4.04 MV/cm), dan D_{it} terendah, turut mencadangkan potensi yang signifikan untuk aplikasi praktikal dalam peranti MOS berasaskan 4H-SiC.

INVESTIGATION OF RADIO FREQUENCY MAGNETRON SPUTTERED THULIUM OXIDE PASSIVATION LAYER ON SILICON AND 4H-SILICON CARBIDE SUBSTRATES

ABSTRACT

Thulium oxide (Tm_2O_3) was deposited on silicon (Si) and 4H-silicon carbide (SiC) substrates using radio frequency (RF) magnetron sputtering technique, functioning as the high dielectric constant (*k*) passivation layers to address the performance limitations of power metal-oxide-semiconductor (MOS) devices, which arose from the low *k* silicon dioxide (SiO_2) passivation layer and the narrow band gap of Si. The preliminary investigation of Tm_2O_3 as a passivation layer for Si-based MOS capacitors was conducted in a combined nitrogen-oxygen-nitrogen (NON) annealing ambient at temperature of 500, 600, 700, and 800°C. The results indicated that nitrogen ions were incorporated into the Tm_2O_3 passivation layer during the annealing process, creating a diffusion barrier layer at the interface. This hindered the formation of the interfacial layer, which exhibited the highest *k* value of 16.0 with relatively high effective oxide charge (Q_{eff}; 4.89×10^{12} cm^{-2}) and interface trap density (D_{it}) at 700°C. Further research was conducted for Tm_2O_3 passivation layer subjected to post deposition annealing at 700°C in different ambient (NON, forming gas-oxygen-forming gas (FGOFG) and argon-oxygen-argon (ArOAr)). The results indicated that the presence of hydrogen and nitrogen in the forming gas ambient enabled the Tm_2O_3 passivation layer to achieve a high *k* value (16.8), a high breakdown field (E_B, 4.03 MV/cm), a low Q_{eff} (1.32×10^{12} cm^{-2}), and an acceptable D_{it}. Subsequent investigation of the effects of FGOFG annealing at temperatures of 500, 600, 700, and 800°C further confirmed that FGOFG annealing at 700°C was the optimal condition for the Tm_2O_3

passivation layer on Si. The feasibility of Tm_2O_3 as the passivation layer for 4H-SiC substrate was examined in the optimized ambient (FGOFG) at 600, 700, 800, and 900°C, wherein the Tm_2O_3 passivation layer annealed at 800°C in the FGOFG ambient demonstrated optimum performance, characterized by the highest k value (12.2), the lowest STD (1.09×10^{12} cm^{-2}), an acceptable D_{it}, and the highest E_B (3.86 MV/cm). Finally, the performance of the Tm_2O_3 passivation layer on 4H-SiC substrate was further improved using a novel dual stage annealing procedure, which included rapid thermal processing (RTP) at 600, 700, 800, and 900°C, followed by an optimized normal annealing (800°C in FGOFG). The findings revealed that the RTP at 900°C effectively limited the formation of the interfacial layer and annihilated the traps. This was evidenced by the acquisition of the highest k value (13.3), the lowest Q_{eff} (1.87×10^{12} cm^{-2}), the lowest leakage current, the highest E_B (4.04 MV/cm), and the lowest D_{it}, suggesting significant potential for practical applications in 4H-SiC-based MOS devices.

CHAPTER 1

INTRODUCTION

1.1 Overview

The field of semiconductor technology had been studied for over a century and a half since the asymmetric current-voltage (*I-V*) characteristics with respect to voltage polarity of a metal-galena contact was discovered by Karl Ferdinand Braun in 1874 (Braun, 1874). Human industry and daily life have become increasingly dependent on a wide range of semiconductor-based devices (She *et al.*, 2017). However, the challenge of power devices attaining higher power density, higher efficiency, and integrating many systems has been highlighted as the energy supply mode has been gradually transferred from conventional fossil fuels to renewable sources in recent years (Langpoklakpam *et al.*, 2022). Particularly in the booming developed photovoltaic and electric vehicle industries, the silicon (Si)-based metal-oxide-semiconductor (MOS) devices were deemed to be having shortcoming of fulfilling the increased demands in blocking voltage capability, operation temperature, and switching frequency to reduce energy dissipation in the devices (Kaminski *et al.*, 2014; Millan *et al.*, 2014). The wide band gap (WBG) semiconductor, namely 4H-silicon carbide (4H-SiC) has been employed as the next generation semiconductor material to replace the narrow band gap Si for the MOS-based devices (She *et al.*, 2017). The employment of 4H-SiC semiconducting material would allow the development of high power and energy efficient MOS-based devices due to the fascinating properties, such as large energy band gap (E_g = 3.26 eV) (She *et al.*, 2017), high E_B (~2-3 MV/cm) (L. Huang *et al.*, 2021; She *et al.*, 2017), and a large thermal conductivity (4.9 W/cm·K) (L. Huang *et al.*, 2021). Another merit of employing 4H-SiC for MOS-based devices

was the ease of duplicating the well-established fabrication technique for Si-based MOS devices (Pensl *et al.*, 2006) as well as the ability of growing high quality silicon dioxide (SiO_2) passivation layer (PL) on 4H-SiC (Shenoy *et al.*, 1995), which has hence hastened the release of 4H-SiC-based MOS devices in the commercial market.

Nevertheless, according to the Gauss' law, the ratio of electric field strength in 4H-SiC and SiO_2 is inversely proportional to the ratio of dielectric constant (k) of 4H-SiC (~10) and SiO_2 (3.9) (Lipkin *et al.*, 1999), indicating that the electric field strength in SiO_2 PL is ~2.5 times higher than that in the 4H-SiC substrate. The utilization of the low-k SiO_2 as the PL for 4H-SiC-based MOS devices would thus inhibit the full potential of 4H-SiC because the device breakdown was limited by the low-k SiO_2 PL rather than the 4H-SiC substrate (Palmour *et al.*, 1997). Therefore, it is of great significance to explore alternative passivation materials that possess a high k and E_g greater than that of SiO_2, low defect density, and a high conduction band offset (CBO) with respect to the 4H-SiC substrate (Palmour *et al.*, 1997).

1.2 Problem Statement

Extensive research has been conducted on SiO_2 PL thermally grown on 4H-SiC and currently attained a promising interface trap density (D_{it}=3.9 × 10^9 $eV^{-1}cm^{-2}$ at E_c-E_t= 0.4 eV) (Cabello *et al.*, 2017) and a lower leakage current density of ~ 10^{-9} A/cm^{-2} at 1 MV/cm (Yin *et al.*, 2022). However, according to Gauss' law ($\nabla \cdot \varepsilon_r \varepsilon_0 \vec{E}=0$), the low k value of SiO_2 would limit the performance of 4H-SiC-based MOS devices in high temperature, high voltage, and high frequency applications hindering the device's blocking voltage capabilities, hence exacerbating reliability concerns (Lipkin *et al.*, 1999). Therefore, numerous efforts were carried out to address the issue by replacing the low k SiO_2 with a high k material as a PL for the 4H-SiC-based MOS devices, aiming to sustain a high E_B and low leakage current density (Siddiqui *et al.*,

2021). In search of alternative passivation materials for 4H-SiC, high *k* materials, such as aluminum oxide (Al_2O_3) (Suvanam *et al.*, 2018), aluminum nitride (AlN) (J. Chen *et al.*, 2019), hafnium oxide (HfO_2) (Kwon *et al.*, 2018), zirconium oxide (ZrO_2), titanium oxide (TiO_2), yttrium oxide (Y_2O_3) (Quah *et al.*, 2010), tantalum pentoxide (Ta_2O_5) (Zhao *et al.*, 2006), lanthanum oxide (La_2O_3) (Y. Wang *et al.*, 2015), as well as various lanthanides rare-earths oxides, such as cerium oxide (CeO_2) (W. F. Lim *et al.*, 2010), praseodymium oxide (Pr_2O_3) (Goryachko *et al.*, 2004), gadolinium oxide (Gd_2O_3) (Fissel *et al.*, 2006b), holmium oxide (Ho_2O_3) (Odesanya *et al.*, 2023) were investigated as potential PLs for the 4H-SiC-based MOS devices.

However, it is crucial to recognize that each of these materials has its own disadvantages. For example, a relatively smaller CBO of 0.53 eV for HfO_2 and 0.45 eV for ZrO_2 PLs on the 4H-SiC substrate was reported (Z. Wang *et al.*, 2020), indicating that these PL might lead to increased leakage current due to the lower barrier height (Siddiqui *et al.*, 2021). Furthermore, materials such as Al_2O_3 and AlN exhibited a relative lower *k* value, which could compromise the original intention of replacing lower *k* SiO_2 PL (Siddiqui *et al.*, 2021). Therefore, exploring high *k* materials like thulium oxide (Tm_2O_3), which has shown both high *k* value and wide band gap on Si (Pan *et al.*, 2010) and germanium (Ge) (Žurauskaitė *et al.*, 2018) substrates is of great significance. Tm_2O_3 was investigated extensively as a high-*k* PL for Si and Ge substrate by virtue of its excellent properties, such as high-*k* value (9.4-18.0) (Kouda *et al.*, 2011; Litta, Hellström, Henkel, Valerio, *et al.*, 2013; Mitrovic *et al.*, 2013; Päiväsaari *et al.*, 2005; Shannon, 1993), wide E_g (5.2-6.8 eV) (Mitrovic *et al.*, 2013, 2015; J. Wang *et al.*, 2012; J. J. Wang *et al.*, 2012), large CBO with relative to Si (2.00-2.95 eV) (J. J. Wang *et al.*, 2012; Yao *et al.*, 2016), low lattice mismatch with the Si substrate (J. J. Wang *et al.*, 2012), and excellent thermal stability (Zdanowicz, 1988).

However, it is regretful that, despite the above-mentioned attractive properties of Tm_2O_3 as a high-*k* PL for 4H-SiC-based MOS devices, there have been no attempts being reported to date to use this material for passivating 4H-SiC surfaces. Therefore, this work presents a systematic and comprehensive investigation of the Tm_2O_3 PL on Si and 4H-SiC substrates, along with the impact of post-deposition annealing (PDA) on its performance to address the aforesaid problems.

1.3 Research Objectives

The primary objective of this research is to unveil the potential of Tm_2O_3 as a high-*k* PL for the realization of 4H-SiC-based MOS devices. In order to achieve this primary objective, it is imperative to address the following aspects:

1. To investigate the effects of varying PDA temperature (500, 600, 700, 800^oC) and ambient (nitrogen-oxygen-nitrogen (NON), forming gas-oxygen-forming gas (FGOFG) and argon-oxygen-argon (ArOAr)) onto physical, chemical, and electrical characteristics of Tm_2O_3 PL deposited on Si substrate.
2. To assess the feasibility of utilizing Tm_2O_3 as a high-*k* PL for 4H-SiC-based MOS device, using the optimized annealing ambient determined for Si substrate (FGOFG).
3. To evaluate the effectiveness of introducing dual stage annealing ("RTP + Normal Annealing") onto characteristics of Tm_2O_3 PL deposited on 4H-SiC substrate.

1.4 Research Scope

In this research, firstly, the investigation was carried out in NON ambient at varying temperatures of 500, 600, 700, and 800^oC to determine the optimal annealing temperature for the Tm_2O_3 PL deposited on Si substrate using radio frequency magnetron sputtering process. The optimized annealing temperature determined in the

previous investigation was used in the ensuing experiment, which involved varying the PDA ambient (NON, FGOFG and ArOAr) to determine the optimal annealing ambient for the Tm_2O_3 PL deposited on Si substrate. Subsequently, the optimized annealing temperature and ambient for Tm_2O_3 deposited on Si substrate were also investigated on 4H-SiC substrate. This was done by investigating the effect of PDA at different temperatures (600, 700, 800, and 900ºC) in the FGOFG ambient. Then, a novel strategy was utilized to improve the performance of the Tm_2O_3 PL on the 4H-SiC substrate. This involved studying the impact of a combinative annealing process, which consisted of a rapid thermal process at temperatures of 600, 700, 800, and 900ºC for a duration of 3 min, followed by the optimized normal annealing process using FGOFG at a temperature of 800ºC for a duration of 30 min.

1.5 Thesis Outline

This thesis comprises six chapters. Chapter 1 provides an overview, problem statement, as well as research objectives and scope of the research carried out. Chapter 2 presents a comprehensive literature review that explores the background studies and fundamental theories relevant to the research. Chapter 3 offers a systematic research methodology, information on the raw materials used, and experimental design specific to the research. Chapters 4 and 5 include the obtained results and discussion of the investigated Tm_2O_3 PL deposited on Si and 4H-SiC substrates, respectively. Finally, Chapter 6 presents a brief summary of the primary findings of this research, along with recommendations for future efforts.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Semiconductor technology has been researched for nearly 150 years since Karl Ferdinand Braun discovered the asymmetric current-voltage properties of a metal-galena contact in 1874 (Braun, 1874). Countless semiconductor devices have been invented, revolutionizing human production and life. Among the various devices, the MOS devices, especially the transistor invented by John Bardeen and Walter Brattain in 1947, were widely considered as one of the greatest inventions of the 20th century (John *et al.*, 1950). It sparked a revolution in electronics comparable to that of steel and steam engines in the Industrial Revolution. The real MOS Field-Effect Transistor (MOSFET) was invented in 1959 by Mohamed Atalla and Dawon Kahng, who introduced a thin layer of SiO_2 as an insulating layer between the metal gate electrode and Si substrate to serve as a passivation layer (PL) and to effectively control the flow of current by harnessing electric fields (Atalla *et al.*, 1965). The MOSFET is one of the most pivotal innovations in the realm of semiconductor technology, fundamentally transforming the landscape of electronic devices by boasting superior scalability, reducing power consumption, and enhancing reliability, hence facilitating the development of high-speed, low-power electronic circuits, laying the groundwork for digital revolution (J. Robertson, 2006). With the subsequent invention and rapid development of large-scale integrated circuits (ICs) on Si, the number of transistors on ICs was doubling approximately every two years, as predicted by Gordon Moore (Moore, 1965). Furthermore, it was worth noting that the superior characteristics of thermally grown native SiO_2, such as its wide E_g (9 eV) and excellent SiO_2/Si interfacial quality, allowed the scaling of Si-based MOS devices to dominate the entire

semiconductor industry over the years (Iwai and Ohmi, 2002). However, the constant scaling of MOS devices has pushed the SiO_2 PL to its limits, leading to its replacement with hafnium-based high-*k* material as a PL in Intel commercial processors in 2007 (Clara, 2007). Moreover, keeping in pace with the escalating global energy and environmental concerns in recent years, which have presented a new challenge for high temperature, high power applications MOS devices, the development of novel wide band gap (WBG) semiconductor substrates, such as silicon carbide (SiC), gallium nitride (GaN), and diamond is becoming imperative (She *et al.*, 2017).

This chapter presents the relevant pertinent fundamental knowledge and current state of this thesis. The advantage and the properties of SiC are presented, along with the challenges encountered for Si and SiC-based MOS devices. Then, the development state of surface passivation for 4H-SiC in particular is outlined. Following that, an overview of the properties of Tm_2O_3, which include the potential and challenge of replacing SiO_2 with Tm_2O_3 as a PL is presented. The effect of the PDA on improving the passivation characteristic of Tm_2O_3 PL are also reviewed.

2.2 The Escalating Demand and Challenge for Si-Based Power Devices

Progress in power electronics technology has ended up resulting in enhanced efficiency, greater power density, and superior integration, with power semiconductor devices being crucial to this progress (Kassakian *et al.*, 2013). Thus far, developments have mostly been driven by various power devices based on Si.

In terms of power applications under 600 V, the trench gate structure type of MOSFET is leading the market. On the other hand, insulated gate bipolar transistors (IGBTs) based on the injection enhancement and field stop technologies are gaining popularity (She *et al.*, 2017). Despite these developments, the Si-based power devices are nearing their performance constraints. It was revealed that the IGBT has a

maximum blocking voltage below 6.5 kV and a feasible working temperature under 175°C (Millan *et al.*, 2014). Furthermore, IGBTs demonstrates poor switching rates due to the bipolar current conduction process, which restricts the applications with lower switching frequencies (Millan *et al.*, 2014). Hence, advancements in Si-based power device will persist, but at a diminished rate. Recently, due to the technological advancements that have occurred in the power industry, the use of WBG materials such as gallium nitride and SiC has increased (She *et al.*, 2017). The characteristics of these materials, such as their wider band gap and high saturation drift velocity, have attracted the attention of power device manufacturers (She *et al.*, 2017).

2.2.1 Potential of SiC as the WBG Semiconductor

Extensive study has been carried out on power devices using various substrates, including Si, SiC, GaN, diamond, gallium oxide (Ga_2O_3), and AlN (Donato *et al.*, 2020). The comparative analysis in term of materials properties of the substrates was shown in Table 2.1 (Donato *et al.*, 2020). At present, commercially available power devices on WBG substrates are limited to SiC and GaN whilst devices based on Ga_2O_3, diamond, and AlN are remain in research and development phase in laboratories (Donato *et al.*, 2020). Despite their excellent physical features, the Ga_2O_3, diamond, and AlN semiconductors are still encountering some obstacles that are impeding their complete use (Donato *et al.*, 2020). The mature technology and optimal balance between performance and cost are crucial for the development of an effective power device substrate (Donato *et al.*, 2020). Among the various commercially available SiC and GaN-based power devices, the GaN-based devices are primarily used for high-frequency applications due to the excellent properties of two-dimensional electron gas (2DEG) (Langpoklakpam *et al.*, 2022). Furthermore, the GaN on Si substrate is a more cost-effective option than SiC for lower voltage applications (typically below 650V),

making it the dominating choice in the market for voltage below 650V (Langpoklakpam *et al.*, 2022). Nevertheless, the presence of lattice and thermal mismatch between the GaN and Si has inevitably resulted in a greater number of dislocations and reduced thermal conductivity in comparison to SiC (Kaminski *et al.*, 2014). Although the availability of bulk GaN could be an alternative to GaN on Si substrate yet the resource is limited to tiny wafer dimensions and remains excessively costly, which would significantly impede the progress of GaN-based devices (Kaminski *et al.*, 2014).

For application involving higher voltages, exceeding 1700V, SiC in particularly the 4H-SiC comes into play due to its wide band gap, high saturation velocity, high E_B and excellent thermal conductivity (Table 2.1) makes SiC more tolerant of high voltages. These properties enable SiC devices to handle higher electric fields, operate at higher temperatures, and manage greater power densities than silicon and, in some aspects, even GaN, making them ideal for high-voltage and high-power applications. Additionally, compared to other WBG semiconductors, SiC is generally more mature in terms of quality of the crystal (Kimoto *et al.*, 2014), the existence of large wafers (Saddow *et al.*, 2004), lower material cost, and is readily available in the market (Kimoto *et al.*, 2014). Furthermore, due to the fact that SiC is the only compound semiconductor with a native and stable insulator, namely the SiO_2, obtained by thermal oxidation, the processing lines of SiC-based devices have great compatibility with that of Si-based devices (Salinaro, 2016), enabling the ideal use of the devices for high-power and voltage applications, which include but are not limited to electric vehicles, industrial motor drives, and power grids (Kaminski *et al.*, 2014). Therefore, SiC-based power devices have been extensively researched for high power/voltage applications for more than a decade.

Table 2.1 Materials properties of 4H-SiC with Si, GaN and Diamond (Donato *et al.*, 2020; Kaminski *et al.*, 2014).

Properties		Si	4H-SiC	GaN	Ga_2O_3	Diamond	AlN
Band gap (eV)		1.12	3.3	3.4	4.9	5.5	6.1
Mobility (cm^2/Vs)	Electron	1500	1000	2000 (2DEG) >1000 (bulk)	300	1060	300
	Hole	480	120	<100 (2DEG) <200 (bulk)	-	2100 (bulk) <300 (2DHG)	14
Thermal conductivity (W/m·K)		150	370	100 (on Si) 165 (on sapphire) 253 (on GaN)	11-27	2200-2400	253-319
Intrinsic carrier concentration (cm^{-3})		10^{10}	10^{-7}	10^{-10}	-	10^{-20}	-
Dielectric constant		11.8	9.8	9.0	9.9	5.5	8.5
Substrate diameter (inch)		8-17.7	8	8	4	<1	2
Substrate dislocations (per cm^{-2})		<10	10^2	10^4	10^4	10^4-10^6	10^4
Saturation velocity ($\times10^7$cm/s)	electron	1.0	1.9	2.5	2	2.5	1.4
	Hole	0.8	1.2	-	-	1.4	-
Built-in voltage (V)		0.6	2.8	2.9	-	4.9	-
Breakdown field (MV/cm)		0.3	2.2	3.3	-	5.6	-

2.2.2 Unlocking the Potential of SiC-Based MOS Power Devices

The summary of the achievements attained in the research and development of commercial SiC-based power devices was illustrated in Figure 2.1. Based on these achievements, SiC has garnered increasing attention in high-power semiconductor devices (Langpoklakpam *et al.*, 2022). Currently, with enhanced material quality and relatively advanced process technology, a multitude of SiC-based electrical products are available on the market. This encompasses bipolar junction transistors (BJTs), junction field effect transistor (JFET), Schottky diodes, and metal-oxide-semiconductor field effect transistor (MOSFET) from several reputable manufacturers.

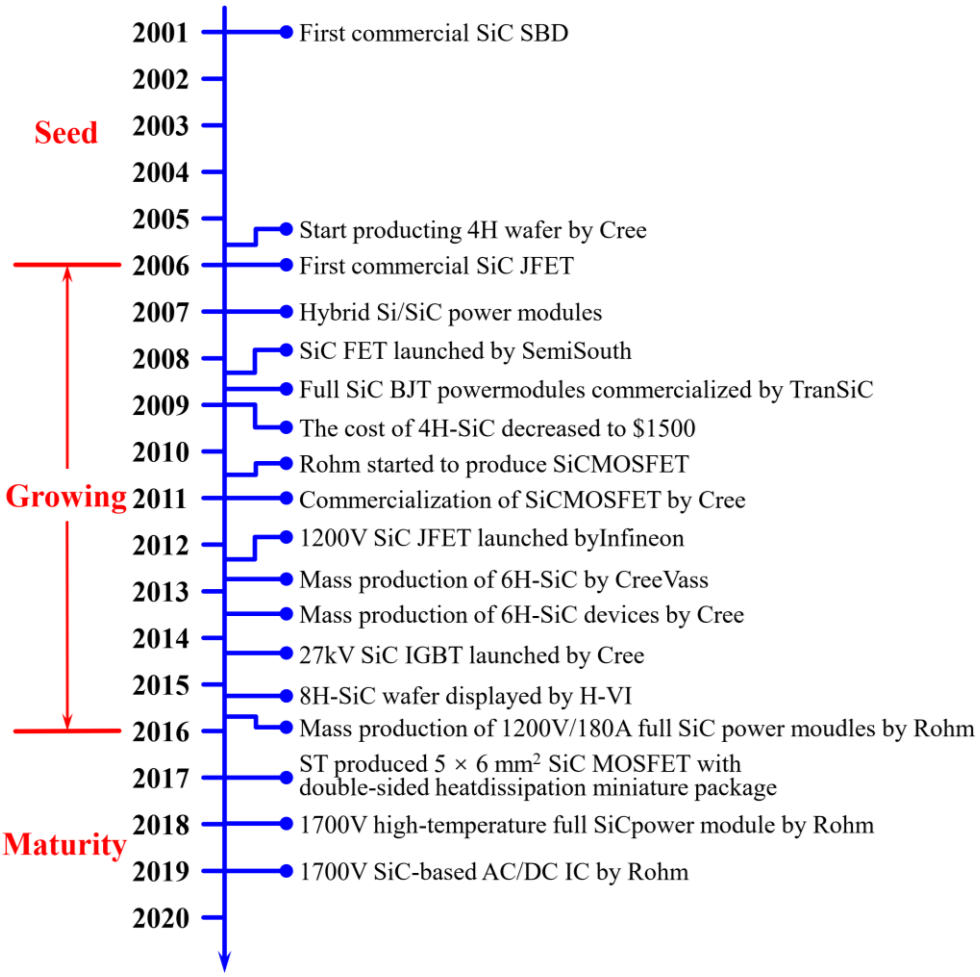

Figure 2.1 The milestones of the development process of SiC power electronic devices (Guo *et al.*, 2019).

Moreover, additional devices, such as insulated gate bipolar transistors (IGBT) and silicon carbide (SiC) light emitting diodes (LED) have also been created in the laboratory (Siddiqui *et al.*, 2021). In 2001, Infineon introduced the first commercial silicon carbide (SiC) Schottky barrier device, which features high blocking voltage and thermal stability. This technology can help power device manufacturers to develop new products (Friedrichs, 2006). Subsequently, the first SiC JFET, SiC BJT, SiC IGBT, SiC MOSFET and various other discrete devices and power modules have progressively entered commercial production (Xun *et al.*, 2017). Currently, some of the most widely used SiC-based power devices include Schottky diode with a voltage of 1.7 kV/25 A, discrete SiC MOSFET with a voltage of 1.7 kV/72 A, and SiC BJT module with a voltage of 1.7 kV/160 A (Yuan *et al.*, 2021). Companies, such as Infineon, Mitsubishi, ST, and ROHM have collectively accounted for over 80% of the market for this type of material (Yuan *et al.*, 2021).

Among these devices, SiC power MOSFET have been recognized as an ideal power switch, showing low on-resistance, minimal gate drive power, fast switching speed, and ability to endure high current and voltage applications concurrently without catastrophic failure (Barkhordarian, 1996). When comparing between the SiC-based power MOSFET with the Si-based power MOSFET, SiC-based power MOSFET exhibits a significantly lower specific conduction resistance ($R_{on,\ sp}$) than the Si counterparts, facilitating reduced parasitic capacitance and enhanced switching speed (She *et al.*, 2017). Thus, for a wide range of blocking voltages, a SiC-based power device can attain lower switching as well as conduction loss. (J. Wang *et al.*, 2008). Furthermore, at the operating temperature of 135°C, the on-resistance of SiC-based power MOSFET increases by 20%, but for Si-based power MOSFET, it surges by 250% (X. Li *et al.*, 2000). In 1987, the first depletion layer N-channel SiC MOSFET for high-

temperature application was created (Palmour *et al.*, 1987). Brown *et al.* later included a simulated operational amplifier (OPA) using depletion MOSFET, capable of functioning at 300°C (Palmour *et al.*, 1987). Purdue University announced a SiC CMOS digital integrated circuit in 2011 that could operate at temperatures up to 350°C. (Pengelly *et al.*, 2012). In the same year, Cree launched the first commercially available SiC MOSFET (Shepard, 2011). Later, ST successfully produced 5 × 6 mm^2 SiC MOSFET with double-sided heat dissipation miniature package in 2017. However, as the operation voltage and temperature continually increased, the reliability of SiC MOSFET devices at high pressures and temperatures was an increasing challenge (Wei *et al.*, 2023). The primary reliability concern issues of SiC MOSFET were degradation of the threshold voltage (Puschkarsky *et al.*, 2019), gate-oxide (PL) (Siddiqui *et al.*, 2021), and body diode (Agarwal *et al.*, 2007). Among these three reliability issues, the degradation of the PL was considered as a significant issue affecting the reliability of SiC MOS devices (Langpoklakpam *et al.*, 2022; Siddiqui *et al.*, 2021).

Significantly, the issues mentioned earlier could be evaluated by examining the MOS capacitor, a fundamental component of MOS devices, which served as the test structure in this study. The MOS capacitor would follow the same fabrication process as MOS devices, allowing for direct measurement and monitoring of their performance. Any improvements in processing that enhanced the electrical properties of the MOS capacitor would also benefit the MOS device (E. H. Nicollian *et al.*, 1982). Therefore, the simplicity and versatility of the MOS capacitor could be effectively utilized to improve integrated circuit processing (E. H. Nicollian *et al.*, 1982).

2.2.3 Material Properties of SiC

SiC is a Group IV-IV compound semiconductor made of 50% silicon and 50% carbon, discovered by Professor Jons Jakob Berzelius in 1823 at the Karolinska

Institute in Stockholm (Berzelius, 1824). The basic unit of a SiC crystal consists of a tetrahedral arrangement of four carbon atoms surrounding a central silicon atom (Figure 2.2 (a)). There is also a second type that is rotated 180° relative to the first (Figure 2.2 (b)). The carbon and silicon atoms are spaced 1.89 Å apart, while the distance between the carbon atoms is 3.08 Å, as illustrated in Figure 2.2 (a) (Jarrendahl *et al.*, 1998).

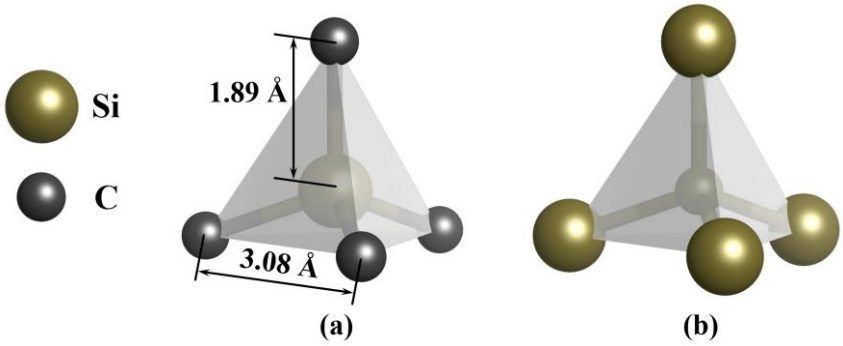

Figure 2.2 The building block of SiC crystals (Saddow *et al.*, 2004).

SiC is the only stable compound of carbon and silicon, with the stacking sequence of silicon and carbon atoms can ideally arrange into over 200 distinct crystallographic shapes, called polytypes (Harris, 1995). Each polytype exhibits specific material properties although the same atoms are used. Amongst the various polytypes, the most prevalent crystal structures are cubic and hexagonal. The former is referred to as α-SiC, such as 3C-SiC while the latter could be regarded as β-SiC, such as 4H and 6H-SiC. Figure 2.3 shows the stacking sequences of 3C-, 4H-, and 6H-SiC polytypes (Winkelmann *et al.*, 2004).

Table 2.2 compares the properties of SiC (three different polytypes) and Si at room temperature (M. B. J. Wijesundara *et al.*, 2011). It was noticed that generally all the SiC polytypes offer larger band gap, higher saturation electron velocity, higher E_B, higher thermal conductivity, and tremendously lower n_i compared with Si. Among the

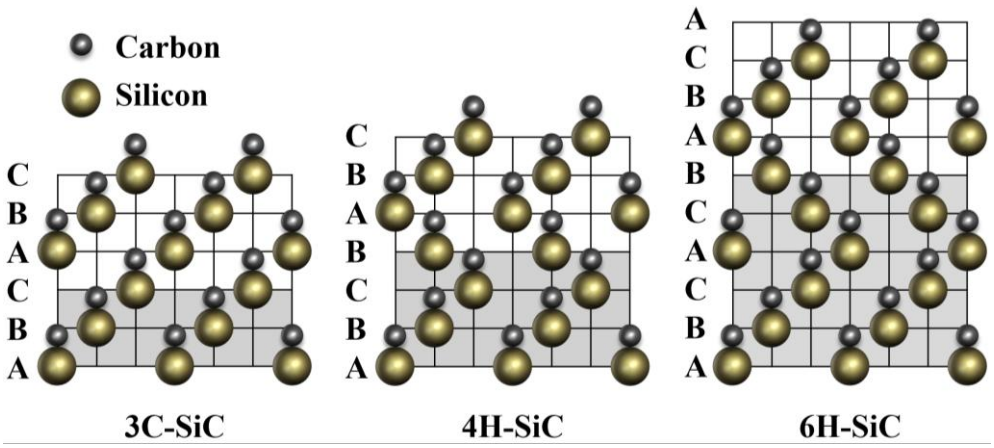

Figure 2.3 The stacking sequences of SiC polytypes: 3C-SiC, 4H-SiC, and 6H-SiC (Winkelmann *et al.*, 2004).

various polytypes, 4H-SiC and 6H-SiC are the most favored, particularly for device manufacturing, due to their ability to produce large wafers and their commercial availability (She *et al.*, 2017). Prior to 1994, 6H-SiC was the primary polytype until the introduction of 4H-SiC wafers. Since then, both polytypes have been utilized in research. In recent years, however, 4H-SiC has emerged as the dominant polytype, surpassing 6H-SiC polytypes that exhibit carrier mobility anisotropy in different planes due to the consistency of 4H-SiC carrier mobility in both planes. Therefore, 4H-SiC is the preferred material for devices used in high power, high temperature, and high-frequency applications by virtue of its high electron mobility (Palmour *et al.*, 1997), wider band gap (Itoh *et al.*, 1994), higher E_B (Konstantinov *et al.*, 1997), and shallower ionization energy of dopant compared to other materials (M. Wijesundara *et al.*, 2011). Additionally, single crystalline wafers of 4H-SiC are readily available (She *et al.*, 2017).

As shown in Table 2.2, compared to Si, the 4H-SiC has much wider E_g, together with its lower n_i would enable a high-temperature operation capability from a blocking stability point of view. This could be associated with the direct proportional

Table 2.2 Materials properties of Si, 3C-SiC, 4H-SiC, and 6H-SiC (Donato *et al.*, 2020; Idris, 2018; Langpoklakpam *et al.*, 2022).

Properties	Si	3C-SiC	4H-SiC	6H-SiC
Band gap (eV)	1.12 Indirect	2.36 Indirect	3.26 Indirect	3.02 Indirect
Melting point (K)	1687	3100	3100	3100
Electron mobility (cm^2/Vs)	1430	1000	1020 ⊥c-axis 1200 ∥c-axis	450 ⊥c-axis 100 ∥c-axis
Hole mobility (cm^2/Vs)	600	40	120	80
Intrinsic carrier concentration (cm^{-3})	10^{10}	10	10^{-7}	10^{-5}
Dielectric constant	11.80	9.72	9.76	9.66
Thermal conductivity (W/cm·K)	1.3	5.0	5.0	5.0
Breakdown field (MV/cm)	0.3	1.4	2.8	3.0
Saturated electron drift velocity ($\times 10^7$ cm/s)	1.0	2.5	2.7	2.0
Lattice constant (Å)	5.43	4.36	c-axis: 10 a-axis: 3	c-axis: 15 a-axis: 3

relationship of the n_i to $\exp(-E_g)$, and thus, a larger E_g gives a lower n_i for any temperature. Besides, SiC outperforms Si to be employed in conditions under which Si cannot adequately perform at temperature above 600°C because of the occurrence of a transition from extrinsic to intrinsic conduction at low temperature for Si (< 250°C) when compared with WBG semiconductors (> 600°C) (Kaminski *et al.*, 2014). Furthermore, the larger E_g of 4H-SiC also allows for a higher electric field operation across the device's drift region without avalanche multiplication of carriers, which

could be related to a higher impact ionization energy possessed by the 4H-SiC (Langpoklakpam *et al.*, 2022). Additionally, the ~10 times E_B in 4H-SiC with respect to Si makes ultra-high-voltage (>10 kV) power devices practically achievable (She *et al.*, 2017).

2.3 4H-SiC Surface Passivation by Silicon Dioxide (SiO_2)

One of the significant advantages that make SiC stand out from the crowd in MOS power devices is that SiC is the only compound semiconductor that has a natural and stable insulator called thermal oxidized silicon dioxide (SiO_2) (Deal *et al.*, 1965). This make the SiC-based devices to possess high compatibility with well-developed Si-based device technology (Cooper, 1997). SiO_2 could be thermally grown on SiC through oxidation, primarily due to the chemical affinity between the Si in SiC and oxygen (O_2), allowing a stable oxide layer to form (Song *et al.*, 2004). This process was analogous to the thermal oxidation of Si but presented unique challenges due to the presence of carbon in SiC (Shenoy *et al.*, 1995). Achieving an optimal SiO_2 layer would require precise control over temperature and growth conditions (Yin *et al.*, 2022). The modified Deal-Grove model, which was developed from the well-established Deal-Grove model for Si, has been utilized for the oxidization of SiC. It contained the out-diffusion and removal of carbon species through the oxide PL (Deal *et al.*, 1965; Song *et al.*, 2004). The detail oxidation process of SiC could be illustrated using the following chemical equation (Song *et al.*, 2004):

$$SiC + 1.5O_2 \rightarrow SiO_2 + CO \qquad (2.1)$$

The thermal growth of SiO_2 on 4H-SiC typically occurred at elevated temperatures ranging from 800 to 1300ºC in the presence of various ambient (D. Cho

et al., 2017; Kikuchi *et al.*, 2014; Kurimoto *et al.*, 2006). The temperatures facilitated the reaction between oxygen and the silicon component of 4H-SiC, while carbon was either incorporated into the oxide layer or escaped as carbon monoxide (CO) gas (Song *et al.*, 2004). The oxidation product of 4H-SiC, influenced by the carbon content, was comprised of oxides of silicon and carbon (SiC_xO_y), with the concentration of SiC_xO_y diminishing as the oxidation temperature rose (Kurimoto *et al.*, 2006). Therefore, to optimize the efficacy of 4H-SiC in power device applications, it is essential to implement more stringent thermal oxidation and annealing processes to eliminate as much carbon as possible from the PL, with the oxide formed at 1300ºC being comparable to Si-oxidized SiO_2 (Song *et al.*, 2004). Initially, it was discovered that carbon atoms and near-interfacial traps (NITs) were responsible for the distribution of electrically active defect states at the 4H-SiC/SiO_2 interface for the 4H-SiC (Afanasev *et al.*, 1997). However, a number of studies conducted by using microstructural and nano chemical analyses indicated that the NITs were not produced from the graphitic regions or carbon clusters found in the 4H-SiC/SiO_2 interlayer. Instead, they were caused by intrinsic defects. These included V_o and defects extending from the interface to the oxide layer, as corroborated by the Ab-initio theoretical study (Okuno *et al.*, 2009; Pippel *et al.*, 2005). Additionally, defects such as Si interstitials and Si dangling bonds could also be found at the interface (Chung *et al.*, 2000). Due to the presence of these defects, the interface trap density for the SiO_2 thermally grown on 4H-SiC was significantly higher (approximately two orders of magnitude) than that on Si. This resulted in an increase in the channel resistance and a decrease in the mobility of the channel (Cooper, 1997).

2.3.1 Post-Oxide Annealing on 4H-SiC/SiO_2 MOS Capacitors

To minimize the concentration of the abovementioned defects, post-oxide

annealing (POA) techniques have been employed to passivate the traps in 4H-SiC/SiO_2 system (Fiorenza and Giannazzo, 2019). Various ambient utilizing oxygen (O_2), argon (Ar), hydrogen (H_2), nitrogen (N_2), ozone (O_3), nitric oxide (NO and N_2O), phosphoryl chloride ($POCl_3$), boron nitride (BN), and forming gas as the sources for the POA process carried out in a temperature range from 400 to 1300^oC (Fiorenza and Giannazzo, 2019). Table 2.3 lists the different conditions for POA of 4H-SiC/SiO_2 as well as the key findings obtained. It was reported that the SiO_2 grown by wet oxidation exhibited superior MOS characteristics compared to dry oxidation, particularly on the C-face of 4H-SiC (Hijikata *et al.*, 2006; Maeda *et al.*, 1988; Palmieri *et al.*, 2008). The investigation into the effects of different oxidation process on MOS characteristics using photoelectron spectra revealed that the small areal density of the compositional transition states during wet oxidation contributed to the favorable electrical characteristics of MOS devices on the 4H-SiC (Hijikata *et al.*, 2006). Furthermore, wet oxidation was demonstrated to significantly diminish interface stress and mitigated the formation of carbon-related defects that typically accumulated at the 4H-SiC/SiO_2 interface during dry oxidation (Indari *et al.*, 2019). This led to improved electrical properties, particularly in reducing gate leakage current (Hijikata *et al.*, 2006; Indari *et al.*, 2019). Subsequent research revealed that the nitridation by NO or N_2O by introducing small amount of nitrogen at the MOS interface was reported to not only diminish the overall traps density but also improving leakage properties of the PL (Gutt *et al.*, 2014). In order to incorporate more nitrogen into the PL, the plasma enhanced and low-pressure chemical vapor deposition (PECVD and LPCVD) methods were employed to deposit nitrogen oxide (SiON) as PL on 4H-SiC (D. Cho *et al.*, 2017; Iwasaki *et al.*, 2009). However, the SiON grown by PECVD and LPCVD would typically result in higher interface state density (D_{it}) and effective oxide charge (Q_{eff})

(D. Cho *et al.*, 2017; Iwasaki *et al.*, 2009).

Reports suggested that POA in Ar ambient followed by a wet O_2 1150°C for 3 hours could reverse the Q_{eff} of the 4H-SiC based MOS capacitor from 5.0×10^{11} to -17.0×10^{11} cm^{-2}, indicating the POA in O_2 ambient substantially influenced deep acceptor-type interface states and negative fixed charges in 4H-SiC based MOS capacitor (Yano *et al.*, 1999). In addition, a 30-min POA at 1000°C in hydrogen ambient was employed to enhance the performance of 4H-SiC/SiO_2 MOS capacitor by neutralizing the Si dangling bonds, which resulted in a decrease in D_{it} (at E_c-E_t = 0.4 eV) from 3.4×10^{12} to 9.8×10^{11} cm^{-2} eV^{-1} and a reduction in flat band voltage (V_{FB}) from 15.7 to 1.1 V (Fukuda *et al.*, 1999). Moreover, the secondary ion mass spectrometer (SIMS) analysis revealed that hydrogen accumulated at the interface and terminated the Si and C dangling bonds (Fukuda *et al.*, 1999). However, the subsequent investigation of conductance-voltage (*G*-*V*) results has indicated that hydrogenation of dangling bonds, as proposed by Fukuda *et al.* (Fukuda *et al.*, 1999), was not the dominant. Instead, it has been found that carbon clusters were the main contributor to D_{it} within the SiC band gap (Pensl *et al.*, 2001). Furthermore, the attempt was made to improve performance of the 4H-SiC/SiO_2 MOS capacitor by using NO annealing, where 1h POA at 1150°C have resulted in the reduction of D_{it} (at E_c-E_t = 0.4 eV) from 9.2×10^{12} to 3.0×10^{11} cm^{-2} eV^{-1} (Chung *et al.*, 2000). This decrease was attributed to the incorporation of nitrogen ions into PL and their formation of chemical bonds with silicon, carbon, and carbon clusters during the annealing process in NO ambient (Chung *et al.*, 2000).

Additionally, a comparison of the effect of POA in NH_3, N_2, and N_2O ambient has revealed that NH_3 was superior in eliminating the interface traps (Soejima *et al.*, 2013). Further cross-sectional transmission electron microscope (TEM) analysis has

shown the POA in NH_3 ambient demonstrated a lower interfacial roughness than in N_2 and N_2O (Soejima *et al.*, 2013). Furthermore, the POA in $POCl_3$ has demonstrated an excellent effect on the 4H-SiC/SiO_2 interface by reducing the shallow interface traps, where $POCl_3$ annealing at 1000ºC could significantly reduce the D_{it} (at E_c-E_t = 0.2 eV) from 1×10^{12} to 9×10^{10} cm^{-2} eV^{-1}, which was much lower than 4×10^{11} cm^{-2} eV^{-1} for that annealed in NO ambient at 1200ºC (Okamoto *et al.*, 2010). Subsequent research has revealed that the incorporation of phosphor by the POA in phosphorus pentoxide (P_2O_5) ambient has converted the entire SiO_2 PL to phophosilicate glass, which in turn demonstrated a lower D_{it} due to the efficient phosphorous passivation of threefold coordinated carbon atoms at the interface, while a higher leakage current was observed for the 4H-SiC/SiO_2 subjected POA in P_2O_5 compared to a in NO ambient (Sharma *et al.*, 2012). Furthermore, the boron (B) was incorporated into SiO_2 by POA on a planar diffusion source composed of boron nitride (BN) and 3.5-6.5% boric oxide (B_2O_3) (Okamoto *et al.*, 2014). The SIMS result indicated that B accumulated near the 4H-SiC/SiO_2 interface and resulted in stress relaxation, and thus, D_{it} (3.0×10^9 cm^{-2} eV^{-1} at E_c-E_t = 0.4 eV) was three orders of magnitude lower than that without boron (1.1×10^{12} cm^{-2} eV^{-1}) (Okamoto *et al.*, 2014). Subsequent study demonstrated the ability of the boron on reducing D_{it} and NITs, where a similar lower D_{it} of 3.9×10^9 cm^{-2} eV^{-1} was attained for 4H-SiC/SiO_2 interface POA at 1150ºC (Cabello *et al.*, 2017).

Furthermore, a higher E_B of 11.3 MV/cm was attained for the SiO_2 POA in N_2O at 1150ºC when compared with E_B of 10.7 MV/cm that POA in $POCl_3$ (Fiorenza *et al.*, 2014). The detrimental effect of the incorporation of the phosphorus in thermal oxidized SiO_2 was verified by the reduction of E_B from 10.0 to 8.7 MV/cm after phosphorus implantations (Mikhaylov *et al.*, 2015). Further research has revealed that the 4H-SiC/SiO_2 MOS capacitor thermal oxidized in N_2O and POA in dry oxygen

ambient demonstrated an E_B of 11.8 MV/cm (D. Cho *et al.*, 2017). The recent research showed that the E_B of the thermal oxidized 4H-SiC/SiO_2 MOS capacitor was significantly improved by POA in electron cyclotron resonance (ECR) ozone (O_3) plasma ambient (E_B = 12.1 MV/cm) (Yin *et al.*, 2022). As a whole, it was revealed that nitrided SiO_2 exhibited superior MOS characteristics compared to SiO_2 annealed in other ambient, especially in NO ambient (Puschkarsky *et al.*, 2019). The NO annealing could significantly decrease the defect concentration in the PL and the interface with 4H-SiC (D_{it} of 5.5×10^{10} eV^{-1} cm^{-2}, Q_{eff} of 9.0×10^{10} cm^{-2}) (Chinone *et al.*, 2017; Jamet *et al.*, 2001), which was crucial for improving channel mobility in 4H-SiC based MOS devices (Langpoklakpam *et al.*, 2022). Furthermore, nitrided SiO_2 was also the most commonly used PL for 4H-SiC based MOS devices in industrial manufacture (Langpoklakpam *et al.*, 2022).

Table 2.3 Various parameters of thermal oxidized SiO_2 on 4H-SiC substrate in previous literatures.

Reference	Deposition Method	POA	D_{it} at E_c-E_t= 0.4 eV (eV^{-1} cm^{-2})	ΔV_{FB} or Q_{eff} (V or cm^{-2})	E_B (MV/cm)
(Afanasev *et al.*, 1997)	Dry O_2 SiO_2	Ar 1120-1150°C	1.3×10^{12}	-	-
(Yano *et al.*, 1999)		Ar 1150°C 30min	-	5.0×10^{11}	-
(Fukuda *et al.*, 1999)		H_2 1000°C	9.8×10^{11}	ΔV_{FB}=3.5V	-
(Prez-Tomás *et al.*, 2009) (Kikuchi *et al.*, 2014)		O_2 800-1050°C	3.1×10^{10}- 1.3×10^{11}	5.7×10^{11}	-
(Okamoto *et al.*, 2010)		$POCl_3$ 900-1000°C	9.0×10^{10}- 1.0×10^{12}	(-2.0×10^{10})- 4.0×10^{11}	-
(Jamet *et al.*, 2001) (Chinone *et al.*, 2017)		NO 1150°C	5.5×10^{10}- 2.0×10^{12}	9.0×10^{10}- 3.0×10^{11}	-
(D. Cho *et al.*, 2017)		10 % N_2O in N_2 1200°C	2.5×10^{11} E_c-0.2eV	2.97×10^{11}	10.1
(Okamoto *et al.*, 2017)		BN 950°C	3.0×10^{9}	-	-
(Iwasaki *et al.*, 2009)		N_2/H_2 400°C	3.1×10^{11}- 5.1×10^{12}	-	-
(Yano *et al.*, 1999)	Wet O_2 SiO_2	Wet O_2 1150°C	-	-1.5×10^{12}	-
		Ar 1150°C	-4.0×10^{11}	-	-
(Chung *et al.*, 2000)		NO 1150°C	3.0×10^{11}	-	-
(Palmieri *et al.*, 2008)		Ar 1120°C	1.4×10^{10}	5.9×10^{11}	10.0
		Wet N_2 1120°C	7.0×10^{11}	8.0×10^{11}	-
(Chinone *et al.*, 2017)		H_2	$<1.0\times10^{10}$	-	-

Table 2.3 (Continued).

Reference	Deposition Method	POA	D_{it} at E_c-E_t= 0.4 eV (eV^{-1} cm^{-2})	ΔV_{FB} or Q_{eff} (V or cm^{-2})	E_B (MV/cm)
(Jamet *et al.*, 2001)	NO-Nitrided SiO_2	N_2 1150°C	1.6×10^{11}	-	-
(Fiorenza *et al.*, 2014) (Swanson *et al.*, 2012)	PECVD SiO_2	N_2O 1150°C	1.8×10^{12} E_c-0.2eV	-	11.3
		$POCl_3$ 1000°C	5.7×10^{11} E_c-0.2eV	-	10.7
(Iwasaki *et al.*, 2009)	PECVD SiON	N_2/H_2 400°C	1.7×10^{11}- 3.1×10^{11}	ΔV_{FB}=5.26-7.43V	-
(D. Cho *et al.*, 2017)	LPCVD SiON	Dry O_2 1200°C	7.0×10^{10} E_c-0.2eV	1.29×10^{11}	11.8
		Wet O_2 1200°C	6.0×10^{10} E_c-0.2eV	6.9×10^{11}	11.3