HIGH EFFICIENCY AND HIGH PSRR CMOS MULTI-VOLTAGE DOMAIN BUCK INTEGRATED LOW DROPOUT REGULATOR

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by

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LIST OF ABBREVIATIONS

5G	Fifth Generation
AI	Artificial Intelligent
ATBGR	Auto-trimming bandgap reference
BGR	Bandgap Reference
CMOS	Complementary Metal-Oxide Semiconductor
CTAT	Complementary to absolute temperature
DEMUX	De-multiplexer
FOM	Figure of Merit
IoT	Internet of things
LDO	Low Dropout Regulator
MVD	Multi-voltage domain
PMU	Power Management Unit
PTAT	Proportional to absolute temperature
PSRR	Power Supply Rejection Ratio
RFEH	Radio Frequency Energy Harvester
SoC	System on Chip
TC	Temperature Coefficient
WSN	Wireless Sensor Node

LIST OF APPENDICES

PENGAWAL SELIA TURUN BERSEPADU DENGAN PENGAWAL SELIA KECICIRAN RENDAH DOMAIN VOLTAN PELBAGAI CMOS BERKEMAMPUAN TINGGI DAN PSRR TINGGI

ABSTRAK

Pengatur kuasa penting untuk memastikan output stabil dalam sistem elektronik dengan mengawal voltan. Pengatur linear seperti pengawal selia keciciran rendah , Pengatur Linear Tetap, dan Pengatur pengalih digunakan untuk mengekalkan voltan stabil dalam aplikasi seperti RF, litar audio, dan sistem analog ketepatan. Pengatur pensuisan seperti Penukar Buck dan Boost pula digunakan untuk menukar voltan dengan cekap, sesuai untuk bekalan kuasa dengan sensitiviti bunyi yang lebih rendah. Dalam kajian ini, pengatur pengawal selia turun-pengawal selia keciciran rendah bersepadu multi-voltan (MVD) yang cekap tinggi dicadangkan. MVD Buck-pengawal selia keciciran rendah beroperasi pada voltan 4.0 V dan mengatur empat domain voltan (1.8 V hingga 3.0 V) dengan kecekapan 85.24%. Reka bentuk ini menggunakan pengawal demultipleks yang hanya memerlukan 42 nW kuasa, serta satu induktor dan kapasitor. Penjana jam 500 KHz dan rujukan bandgap 1.25 V digunakan untuk menyokong fungsi pengawal selia turun dan pengawal selia keciciran rendah. Skim pampasan digunakan untuk memastikan kestabilan sistem walaupun beban berubah-ubah. MVD Buck-pengawal selia keciciran rendah menunjukkan peraturan garisan dan beban yang baik serta nisbah penolakan bekalan kuasa (PSRR) yang tinggi pada pelbagai frekuensi. Reka bentuk ini sesuai untuk litar RF dalam meter kuasa RF mudah alih dan aplikasi sensitif lain.

HIGH EFFICIENCY AND HIGH PSRR CMOS MULTI-VOLTAGE DOMAIN BUCK INTEGRATED LOW DROPOUT REGULATOR

ABSTRACT

Power regulators are essential in ensuring stable output for electronic systems by controlling voltage levels. Linear regulators, such as Low Dropout (LDO) Regulators, Fixed Linear Regulators, and Shunt Regulators, adjust resistance to maintain stable voltages, commonly used in RF applications, audio circuits, and precision analog systems. Switching regulators, including Buck and Boost Converters, efficiently convert voltage by rapidly switching a transistor, typically used in power supplies where noise sensitivity is lower. In this work, a high-efficiency multi-voltage domain (MVD) integrated buck-LDO regulator with a combined compensation scheme is proposed. The MVD Buck-LDO operates with a 4.0 V supply headroom and regulates four voltage domains (1.8 V to 3.0 V) with an efficiency of 85.24%. An integrated demultiplexer controller consumes just 42 nW. The design minimizes external components, requiring only a single inductor and capacitor, with a 500 KHz clock generator. A single 1.25 V bandgap reference supports both buck and LDO functions. Reverse nested Miller and Type II compensation schemes ensure system stability under varying load conditions. The MVD Buck-LDO demonstrates strong line and load regulation, with 0.428 mV/V and 0.0005 mV/mA in the low voltage domain, and 0.481 mV/V and 0.079 mV/mA in the high voltage domain. Its power supply rejection ratio (PSRR) reaches 80 dB at low frequencies, 53 dB at mid frequencies, and 79 dB at high frequencies. This design provides an efficient and compact power regulation solution, particularly suited for RF circuits in handheld RF power meters and other sensitive applications.

CHAPTER 1

INTRODUCTION

1.1 Background

Electronic device battery life is greatly increased by the use of efficient power regulators. By managing and regulating the voltage applied to various device components, these parts guarantee dependable and efficient operation. The longevity of a device's battery is directly impacted by the efficiency of these regulators, which also affects total energy usage. The imperative demand for longer battery life in portable devices has led to a recent and revolutionary change in power regulator design and application. This transition is driven by cutting-edge technology like highly integrated Power Management Integrated Circuits (PMICs) and complex load balancing strategies. In addition to addressing today's energy issues, more efficient power regulation holds the key to extended battery life, which will have a substantial impact on how convenient and useful electronic gadgets are in general for daily use.

The issues of power management in wearable technology are unique. Because wearables are becoming more and more popular, power management becomes even more important as wearables focus on tracking health and lifestyle. Fitbits and other wearable electronics are compact and typically run on a single little battery [1]. This complicates the task of striking the ideal balance between functionality and battery usage. Managing power in wearables entails solving issues including battery space constraints, real-time monitoring capabilities, and user convenience in order to make sure the devices function properly while extending the battery's life [2]. Cutting-edge solutions for power management are essential as wearables becoming increasingly complex in order to solve these issues and guarantee a satisfying user.

In the ever-evolving field of integrated circuits, System on Chip (SoC) technology requires effective power management. With the increasing demands of contemporary computing, SoC designs are evolving to accommodate more complex power management requirements. With so many features packed onto a single chip, SoC devices need to achieve a compromise between power efficiency and great performance. Finding the ideal balance between efficient device operation and prudent energy use has been the main emphasis of power management in SoC history [3]-[4]. To improve the overall energy efficiency of SoC devices, researchers have focused on developing sophisticated power-gating algorithms, dynamic voltage and frequency scaling, and power-efficient design methodologies. Even while SoC technology is still a vital component of many devices, research into more sophisticated power management techniques is necessary to solve environmental issues and reasonable power consumption constraints [5].

In the world of modern computing, artificial intelligence (AI) power management is essential. As artificial intelligence (AI) capabilities, such as deep neural networks and learning tasks, develop, efficient power management becomes more crucial. High-performance computation and prudent energy utilization have always been balanced in the history of power management in artificial intelligence [6]. In order to minimize the energy footprint of AI models, researchers have created more intelligent hardware designs, improved algorithms, and optimization techniques. Further research into power management is necessary to address environmental concerns and realistic power consumption restrictions as AI continues to play a prominent role in a variety of applications.

Wireless Sensor Networks (WSN) power management poses special difficulties. Ensuring effective power usage is essential since WSNs are utilized in many different contexts. The tiny sensor nodes, which are frequently positioned in isolated areas, depend on batteries for a long time [7]. The difficulty is striking the ideal balance between extended battery life and maximum gadget capability. As networks get larger, researchers have been working on creative ways to reduce the amount of power used by sensor nodes. These methods have addressed issues with data throughput, communication range, and power efficiency. The increasing integration of WSNs in diverse applications has led to the need for developing ways to address obstacles and improve the efficiency of power management [8].

Because IoT technologies are used in a variety of ways, power management in the Internet of Things (IoT) presents a unique set of issues. An essential aspect of everyday life for IoT devices is efficient power management [9]. The diversity of Internet of Things devices, ranging from industrial sensors to smart home devices, makes it difficult to discover universal power management solutions [10]. The limited operating settings in which many IoT devices function make it more difficult to guarantee extended device lifespans. To solve scaling difficulties, researchers concentrate on creating standardized, energy-efficient communication protocols and optimizing power usage in devices with limited resources. Researchers and engineers continue to place a high priority on coming up with creative solutions to power management problems as the Internet of Things expands.

With the growing need for more environmentally friendly transportation, managing electricity in electric vehicles (EVs) presents special difficulties. Energy optimization is difficult with EVs since they run on battery power. Complexity to power management is added when driving range is balanced with battery capacity, weight, and charging system. Thermal management and battery deterioration are two issues that come with fast-charging systems [11]. Sustaining optimal performance and extended battery life requires ongoing work to improve battery technology, provide intelligent charging infrastructure, and improve power management techniques.

The dramatic advances in wireless technology present special challenges when it comes to handling power in 5G applications. 5G is going to change a lot of businesses as people want faster and more dependable connectivity. 5G's sophisticated network architecture and faster data transmission rates make efficient power management essential. Figure 1.1 illustrates LDO implementation in a 5G battery-powered system [12]. Here, the dynamic supply level scaling scheme is used in the Power Management Integrated Circuit (PMIC) unit to sustain the battery life for longer.

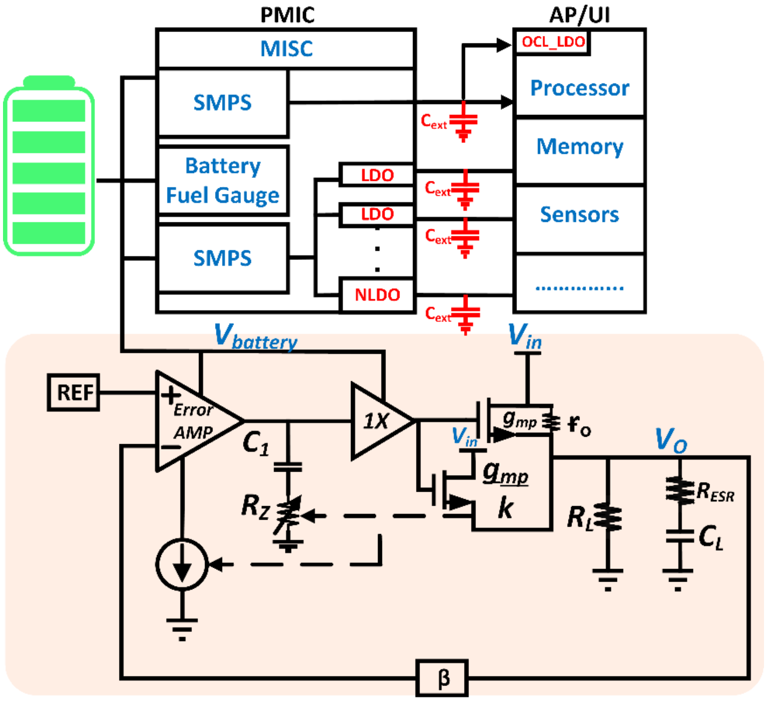

Figure 1.1 Implementation of LDO in 5G battery-powered system [12]

The landscape of power management is made more complex by the need to balance energy consumption and high-performance connection in several tiny cells and power-hungry devices. To overcome obstacles in this fast-paced industry, researchers concentrate on creating communication protocols that use less energy and optimising power usage. In order to ensure smooth and sustainable operation as 5G continues to revolutionise communication, creative solutions to power management issues are still essential.

The market provides a variety of advanced power regulators that are intended to solve particular problems and maximise energy efficiency in response to the numerous power management challenges that have been described in different fields. For example, Low Dropout Regulators (LDOs) are essential for maintaining consistent and optimal performance in electronic devices because they regulate voltage with low dropout, which prolongs battery life. Buck regulators effectively reduce voltage, achieving a delicate balance between performance and power consumption in wearables with constrained battery capacity. In order to improve overall efficiency and solve energy issues, Power Management Integrated Circuits (PMICs) are a cutting-edge technology that incorporate sophisticated features like voltage regulation and load balancing. Collectively, these various power regulators support continuous initiatives to extend battery life, improve energy efficiency and guarantee the long-term operation of electronic devices in a wide range of applications.

1.2 Problem Statement

In electrical systems, fine-grained power distribution is frequently achieved through the use of multi-voltage domains, where Power Management Units (PMUs) have been employed in System-on-Chip (SoC) designs to manage these domains for powering different load circuits [13]. In Internet of Things (IoT) applications, such as wearables, sensors, and RF transceivers, multiple voltage domains are used to improve power efficiency and extend battery life [14]. These systems require components like sensors, a CPU, and an RF transceiver to be powered within a multi-voltage domain, enabling optimized energy consumption [14]. In wireless sensor nodes (WSNs), which comprise transmitters, power units, processing units, and sensing units, advanced power management solutions are crucial for prolonging battery life while data is continuously monitored and transmitted to processing units [15]-[16]. Each component in the WSN operates within its own voltage domain, necessitating the development of multi-voltage domain regulators with high efficiency to support various voltage levels and enhance system performance.

To meet the requirements of applications operating at high frequencies, such as medical equipment and RF communication systems, the reduction of noise interference, which can degrade performance and reliability, is essential. Multi-voltage regulators with high Power Supply Rejection Ratios (PSRR) across wide frequency ranges are needed to minimize noise coupling [17]. Traditional multi-voltage regulators face limitations, such as switching noise and cross-regulation, which have prompted the adoption of alternative solutions. These include single-inductor multiple-output (SIMO) DC-DC converters and independent Low Drop-Out (LDO) regulators, which offer cleaner power with minimal ripple [17]- [18]. In applications like RF communication, fluctuations in load, driven by varying signal strengths, modulation techniques, and transmission conditions, demand low-ripple, well-regulated multi-voltage domain power supplies [17].

Microcontrollers further require dynamic voltage scaling, where the supply voltage must be adjusted according to system frequency [19]. For instance, lower voltages are used when flash memory programming is unnecessary, while higher voltages are required when it is [20]. This exemplifies the need for adaptable power solutions that respond to varying voltage requirements. Device-level applications, such as Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs), similarly depend on multiple voltage domains for proper operation [21]. Though a PMU provides a feasible solution, in IoT applications with infrequent monitoring—such as industrial temperature sensing or remote heart rate monitoring—the PMU may become less relevant due to the wireless sensor staying idle for extended periods [16].

Moreover, power management solutions face significant challenges at sub-250 nm technology nodes. Limitations like restricted bandwidth, low DC gain (typically in the range of 50–100 for 250 nm and decreasing further at smaller nodes), and finite output conductance of pass transistors have hindered traditional LDO regulators' ability to provide high PSRR, particularly under increasing operating frequencies [22]. Innovative regulator topologies, such as LDOs with programmable output voltages and enhanced PSRR, are needed to address these issues, while providing efficient power management, noise suppression, and voltage scalability [21]-[23]. Time-division multiplexing and other complex controller architectures have been proposed to manage numerous voltage domains, though they introduce complexity and require more silicon area [24].

The integration of power management systems into SoC solutions has driven the development of switching converters with higher operating frequencies, where the increased frequency of output ripples poses new challenges for ensuring high PSRR [25]. On-chip LDO (OCL-LDO) designs aim to minimize parasitic components, but meeting fast transient response demands often requires high current consumption [26]-[27]. The balance between bandwidth, gain, load response, and stability in LDO design is vital, as trade-offs can affect PSR, transient response, and overall efficiency [22]. Recent innovations, such as adaptive power transistors, have been introduced to optimize load distribution and preserve stability under high loads, though these techniques often require high quiescent current, making them less suitable for low-power designs [28].

Thus, further research is required to develop regulator topologies that can effectively address the challenges associated with multi-voltage domains, load regulation, and voltage scalability, while ensuring stability, efficiency, and compactness in power management for SoC designs. These advancements are critical to the ongoing integration of power supply systems into SoC architectures, where optimized power solutions are essential for high-performance applications, including medical devices and IoT systems.

1.3 Research Objectives

The following are the main objectives of this research:

I. Design a streamlined controlling mechanism of Multi-Voltage Domain Buck-LDO regulator in180 nm CMOS technology with the target of achieving a minimum power efficiency of 80% across all four multi-voltage domains.

II. Design a regulator that maintains a maximum Power Supply Rejection Ratio (PSRR) of 50 dB throughout a broad frequency range (10 Hz to 100 MHz) without compromising system stability.

III. Design a regulator to maintain output ripple below 20 mV and load regulation below 0.01 mV/mA across all four multi-voltage domains, ensuring stable and reliable output performance.

1.4 Research Scope

This research is focused on the design and development of a high-efficiency, high-PSRR CMOS Multi-Voltage Domain (MVD) Buck-LDO regulator in 180nm CMOS technology, addressing challenges in power management across multi-voltage domains. The MVD Buck-LDO regulator is designed to operate across four distinct voltage domains (1.8 V to 3.0 V) with a minimum efficiency of 80%. A streamlined controlling mechanism is integrated to enhance power efficiency and reduce power consumption across all voltage domains.

A PSRR of at least 50 dB is targeted across a broad frequency range (10 Hz to 100 MHz) by incorporating compensation techniques such as reverse nested Miller and Type II schemes, ensuring stability under varying load conditions. Output ripple is minimized to below 20 mV, and load regulation is maintained at less than 0.01

mV/mA across all voltage domains. Robust line and load regulation is ensured to meet the demands of high-frequency and noise-sensitive applications, such as RF communication systems and medical devices.

External components are minimized by employing a single inductor and capacitor design, supported by a 500 kHz clock generator and a 1.25 V bandgap reference shared between the buck and LDO functions. Silicon area is optimized, and design complexity is reduced to enable integration into System-on-Chip (SoC) architectures. The regulator is tailored for multi-voltage domain applications, including Wireless Sensor Networks (WSN), Internet of Things (IoT) devices, SoCs, and other power-sensitive systems, with adaptability ensured for use in wearable devices, RF transceivers, analog systems, and medical devices.

Critical limitations of traditional power management solutions, such as restricted bandwidth, low DC gain, and finite output conductance, are addressed through the proposed innovative regulator topology. This work aims to provide a compact, energy-efficient, and reliable power management solution for a wide range of modern electronic applications.

1.5 Research Contribution

The purpose of this project is to contribute to the development of a power solution needed for multi-voltage domains, which could be specific to the applications stated below: WSN, SoC, and Internet of Things. The employment of a single-chip Multi-Voltage Domain (MVD) Buck-LDO regulator permit for the control of the regulator through a microcontroller, FPGA, and manual means, thereby achieving higher power efficiency. The encouragement for the adoption of this power solution in radio frequency, audio systems, Analog-to-Digital Converters, Digital-to-Analog

Converters, Medical Devices, sensor interfaces, and numerous other applications is driven by the high-power supply rejection ratio and power efficiency exhibited by the regulator.

1.6 Thesis Outline

The thesis is organized as follows in order to actualize the desired objectives and the planned structure for this study:

A thorough review of the research on low dropout regulators (LDOs) is covered in depth in Chapter 2. In-depth discussions and analyses of multiple topologies targeted at improving the power supply rejection ratio, transient response, load current, and power efficiency of LDOs are provided in this section. Following an in-depth review of the literature on Buck regulators, the advantages, and shortcomings of the LDO are contrasted with those of the regulator. The architectures of LDOs, Bucks, and combined Buck-LDOs are explored as well in this chapter. This section summarizes the study and findings about the common bandgap reference adopted in both LDOs and Buck regulators.

In Chapter 3, the process for achieving high power efficiency in the Multi Voltage Domain Buck-LDO regulator is described in detail. This section includes a comprehensive theoretical analysis of the MVD Buck-LDO regulator at the block level, including elements like the Low Dropout regulator, demultiplexer, bandgap reference (BGR), and Buck regulator. The simulation results of each block are given in detail, showcasing the features and performance of specific parts. The integrated architecture of the multi-voltage domain Buck-LDO regulator is revealed in this chapter, along with detailed design information, after the block level simulation validation was successful. Furthermore, the chapter provides a brief overview and explanation of the measurement setups used in the subsequent validation procedures.

In Chapter 4, the multi-voltage domain Buck-LDO regulator's measurement findings are presented, with an emphasis on the regulator's high PSRR and high efficiency. The part first makes use of the bandgap reference's measurement data. The MVD Buck regulator's measurement results are next shown, and finally, the integrated MVD Buck-LDO analysis is shown. As an additional visual aid for understanding the implemented architecture, the layout and micrograph of the fabricated chip for the proposed design are also presented.

The conclusions derived from the research findings are briefly reviewed in Chapter 5, providing a clear summary of the key findings and results. In addition, future work proposals are presented, outlining possible directions for investigation and development in the subject in light of the research findings and areas that need improvement.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Voltage regulator is widely used in power management unit because it is able to provide constant and stable supply to the system. Selecting the right regulator is important when designing the PMU. Linear regulators and switching regulators has its own good and bad. The advantages of the linear regulator over switching regultor is that it have higher power supply rejection ratio, less external component needed and ease to integrated in SoC application [29]-[30], low ripple voltage [31]-[32], standby current is low as no switching operation take place [33] and low-noise power supply along the PCB traces and also flat flex cable [34]-[35]. The trade off of the linear regulator is low power efficiency which can only be used for step down the voltage and it dissipates more heat.

The LDO and DC-DC switching regulator architectures have been covered in this chapter initially. The literature on power efficiency, power supply rejection ratio and stability for both switching regulators and LDOs has subsequently been reviewed. Following is a list of the differences between the two regulators.

2.1.1 Architecture of Low Dropout Regulator (LDO)

A subset of linear regulator, which is the LDO is capable to contribute a moderate power efficiency. But compare to switching regulator, LDO is still struggling to perform in terms of power efficiency. By reducing the voltage drop between input over output voltage, the power efficiency of the LDO getting better. Huge voltage dropout variation between input to output of LDO will cause for poor power efficiency.

Switching regulator has its own advantages such as high power efficiency, low heat dissipation and able to step up and step down the voltage. Eventhough switching regulator carry many benefit, but designers like to go with linear regulator for embedded circuit. This is because of its lower noise, higher PSRR and simple circuit. Eventhough power efficiency is an important factor, various research are still ongoing to improve the performance of a linear regulator. Low dropout voltage regulator is one of linear regulator which widely used in embedded products.

Figure 2.1 shows the conventional LDO regulator which consists of a bandgap reference to generate voltage reference, an error amplifier, a PMOS transistor used as pass element, and a feedback network resistor.

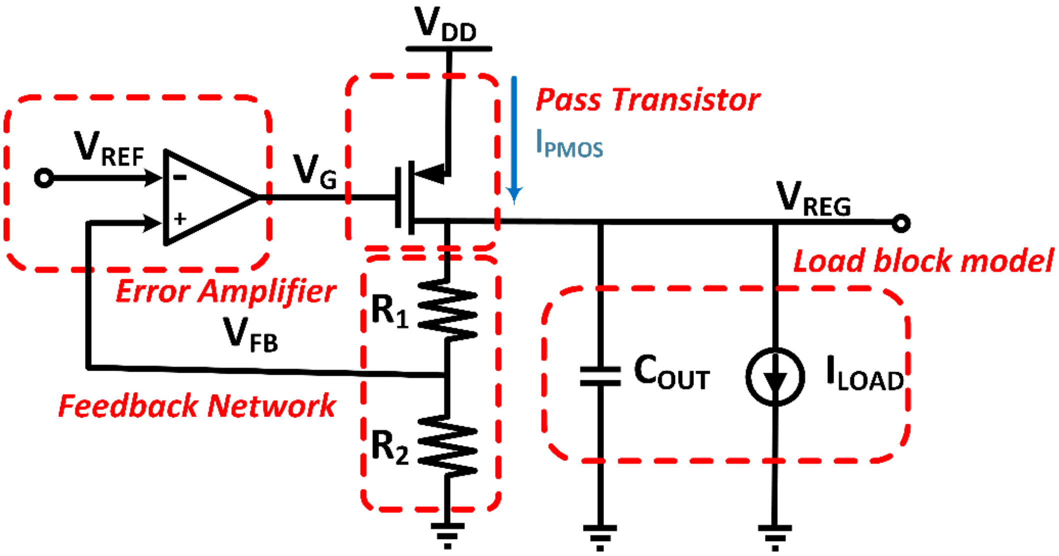

Figure 2.1 Conventional LDO regulator

Reference voltage which generated by bandgap voltage reference which is designed with proportional to-absolute-temperature (PTAT) [36]-[37] and complementary to-absolute-temperature (CTAT) [38]-[39]circuit. The CTAT has a higher temperature coefficient while the PTAT design needs to be optimized in order to adjust the temperature coefficient [40]. The error amplifier has two inputs, in where one input is tied to reference voltage while another input is connected to the feedback network resistor. The feedback network resistor will sample the variation of the input voltage and the error amplifier will continuously do the comparison between the voltage of feedback resistor [41]-[42] and the reference voltage. Corrected signal is driven again through the gate of pass transistor in order to provide a constant output voltage. The output voltage is expressed as:

$$V_{out}=\left(1+\frac{R_{fb1}}{R_{fb2}}\right)V_{ref} \tag{2.1}$$

Besides, conventional LDO has an off-chip capacitor where the output of LDO became dominant pole in order to guarantee the stability of the system and the ripple of output voltage was minimized.

The performance of the LDO can be measured using FoM. Smaller FoM has better performance [43] . The formula to measure the FoM in terms of second (s) is:

$$FoM=\frac{T_s}{PSR_{V/V}}\frac{I_q}{I_{MAX}} \tag{2.2}$$

Based on (2.2), the FoM determined by the settling time, power supply rejection ratio, quiescent current and total maximum current of the system. By lowering the settling time and quiescent current, subsequently, maximizing higher PSRR and load current can ensure the performances of the LDO is optimized. Unfortunately, in real cases, when improving one parameter, another parameter will be traded-off. Researchers are introducing various methodologies to optimize lower FoM of the LDOs.

2.1.2 Architecture of DC-DC Switching Regulator

DC-DC switching regulators [44]-[45]are characterized by their exceptional efficiency, large driving capacity, and diverse output voltage possibilities. An illustration of the primary components of a DC-DC switching converter can be seen in Figure 2.2.

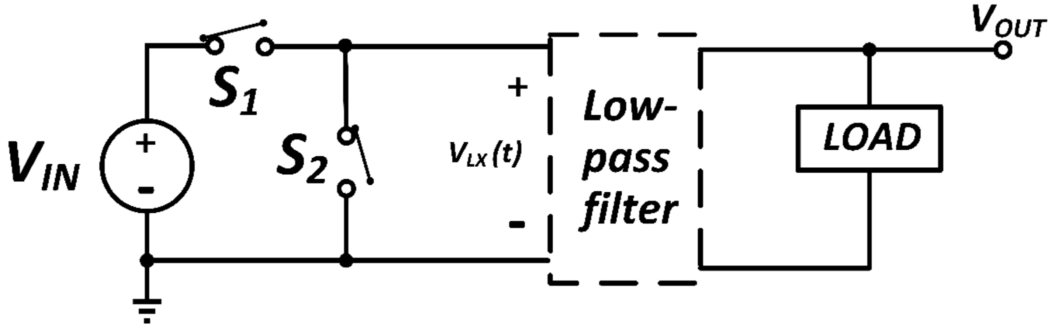

Figure 2.2	Basic diagram of DC-DC converter

In accordance with the intrinsic "switching" feature, switches S1 and S2 are essential in controlling the energy transfer from the input DC voltage source V_{IN} to the output V_{OUT}. When S1 is active and S2 is off, energy moves from V_{IN} to V_{OUT} and vice versa. On the other hand, when S1 or S2 are both in a on state, no energy is transferred from V_{IN} to V_{OUT}. By flipping S1 and S2 in turn, it is possible to efficiently regulate the energy provided to V_{OUT}. After that, a low-pass filter is used to remove the high-frequency elements produced by the switching process. By using a similar argumentation, the DC component, which is equal to the average value obtained through Fourier analysis, could be found. At the end of the day, energy is transferred to V_{OUT} in the form of a DC voltage, which powers the output load [46].

For a short while, it is not even allowed to turn on S1 and S2 concurrently. This simultaneous activation results in significant energy loss and redirecting energy from the input to the ground. It is difficult to determine when S1 and S2 will activate exactly. Maintaining a consistent turn-on time ratio for both S1 and S2 is crucial, regardless of how often they alternate in their activation. For a given load state, this consistency guarantees a constant flow of energy to the output when a particular output voltage is needed.

The following expression describes the relationship between the switching frequency (f_S) and the switching period (Ts):

$$f_S = \frac{1}{T_S} \tag{2.3}$$

In DC-DC switching converters, the duty cycle, represented by equation 2.4 represents the amount of time required for transferring energy from input to output during a switching cycle. It is the percentage of the total switching time that S1 is on. Because the switching cycle is repeating, a constant switching frequency has been achieved.

$$D = \frac{S_1\, turn - on\ time}{T_S} \tag{2.4}$$

The switching activity between switches S1 and S2, visible at the switching node L_X, is shown in Figure 2.3.

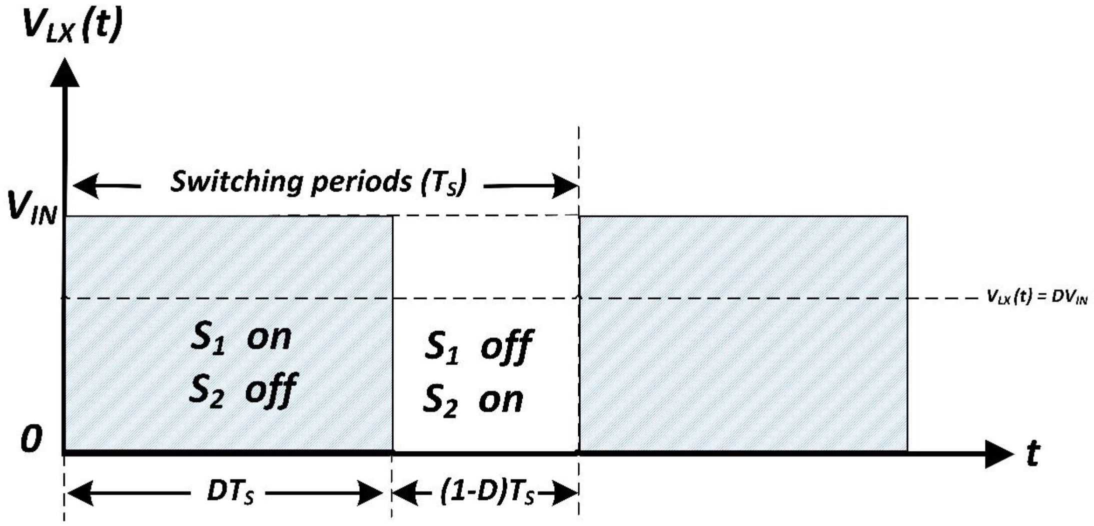

Figure 2.3 Switching waveform of DC-DC regulator

When S1 is turned on, L_X connects to the supply voltage, V_{IN}, which means that V_{LX} (t)=V_{IN}, where V_{IN} is the DC component of V_{IN} (t). On the other hand, L_X is discharged to zero volts and then dragged to the ground when S2 is turned on. A low-pass filter is utilized to remove the higher-frequency harmonics (t) to isolate the DC component of the signal, V_{LX}. Stated otherwise, the average value of V_{LX} (t) for the period of interest is equal to the DC component, which is obtained from the Fourier transform.

As denoted by V_{LX} (t), the DC value of the signal at the switching node is.

$$\overline{V_{LX}(t)} = \frac{1}{T_S}\int_0^{T_S} V_{LX}(t)dt = DV_{IN} \qquad 2.5$$

It may be inferred that the mean of V_{LX} (t) is equal to the source voltage times the duty cycle, as the output voltage is exactly proportional to this mean. Consequently, the duty cycle controls the SWR's output voltage.

A buck converter [47]-[48] topology is employed. Besides, the boost and buck-boost converters are two other basic topologies of the SWR. A boost converter raises the source voltage to a step-up or step-down voltage level, although a buck-boost converter can accomplish the same. Both buck and boost converters consist of switches and a filter, just like buck converters do. The filter is realized by use of an off-chip inductor and capacitor in a second-order LC filter. As the output voltage is stabilized by the capacitor, the inductor current's continuous nature determines the amount of current applied to the load.

Buck converters, which are extensively used in many industries to lower a greater input voltage to an output voltage, have the simplest construction among Switched-mode Power Supplies (SMPS) [49]-[50]. Being a voltage step-down converter, the buck converter lacks galvanic isolation between the input and output and functions as a non-isolated converter. Buck converters are widely used for power distribution in complex systems, including server motherboards and broadband communication boards. They get the necessary local voltage from a higher voltage bus that is shared by several converters.

The buck converter is composed of a single active switch, rectifier, and filter components, all of which are managed by an integrated circuit. Power distribution throughout the entire application is made cost-effective and extremely efficient by this simple design. A qualitative advantage is provided by the filter inductor on the output side of the buck converter, which ensures a steady and even output current waveform to the load. However, significant load fluctuations necessitate careful consideration.

The accessibility of the input, which is managed by switch S, produces a dynamic waveform for the input current. This dynamic behavior is considered undesirable since the switching current generates noise throughout the system. Capacitor C facilitates good decoupling, which is a crucial part of this system [51].

There are two types of operation modes for the inductor current in any converter: the continuous conduction mode (CCM) [52]-[53] and the discontinuous conduction mode (DCM) [54]-[55]. A continuously nonzero inductor current is a defining characteristic of CCM, while a low switching frequency or high load resistance cause the average inductor current to drop to an unacceptable level, which pushes the converter into DCM [56]. The best use of semiconductor switches and passive components, as well as optimal efficiency, are achieved by choosing CCM [57].

Maintaining the CCM lowers the dynamic order of the converter, which is essential for best performance and economical utilization of passive components and semiconductor switches. A particular control method is required since the DCM reduces the dynamic order of the converter. To maintain the CCM, it is therefore essential to determine the inductor's minimum value. Basically, the CCM is preferred because of its best performance, and maintaining it necessitates figuring out what the inductor's minimum value should be.

The simplified buck converter structure is shown in Figure 2.4. It consists of the load, the two-pole low-pass filter (L and C), and the two switches D (diode) and S (power electronics switches that can be partially or fully controlled). In this arrangement, the switch duty cycle is assumed.

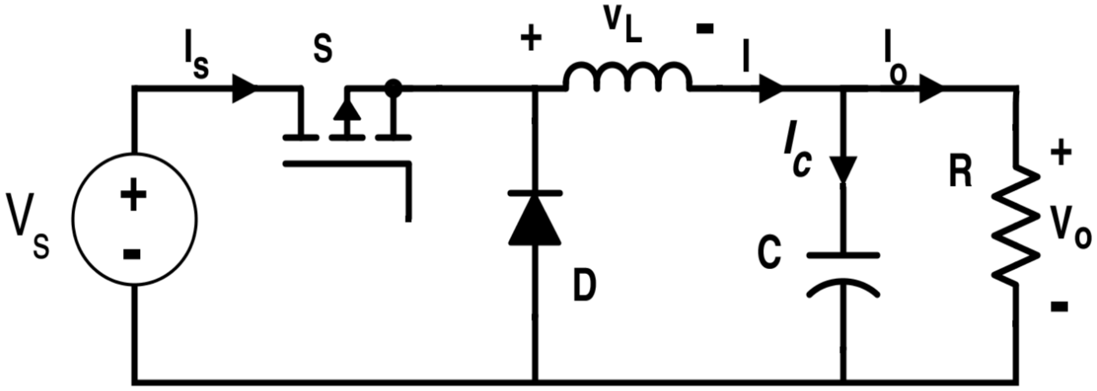

Figure 2.4 DC-DC Buck Converter circuit

2.2 A Comprehensive Review of Power Efficiency

2.2.1 Low Dropout Regulator

The efficiency of an LDO regulator is affected by the quiescent current and the input/output voltages in the following way:

$$Efficiency\ (\eta) = \frac{P_{OUT}}{P_{IN}} \tag{2.6}$$

$$Efficiency\ (\eta) = \frac{I_o V_o}{(I_o + I_q)V_i} x100\% \tag{2.7}$$

Minimizing quiescent current and dropout voltage is crucial for optimal efficiency. Furthermore, it is essential to reduce the voltage differential between the input and output of LDO regulators because their efficiency is dependent on power dissipation.

The power dissipation (PDISS) of an LDO regulator can be calculated as follows:

$$P_{DISS} = (V_{IN} - V_{OUT}) x I_{OUT} + V_{IN} x I_q \qquad 2.8$$

Regardless of the load scenario, the input to output voltage differential is essential for calculating efficiency. Since the LDO cannot store significant amounts of superfluous energy, power lost to heat occurs within the device in the event that the load is not powered.

The minimal voltage differential between the input and output needed to maintain regulation is referred to as dropout. To reduce power loss and increase efficiency, it is recommended to maintain the dropout voltage as low as possible. The output voltage is commonly regarded as having dropped to 100 mV below its nominal value prior to dropout being declared to have happened. The dropout voltage may be affected by the junction temperature and the load current.

Since the low dropout regulator is designed to reduce smaller voltage levels by design, there isn't a good way to deal with this and achieve higher efficiency of power. Most papers focus mostly on quiescent current control because lowering it improves the LDO's current efficiency and provides a mechanism to get higher power efficiency. The topology for lowering quiescent current was reviewed in this section.

S.Chong et al, proposed a 0.9-µA adaptive stage LDO regulator to achieve an ultra-low quiescent current [28]. The structure of the proposed LDO arranged as dynamic-biased error amplifier as 1st stage, non-inverting amplifier as 2nd stage, power transistor as 3rd stage. Based on the load current loading, the regulator will change between a 2-stage and a 3-stage cascaded topologies along with the power transistor. During light load or no-load condition, the non-inverting amplifier will enter to triode region and the main power transistor it will be turned off. The proposed regulator can be viewed as a 2-stage structure when the load current is less than the defined threshold current. To obtain a low quiescent current, a dynamic biassing approach was introduced to the first stage amplifier, where the bias current is directly proportional to the current of the sub-power transistor, and the rise of the bias current is gated when the main pass transistor is turned on. The primary power transistor is turned on when the load current is increased, forming a three-stage structure. In addition, during heavy load condition, the pole on the output regulator was changed to a higher frequency. By adopting a multistage structural design that can lower the quiescent current under no load conditions, the proposed solution eliminates the stability issue as well as the minimum load current. Since this topology focus on the quiescent current, the transient response and PSSR is failing to optimize by the author.

A. J. López-Martín et al. proposed a flipped voltage follower (FVF) [58]-[59] topology to improve the performances of the OTA by adaptive biasing [60]. With the proposed topology, the tail current of the input differential stage is boosted. To minimize the static power consumption, the FVF will provide a variable bias current. The bias current is provided only when the input signal is detected. When there is no input signal, only the constant quiescent current is provided.

Young-il Kim et al, proposed a class-AB OTA [61]-[62] which behaves as an error amplifier, ERR AMP [63]. This topology helps to increase the current capability during large signal with lower quiescent current. The proposed OTA is shown in Figure 2.5, where it utilizes topologies of high-performance OTA with single-pole and adaptive biasing and local common-mode feedback Class AB OTA from [64] and [60] respectively to achieve a higher DC gain and slew rate.

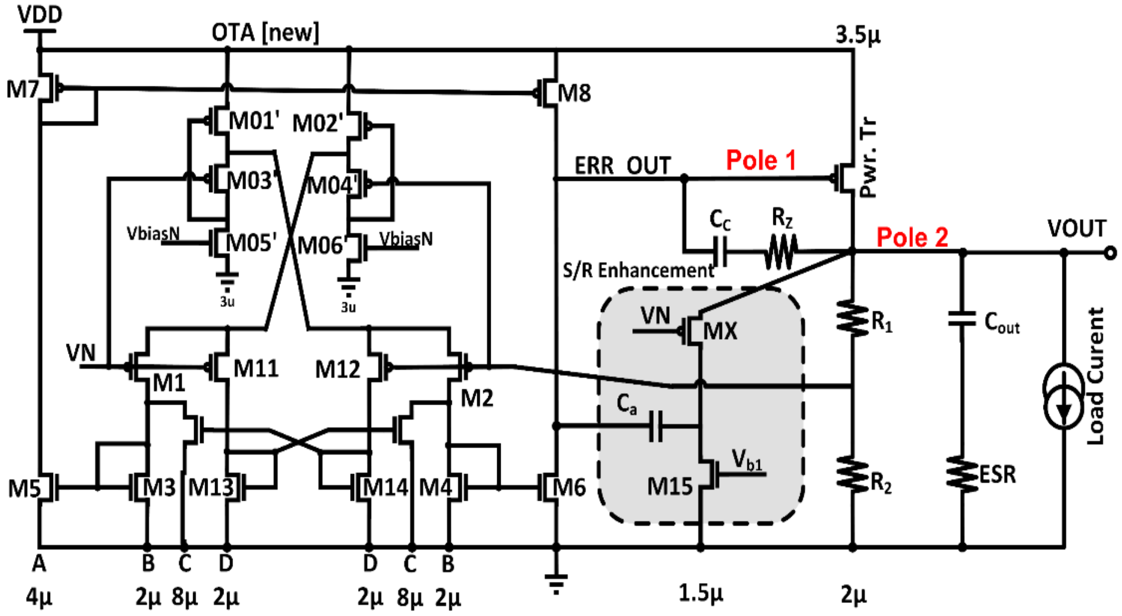

Figure 2.5 Schematic of the LDO with ERR AMP together SR enhancement circuit

Referring to Figure 2.5, the transistor M_{04} functions as source follower amplifier in where it is employed to detect the voltage, V_p variation. The signal is then amplified by M_1 and M_{11}, which operate as a common gate amplifier. M_3 and M_4 transistor drains function in a class-AB mode. The total transconductances of the proposed OTA is multiplied with additional signal path. In the proposed OTA, the overall gain, transconductance, and the output resistance are increased while the quiescent current is decreased.

Raveesh Magod, et al, presented a hybrid bias current generator (HBCG) to achieve a 1.24 μA quiescent current in a NMOS LDO [65]. The transient response is improved by boosting the bias current dynamically and adaptively. Both adaptive current scaling and dynamic current scaling can be implemented by utilizing HBCG. The hybrid biasing circuit which is proposed in this work helps to reduce the overshoot and undershoot voltage. At this low quiescent current, the recovery performance is