INVESTIGATION OF GALLIUM OXIDE AND GALLIUM CERIUM OXIDE PASSIVATION LAYERS ON SILICON AND 4H–SILICON CARBIDE SUBSTRATES FOR METAL-OXIDE-SEMICONDUCTOR BASED DEVICES

PUTERI HASLINDA BINTI MEGAT ABDUL HEDEI

UNIVERSITI SAINS MALAYSIA

2025

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by

PUTERI HASLINDA BINTI MEGAT ABDUL HEDEI

Thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

January 2025

DECLARATION

I hereby declare that this thesis, submitted to Universiti Sains Malaysia as partial fulfilment of the requirement for the Doctor of Philosophy, has not been submitted to any other Universities or Institutions for any degrees. I also declare that the work described herein is based on my original work, except for quotations and citations that have been duly acknowledged.

Puteri Haslinda Binti Megat Abdul Hedei
Date:12/08/2024

ACKNOWLEDGEMENT

I am deeply grateful to Allah and all those who have supported me throughout my thesis. This journey would not have been possible without the guidance, encouragement and unwavering support of many remarkable individuals. First and foremost, I would like to express my heartfelt thanks to my supervisor, Dr. Quah Hock Jin and my co-supervisor, Prof. Dr. Zainuriah Hassan. Their profound expertise, insightful feedback and continuous encouragement have been instrumental in shaping this research. I also want to thank Dr. Lim Way Foong for her commitment to excellence and dedication to mentoring, which have not only guided me through the complexities of my work but also inspired me to strive for greater heights. I am truly fortunate to have had their support and guidance throughout this endeavour. I am equally indebted to my family, whose support has been a cornerstone of this journey. To my Ayah (Megat Abdul Hedei), Mama (Norsiah), Abang (Megat Hafiz), Kakak (Puteri Hamira) and Kak Efa (Rozifa), your belief in my abilities and your sacrifices have been a constant source of motivation. My heartfelt appreciation also goes to my friends, whose encouragement and friendship have been invaluable. My friends have been a source of joy and respite during the most intense moments of this journey. Your support, whether through thoughtful conversations or simply being there to listen, has made this experience more enjoyable and manageable. I also would like to acknowledge the financial support from Malaysia Ministry of Education (MOE) for providing Fundamental Research Grant Scheme (FRGS; FRGS/1/2019/STG07/USM/02/3). Finally, I wish to acknowledge everyone who has contributed to my research in any capacity. Thank you all for being an essential part of this journey.

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LIST OF SYMBOLS

a	Lattice Parameter
C	Capacitance
C_{ox}	Oxide Capacitance
D	Crystallite Size
D_{it}	Interface Defect Density
d	Interplanar Spacing
δ	Dislocation Density
E_g	Bandgap
eV	Electron Volt
ε	Microstrain
ε_o	Permittivity of Free Space
ε_{RMS}	Root-Mean-Square Microstrain
I	Current
J	Current density
k	Dielectric Constant
q	Electronic Charge
Q_{eff}	Effective Oxide Charge
T	Temperature
t	Time
T_{hkl}	Coefficient Texture
t_{TOT}	Total Oxide Thickness
V_g	Gate Voltage
λ	Wavelength

LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
ALCVD	Atomic Layer Chemical Vapour Deposition
ALD	Atomic Layer Deposition
C-V	Capacitance-voltage
CVD	Chemical Vapour Deposition
DC	Direct Current
EDX	Energy Dispersive X-ray
FESEM	Field Emission Scanning Electron Microscopy
FTIR	Fourier Transform Infrared Spectroscopy
GIXRD	Grazing Incidence X-Ray Diffraction
ICDD	International Centre for Diffraction Data
I-t	Current-Time
I-V	Current-Voltage
J-E	Current density- Electric field
J-V	Current density-Voltage
KM	Kubelka-Munk
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal-oxide-semiconductor
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PL	Passivation Layer
PVD	Physical Vapour Deposition
RCA	Radio Corporation America
RF	Radio Frequency
RMS	Root-mean-square
STD	Slow Trap Density

UV-Vis	Ultraviolet-visible spectroscopy
XRD	X-Ray Diffraction Analysis
XRR	X-Ray Reflectivity
XPS	X-Ray Photoelectron Spectroscopy

PENYIASATAN LAPISAN PEMPASIFAN GALIUM OKSIDA DAN GALIUM SERIUM OKSIDA ATAS SUBSTRAT SILIKON DAN 4H–SILIKON KARBIDA UNTUK PERANTI BERASASKAN LOGAM-OKSIDA-SEMIKONDUKTOR

ABSTRAK

Teknologi yang berkembang dalam peranti berasaskan logam-oksida-semikonduktor (MOS) telah mencetuskan penggantian silikon (Si) konvensional dengan penggunaan semikonduktor sela jalur lebar, 4H-silikon karbida (SiC). Isu lain yang dihadapi adalah berkaitan dengan had silikon dioksida (SiO_2) untuk memenuhi permintaan semasa bagi peranti elektronik yang lebih kecil, lebih pantas dan lebih cekap. Ini telah mendorong pencarian bahan alternatif dengan pemalar dielektrik (k) yang lebih tinggi. Oleh itu, kajian ini tertumpu kepada penyiasatan filem galium oksida (Ga_2O_3) dan galium serium oksida ($Ga_xCe_yO_z$) yang terpercik pada substrat Si dan 4H-SiC oleh pemercitan magnetron frekuensi radio-arus terus untuk merealisasikan peranti MOS. Penyiasatan awal ke atas filem Ga_2O_3 dilakukan dengan mengubah parameter penyepuhlindapan selepas pemendapan, seperti ambien (nitrogen-oksigen-nitrogen (N_2-O_2-N_2), argon, oksigen), masa inap (30, 60, 90 dan 240 min), dan suhu (400, 600, 800 dan 1000°C). Telah didedahkan bahawa filem Ga_2O_3 yang disepuhlindapan dalam ambien N_2-O_2-N_2 selama 60 minit pada 800°C menunjukkan kehadiran fasa β-Ga_2O_3 yang stabil dengan sifat struktur, optik, morfologi dan elektrik yang boleh diterima disebabkan oleh penggabungan ion nitrogen ke dalam kekisi. Analisis seterusnya dengan menggunakan parameter penyepuhlindapan yang dioptimumkan untuk kajian perbandingan antara Ga_2O_3, serium gallium oksida ($Ce_xGa_yO_z$) dan $Ga_xCe_yO_z$ pada substrat Si telah menekankan kepentingan

menggabungkan ion galium ke dalam kekisi CeO_2. Oleh itu, penyiasatan lanjut dilakukan dengan mendepositkan $Ga_xCe_yO_z$ pada substrat Si dan 4H-SiC, diikuti dengan penyepuhlindapan pasca pemendapan dalam ambien N_2-O_2-N_2 pada suhu 800°C selama 60 minit. Kajian itu mendedahkan bahawa lapisan SiO_2 paling nipis terdapat dalam $Ga_xCe_yO_z$ pada sampel 4H-SiC telah membantu penambahbaikan sifat elektrik, seperti tahap kapasitansi penumpukan yang tinggi, *k* yang tinggi (19.47), ketumpatan arus bocor rendah (7.48 x 10^{-10} A cm^{-2}) dan medan elektrik pecah tebat yang tinggi (4.21 MV/cm), yang akan memberikan sumbangan penting untuk meningkatkan pembangunan peranti berasaskan MOS.

INVESTIGATION OF GALLIUM OXIDE AND GALLIUM CERIUM OXIDE PASSIVATION LAYERS ON SILICON AND 4H–SILICON CARBIDE SUBSTRATES FOR METAL-OXIDE-SEMICONDUCTOR BASED DEVICES

ABSTRACT

The evolving technologies in metal-oxide-semiconductor (MOS)-based devices have provoked the replacement of conventional silicon (Si) by the utilization of wide band gap semiconductor, 4H-silicon carbide (SiC). Another encountered issue was related to the limitation of silicon dioxide (SiO_2) to meet the current demand for smaller, faster and more efficient electronic devices. This has driven the search for alternative materials with higher dielectric constants (k). Therefore, this study focused on investigating gallium oxide (Ga_2O_3) and gallium cerium oxide ($Ga_xCe_yO_z$) films sputtered on Si and 4H-SiC substrates by direct current-radio frequency magnetron co-sputtering for the realization of MOS devices. Initial investigation on Ga_2O_3 films was done by varying the post-deposition annealing parameters, such as ambient (nitrogen oxygen-nitrogen (N_2-O_2-N_2), argon, oxygen), dwelling time (30, 60, 90 and 240 min) and temperatures (400, 600, 800 and 1000°C). It was revealed that the Ga_2O_3 film annealed in N_2-O_2-N_2 ambient for 60 min at 800°C demonstrated the presence of stable β-Ga_2O_3 phase with acceptable structural, optical, morphological and electrical properties due to the incorporation of nitrogen ions into the lattice. The subsequent analysis by employing the optimized annealing parameters to comparative studies amongst Ga_2O_3, cerium doped gallium oxide ($Ce_xGa_yO_z$) and $Ga_xCe_yO_z$ on Si substrates had emphasized the significance of incorporating gallium ions into the CeO_2 lattice. Thus, further investigation was done by depositing the $Ga_xCe_yO_z$ on Si and 4H-SiC substrates, followed by post-deposition annealing in N_2-O_2-N_2 ambient at

temperature of 800°C for 60 min. The study revealed that the thinnest SiO_2 layer was present in the $Ga_xCe_yO_z$ on 4H-SiC sample had assisting the improvement of electrical properties, such as high accumulation capacitance level, high-*k* (19.47), low leakage current density (7.48×10^{-10} A/cm) and high breakdown electric field (4.21 MV/cm), which would give a significant contribution to enhancing the development of the MOS-based devices.

CHAPTER 1

INTRODUCTION

1.1 Overview

The current advancements in the semiconductor industry primarily revolve around four simultaneous areas of emphasis that include scaling down devices to an unprecedented scale, reducing power consumption, enhancing operating speed and expanding the temperature range within which the devices can function reliably. Silicon (Si)-based metal-oxide-semiconductor (MOS) devices are now used in high-power electronics, such as radio frequency (RF) power amplifiers and high-frequency power switchers to achieve greater efficiency and energy savings [1,2]. Nevertheless, the narrow bandgap (E_g= 1.18 eV at room temperature) of Si materials has a detrimental impact on the performance and heat dissipation properties of Si-based power electronic devices [3]. Consequently, these limitations restrict the device's operation to moderate voltages and temperatures [4]. In order to address the limitations of Si-based MOS power devices, there has been significant interest in wide E_g semiconductors during the past two decades to withstand larger electric fields. Among a range of wide E_g semiconductors, silicon carbide (SiC) [5], gallium nitride (GaN) [5] and gallium oxide (Ga_2O_3) [6] have emerged as potential candidates that could surpass Si performance as semiconductors in MOS devices.

Amongst them, SiC has become a key contender in the wide E_g semiconductor materials since it is readily available in the commercial market and has the ability to promote the growth of silicon dioxide (SiO_2) [7]. SiC is found in several polytypes, such as 3H, 4H and 6H-SiC [8]. Among the several polytypes, 4H-SiC stands out for its remarkable properties in the field of semiconductor materials [8]. These

characteristics comprehend a wide E_g of ~3.2 eV [9,10], a high breakdown field (E_B) ranging from 2.3 to 3 MV/cm [9,10], a high saturation electron drift velocity of approximately 2 x 10^7 cm/s [10] and a high thermal conductivity of about 3 to 5 W/cm K [9,10]. Multiple studies have demonstrated the capability of 4H-SiC based MOS devices to function effectively under challenging conditions across various applications [11]. The transition from Si to 4H-SiC signifies a substantial technological advancement in the semiconductor sector. Driven by the superior electrical, thermal and physical properties of 4H-SiC, this transition promises to enhance the performance and efficiency of electronic devices across various high-power, high-temperature and high-frequency applications. While challenges remain, the future of 4H-SiC semiconductors is bright, with its adoption poised to grow as technology and manufacturing processes continue to evolve.

1.2 Problem Statement

The SiO_2 has long been the cornerstone material in the semiconductor industry, primarily used as the passivation layer (PL) in MOS devices. For decades, its exceptional insulating qualities, thermal stability and compatibility with Si technology have established it as the preferred material [12]. Nevertheless, as device dimensions continue to shrink in line with Moore's Law, the limitations of SiO_2 have become increasingly apparent [13]. As the thickness of the SiO_2 layer decreases to a few nanometers scale, the leakage current due to quantum tunnelling becomes significant [14]. The presence of this leakage current does not only result in a higher power consumption but also poses issues in dissipating heat, which can potentially impact the reliability and performance of the device [14]. Furthermore, the maximum potential of SiO_2 to be scaled down has been reached, highlighting the urgent need to discover

materials that could offer enhanced electrostatic control while enabling further miniaturization.

High-dielectric constant (*k*) materials offer a viable solution to the limitations of SiO_2 by enabling continued miniaturization of electronic devices while improving performance and reducing power consumption [15]. Despite the challenges of integrating high-*k* materials, their benefits make them indispensable in the quest for more advanced and efficient semiconductor devices. As research and development in this field progresses, high-*k* materials will undoubtedly play a pivotal role in shaping the future of electronics. The high-*k* materials are characterized by their ability to retain more electrical charge than SiO_2 for the same physical thickness [16]. This allows for the use of thicker layers to obtain the same capacitance, resulting in a reduction of leakage currents [16]. In addition, high-*k* materials offer a higher capacitance at reduced thickness, which enables further scaling of MOS devices, thus contributing to the continued miniaturization and performance enhancement [17]. Common high-*k* materials include zirconium dioxide (ZrO_2) [18], cerium oxide (CeO_2) [19], aluminium oxide (Al_2O_3) [20,21], praseodymium oxide (Pr_2O_3) [22], neodymium oxide (Nd_2O_3) [23], samarium oxide (Sm_2O_3) [24], europium oxide (Eu_2O_3) [25], gadolinium oxide (Gd_2O_3) [26], terbium oxide (Tb_2O_3) [27], dysprosium oxide (Dy_2O_3) [28], hafnium oxide (HfO_2) [29], lanthanum oxide (La_2O_3) [30], holmium oxide (Ho_2O_3) [31], erbium oxide (Er_2O_3) [32], thulium oxide (Tm_2O_3) [33], ytterbium oxide (Yb_2O_3) [34], lutetium oxide (Lu_2O_3) [35] and hafnium silicate ($HfSiO_4$) [36].

Among them, the rare earth CeO_2 was elucidated as a feasible alternative passivation layer (PL) for SiC-based MOS devices due to its fascinating properties, such as high-*k* values (~18-23) [37,38] large E_g (3.2-3.6 eV) [39] and large conduction band offset with respect to SiC substrate (0.88 eV) [40]. However, the tendency of

CeO_2 to interchange from Cerium (IV) (Ce^{4+}) to Cerium (III) (Ce^{3+}) state, depending on the oxygen concentration during deposition and post-deposition annealing processes has triggered the release of oxygen ions from CeO_2, in which these ions have diffused to the interface between CeO_2 and SiC surface to participate in the formation of undesirable low-*k* SiO_2 interfacial layer [41]. Besides reducing the overall *k* value of the investigated CeO_2 PL, the formation of oxygen vacancies in CeO_2 lattice under oxygen-deficient conditions has provoked the formation of additional defects that would degrade the electrical performance of PL [42]. Therefore, divalent, tetravalent and trivalent cations were proposed to be introduced into CeO_2 lattice to alleviate the interchange of state from Ce^{4+} to Ce^{3+} that was postulated to yield positive impacts, such as impeding the formation of oxygen vacancies and enhancing the passivating properties of these PL [43,44].

It was discovered that introducing divalent cations had improved its redox-reduction activities, reducing the E_g as well as improving the catalytic activity [45-47]. A similar observation was found when the introduction of tetravalent cations, such as zirconium (IV) (Zr^{4+}) [43], hafnium (IV) (Hf^{4+}) [43], titanium (IV) (Ti^{4+}) [43] and thulium (IV) (Th^{4+}) [43] into CeO_2 lattice have triggered the formation of more oxygen vacancies acting as leakage current path [48], which were considered as an undesirable condition for PL. Although oxygen vacancies were formed when trivalent cations, such as manganese (III) (Mn^{3+}), gadolinium (Gd^{3+}) and scandium (III) (Sc^{3+}) were introduced into the CeO_2 lattice, redox inactive oxygen vacancies were formed due to the coulomb attraction between these trivalent ions and oxygen vacancies [44,49]. Hence, the available oxygen vacancies acting as sites for oxygen ions to hop to the interface were cut down in the trivalent cations doped CeO_2 that would mitigate the formation of SiO_2 interfacial layer [41]. In this work, trivalent gallium (Ga^{3+}) cations

with smaller ionic radius (0.062 nm) [50] than the previously employed trivalent cations [51,52] were introduced into the CeO_2 lattice with the intention of minimizing lattice distortion as well as enhancing the aliovalent substitution efficiency [51,53]. Nonetheless, the $Ga_xCe_yO_z$ on 4H-SiC substrates was not fully discovered and the research was scarce. In addition, while high-*k* materials offer numerous advantages, their integration into semiconductor processes presents several challenges. The interface between the high-*k* material and the 4H-SiC substrate must be carefully explored to avoid defects that can degrade device performance. Techniques such as interfacial layer incorporation and annealing processes could be employed to improve interface quality. Continuing research and development in this area will be vital to overcoming the existing challenges and fully realizing the potential of high-*k* materials in advanced electronic applications.

1.3 Objectives

This research focuses on implementing alternative semiconductors and high-*k* gate oxide to address the challenges of scaling MOS devices. This research aims to investigate Ga_2O_3 and $Ga_xCe_yO_z$ films that were sputtered on Si and 4H–SiC substrates. Thus, the primary objectives of this study are established as follows:

(i) To investigate the effects of varying post-deposition annealing parameters on the structural, optical, morphological and electrical properties of Ga_2O_3 films.

(ii) To investigate the effects of varying post-deposition annealing parameters on the structural, optical, morphological and electrical properties of $Ga_xCe_yO_z$ films.

(iii) To explore the potential of $Ga_xCe_yO_z$ films as a high-*k* PL deposited on 4H-SiC for MOS device application.

1.4 Scope of Study

In this research, the investigation of Ga_2O_3 on Si substrates and $Ga_xCe_yO_z$ on Si and 4H-SiC substrates was conducted. The radio frequency (RF) and direct current (DC) magnetron sputtering technique was selected to deposit these materials on Si and 4H-SiC substrates. Specifically, the effects of post-deposition annealing temperatures (400, 600, 800 and 1000°C), dwelling time (30, 60, 90 and 240 min) as well as annealing ambient (nitrogen-oxygen-nitrogen (N_2-O_2-N_2), argon and oxygen) were investigated for Ga_2O_3 on Si substrates. Further investigations were done by investigating $Ga_xCe_yO_z$ on Si and 4H-SiC substrates. The variation of post-deposition annealing temperature was between 600, 700, 800 and 900°C for the $Ga_xCe_yO_z$ on 4H-SiC substrates. The structural, morphological, chemical, optical and electrical characteristics of the investigated samples were done to establish the potential of $Ga_xCe_yO_z$ as high-*k* PL for MOS-based devices.

1.5 Thesis Outline

This thesis comprises six chapters. Chapter 1 presents a comprehensive overview of the context of studies, the issue being addressed, the research goals and the scope to which this research is focused. Chapter 2 provides an in-depth analysis of the theoretical foundation and existing research on MOS-based devices. This chapter also includes a review of Si, 4H-SiC and Ga_2O_3 as semiconductors as well as Ga_2O_3 and CeO_2 as PL. Chapter 3 provides a detailed description of the technique, experimental design, materials and equipment employed in this investigation. Chapter

4 and Chapter 5 discuss the structural, optical, chemical, morphological and electrical properties of Ga_2O_3 on Si substrates and $Ga_xCe_yO_z$ on Si and 4H-SiC substrates based on variation of post-deposition annealing conditions. Chapter 6 provides a comprehensive overview of the research's findings and results, as well as future recommendations to enhance the current study.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Si-based power devices, operating on the basis of MOS structure have been widely employed in almost all extant power devices, such as computers, laptops, smart phones and automotive electronics [1-2]. However, the efficiency of Si-based power devices is approaching to its theoretical limit [54] due to the future technological breakthroughs towards advanced applications, such as electronic gadgets, electric vehicles, home appliances and power generations that have pushed the use of semiconductors with high efficiency and outstanding reliability for the development of high-power devices. The narrow E_g (1.10 eV) and low E_B (0.25 MV/cm) of Si had restricted the device operation at higher power as a consequence of the inefficiency of Si to dissipate heat and, thus triggering high power loss [55-57]. Hence, focusing research on the development of SiC as a wide E_g semiconductor to replace Si is a reasonable step towards ultimately meeting a higher efficiency MOS-based power device since SiC could deliver superior properties, such as wide E_g (~3.26 eV), high thermal conductivity (~370 W/mK) as well as the high E_B (~2.2 x 10^6 V/cm) [57,58], which would allow the device to operate at minimized power loss.

While exploring the capability of SiC to deliver better device operation when compared to Si, the quality of the PL used in the MOS structure is paramount. SiO_2 has been the state-of-the-art PL for Si and SiC-based MOS devices produced by thermal oxidation of the Si and SiC substrates. However, low-*k* of SiO_2 (k= 3.9) as well as low E_B and low gate oxide capacitance when being used for MOS devices had caused reliability issues devoted to heat dissipation and high leakage current density

(*J)* [59,60]. Therefore, a shift towards employing PL with a higher-*k* value was implemented to allow an increase in the gate oxide capacitance without the concomitant *J*.

The rare earth CeO_2 was elucidated as a feasible alternative PL, which has been used in both Si and SiC-based MOS devices due to its fascinating properties, such as high-*k* values (~18-23) [37,38] large E_g (3.2-3.6 eV) [39] and large conduction band offset with respect to Si (2.7 eV) [61] and 4H-SiC substrate (0.88 eV) [40]. However, the tendency of CeO_2 to interchange from Cerium (IV), Ce^{4+} to Cerium (III), Ce^{3+} state, depending on the oxygen concentration during deposition and post-deposition annealing processes would trigger the release of oxygen ions from the CeO_2, which contributed to the formation of an undesirable low-*k* SiO_2 interfacial layer at the CeO_2/Si [62,63] and/or CeO_2/SiC interface [41]. Besides reducing the overall *k* value of the investigated CeO_2 PL, the formation of oxygen vacancies in the CeO_2 lattice under oxygen-deficient conditions has provoked the formation of additional defects that would degrade the electrical performance of PL [42]. Therefore, trivalent cations were proposed to be introduced into CeO_2 lattice to alleviate the interchange of state from Ce^{4+} to Ce^{3+} that was postulated to yield positive impacts, such as impeding the formation of oxygen vacancies and enhancing the electrical properties of these PL [43,44]. Although oxygen vacancies were formed when trivalent cations, such as Mn^{3+}, Gd^{3+} and Sc^{3+} were introduced into the CeO_2 lattice, redox inactive oxygen vacancies were formed due to the coulomb attraction between these trivalent ions and oxygen vacancies [44,49]. Hence, the available oxygen vacancies acting as sites for oxygen ions to hop to the interface was cut down in the trivalent cation-doped CeO_2 that would mitigate the formation of SiO_2 interfacial layer [41]. Nonetheless, the exploration of trivalent cation-doped CeO_2 as PL on Si and 4H-SiC substrates were not fully

discovered and the research was scarce. Therefore, in this work, trivalent Ga^{3+} cation with smaller ionic radius (0.062 nm) [50] than the previously employed trivalent cations [51,52] were introduced into the CeO_2 lattice with the intention of minimizing lattice distortion as well as enhancing the aliovalent substitution efficiency [51,53].

This chapter highlights the importance of the 4H-SiC substrate as the wide E_g semiconductor as well as reviewing the characteristics needed for high-*k* material, properties of high-*k* materials and formation of defects. This chapter also includes the properties and possibilities of Ga_2O_3 as a doping material to overcome the limitations imposed by CeO_2.

2.2 Revolution of Si Technology with Wide Bandgap Semiconductors

Semiconductors have been at the heart of technological advancements for decades, driving the evolution of modern electronics. While Si has been the cornerstone of semiconductor technology, the emergence of wide E_g materials, such as GaN, Ga_2O_3 and SiC marks a new era in the semiconductor revolution.

One of the primary reasons for extensive application of Si at the beginning of era of the semiconductor industry is due to the abundance of Si in the Earth's crust, comprising about 28% by weight [64]. This high availability has translated to a relatively low cost of raw materials, making Si an economically viable option for large-scale production of semiconductor devices [65] and thus revolutionizing the technology landscape. Moreover, the ease of Si to be thermally oxidized, resulting in the formation of good quality SiO_2 as the native oxide for MOS devices [66] has resulted in the advancement and fabrication of Si-based MOS devices in the semiconductor industry since the 1960s, which had been accomplished via the refinement of production techniques, device designs and material quality [67]. Si

versatility is reflected in its wide range of applications in the semiconductor industry. It is the primary material used in the production of transistors, which are the fundamental building blocks of integrated circuits that are integral to virtually all electronic devices, including computers, smartphones and industrial machinery [68].

Nevertheless, as the world evolved into the modern era, several commercial power devices were approaching their theoretical limit concerning their capacity to withstand high voltage and achieve high-frequency switching [54]. The Si-based device had suffered from the high *J* and low E_B of 0.25 MV/cm that resulting in heat dissipation and degradation in the MOS device performance. Consequently, in past decades, power system designers have attempted to discover alternate strategies for fulfilling demands of modern power devices. A potential solution to conform to the demands of current electronics devices, which could only be achieved through the adaption of a more superior wide E_g semiconductors, such as GaN, SiC and Ga_2O_3 [69]. The employment of these wide band gap semiconductors would minimize the heat generation during the operation of devices, achieving design of electronics devices with smaller dimensions, as well as operating at a higher electric field.

2.2.1 Gallium Nitride (GaN)

GaN is an exceptional semiconductor material that has brought significant advancements in a wide range of electronic applications requiring high power and high frequency. Its unique properties, including a wide E_g (3.4 eV), high electron mobility (1200 to 1250 cm^2/Vs) and excellent thermal stability have made it an essential component in modern electronics [5,70]. GaN devices exhibit higher efficiency compared to Si, particularly in power conversion applications. They can operate at higher frequencies and voltages, reducing energy losses and improving overall system

efficiency. GaN devices possess the capability to function at elevated frequencies and power levels, resulting in their reduced size and weight. The compactness of this product is especially advantageous in situations of limited space and weight. Despite its moderate thermal conductivity, the wide E_g of GaN allows for higher thermal stability and operation at elevated temperatures. This capability reduces the need for extensive cooling systems, further enhancing efficiency and reliability.

2.2.2 Silicon Carbide (SiC)

Generally, there are three polytypes of SiC which are 3C-SiC polytype (commonly recognized as a low-temperature polytype), 4H- and 6H-SiC polytypes (high-temperature polytypes). These polytypes have the same chemical composition but different crystal structures along the c-axis, where C and H represent cubic and hexagonal atom arrangements (shown in Figure 2.1), that leads to variations in their physical properties [71]. The primary emphasis of the SiC polytypes is 4H- and 6H-SiC due to their ability to withstand high temperatures, which facilitates efficient heat dissipation [71]. This is a crucial aspect in ensuring the stability and durability of electronic devices during high-power operations.

Among them, 4H-SiC demonstrates exceptional performance in high-power and high-frequency electronic devices. Its superior electron mobility (900 cm^2/Vs) and large E_g (3.26 eV) would allow its use for effective performance at high temperatures and voltages, establishing it as a reliable choice for power electronics [70,72,73]. These applications encompass power switches, diodes and rectifiers, specifically in industries that require strong performance under challenging conditions, such as electric vehicles, renewable energy systems and aerospace electronics. In addition, 4H-SiC also has a remarkable physical durability and chemical inert that makes it ideal for

semiconductor devices that operate in harsh conditions [8]. Another feasibility of employing 4H-SiC semiconductor in MOS-based devices was the ability to produce a high-quality SiO_2 through thermal oxidation so its development can mimic Si. For aforementioned reasons, 4H-SiC had stood out as a wide E_g semiconductor [74].

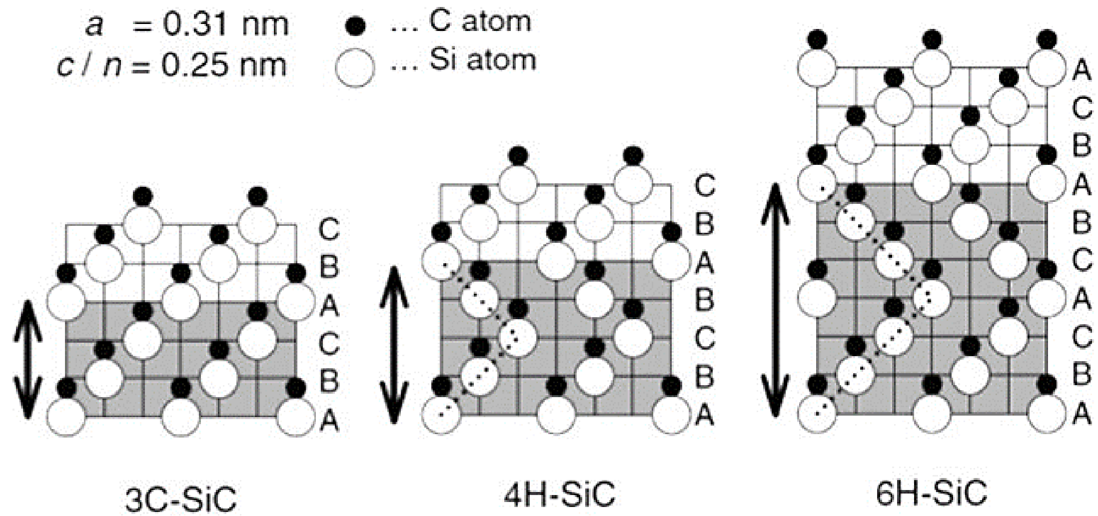

Figure 2.1 The atom arrangement of SiC polytypes [75].

2.2.3 Gallium Oxide (Ga_2O_3)

Ga_2O_3 outperforms other semiconductors due to its exceptionally wide E_g (4.7-4.9 eV) [76-78], high E_B (~ 8 MV/cm) [78,79] and a significant Baliga's figure of merit (BFOM = 3444) [80,81]. The utilization of Ga_2O_3 for MOS-based devices could achieve a higher packing density and higher E_B compared to the devices based on SiC and GaN [76,82-84]. The single crystalline or polycrystalline Ga_2O_3 could possibly appear in five different types of Ga_2O_3 polymorphs (α, β, γ, δ and ε) [85,86]. Although the α- and δ-Ga_2O_3 comprise larger E_g of 4.99 and 4.84 eV, respectively, compared to β-Ga_2O_3, the β-Ga_2O_3 emerges as the most preferable polymorph due to its thermodynamically and chemically stable crystal structure.

The high E_B of β-Ga_2O_3 (8 MV/cm) would allow for the design of power devices that could handle higher voltages and currents, which is crucial for applications such as electric vehicles, renewable energy systems and power grids. Moreover, the lower cost of producing β-Ga_2O_3 substrates compared to SiC and GaN substrates makes it a more economically viable option for mass production. This cost advantage, combined with its superior performance characteristics, positions β-Ga_2O_3 as a promising material for next-generation power electronic devices.

In comparison, 4H-SiC offers several advantages as semiconductor over β-Ga_2O_3 and GaN, particularly in terms of thermal conductivity, maturity of technology, high-temperature operation, mechanical strength and radiation hardness. These properties make 4H-SiC a superior choice for high-power, high-temperature and harsh-environment applications. A comparison of the properties of the Si, GaN, Ga_2O_3 and 4H-SiC are summarized in Table 2.1 to provide a clearer view of their properties.

Table 2.1 Comparison of properties of Si, GaN, Ga_2O_3 and 4H-SiC [70,73,76-78].

Properties	**Si**	**4H-SiC**	**GaN**	**β-Ga_2O_3**
Bandgap (eV)	1.1	3.3	3.4	4.7-4.9
Dielectric Constant	11.8	9.7	9.0	10
Thermal conductivity (W/cm K)	1.5	3.8	2.1-2.3	0.1-0.3
Breakdown electric field (MV/cm)	0.3	2.5	3.3	8
Saturation velocity (10^7 cm/s)	1	2	2.5	1.8-2
Electron mobility (cm^2 /Vs)	1400-1480	1000	1200-1250	300

2.3 Overview of Metal-Oxide-Semiconductor (MOS)

The Metal-Oxide-Semiconductor (MOS) structure is a pivotal component in the field of semiconductor technology. It forms the foundation for many contemporary electronic devices, including transistors and integrated circuits, which are essential for the functioning of modern electronics. Understanding the MOS structure and its applications provides insight into the rapid advancements in electronic device miniaturization and performance enhancement. The MOS structure consists of three primary layers, which include the metal gate, the oxide insulator and the semiconductor substrate, as shown in Figure 2.2 [87]. Each of these layers plays a crucial role in the operation of MOS devices. The gate electrode is typically made of metal such as aluminium. The gate serves as the control terminal that modulates the flow of charge carriers in the semiconductor. By applying a voltage to the gate, an electric field is created, influencing the conductivity of the underlying semiconductor material.

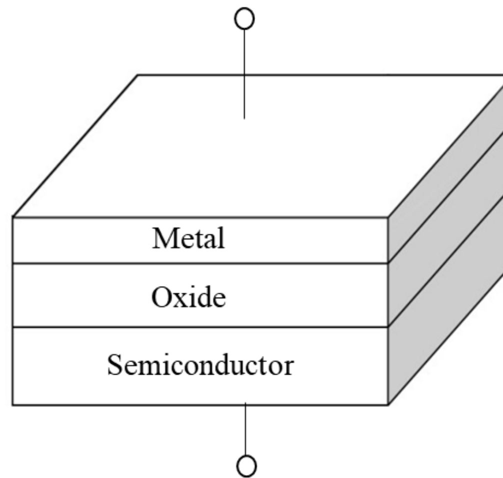

Figure 2.2 Simple MOS structure [87].

For the oxide layer, commonly, SiO_2 is an insulating material that separates the metal gate from the semiconductor. The primary function of the oxide layer is to act as an insulator between the metal gate and the semiconductor substrate. This insulation is crucial because it prevents direct electrical contact between the gate and the semiconductor, which would otherwise result in undesirable leakage current. By providing this insulation, the oxide layer allows for the control of the semiconductor's conductivity via the gate voltage without direct current flow between the gate and the substrate. In addition, the oxide layer contributes to the formation of the gate capacitance in MOS devices. When a voltage is applied to the metal gate, an electric field is established across the oxide layer, inducing charge carriers in the semiconductor. The ability of the gate to control the charge carriers in the semiconductor is dependent on the capacitance of the oxide layer. A thinner oxide layer results in higher capacitance, enhancing the gate control over the channel conductivity and improving the device's switching characteristics. The oxide layer also serves as a surface PL for the semiconductor. Surface passivation involves reducing the number of electronic states at the semiconductor surface that can trap charge carriers and degrade device performance. The oxide layer helps to stabilize the semiconductor

surface by reducing surface recombination and improving the overall reliability and performance of the MOS device.

The semiconductor substrates, of which Si is the most commonly used semiconductor material, though alternatives, such as GaN, Ga_2O_3 and SiC are also employed as aforementioned in the previous section.

2.3.1 Modes of Operation

Under a zero-bias condition ($V_g = 0$), the oxide-semiconductor interface will be devoid of any charges. In this case, no depletion region is noticed. When the positive or negative bias is applied, three cases will arise at the oxide-semiconductor interface.

As the n-type semiconductor substrate is applied with a positive gate voltage ($V_g > 0$), the majority of carriers, which are electrons will be drawn closer to the oxide-semiconductor interface, as shown in Figure 2.3. This is due to accumulation conditions where the Fermi energy (E_F) of semiconductor is higher than E_F of metal. Therefore, the valence band (E_v) of semiconductor will bend upwards, closer to the E_F.

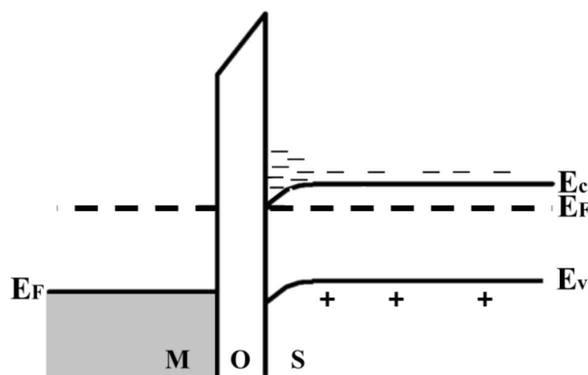

Figure 2.3 Energy band diagram of n-type semiconductor in accumulation region ($V_g > 0$) [88].

Figure 2.4 illustrates the depletion condition that occurs when a negative bias ($V_g < 0$) is applied to the semiconductor. In this condition, the electron concentration at the interface between the oxide and the semiconductor has been reduced to a level lower than the doping concentration of the semiconductor. This occurs as a result of the gate's positive charge exerting a force that will push the mobile holes into the semiconductor. Consequently, the semiconductor experiences a reduction of mobile carriers at the interface, resulting in a negative charge caused by the presence of ionized acceptor ions in the space charge region. The E_v bends downwards due to the E_F of the semiconductor substrate is lower than the E_F of metal.

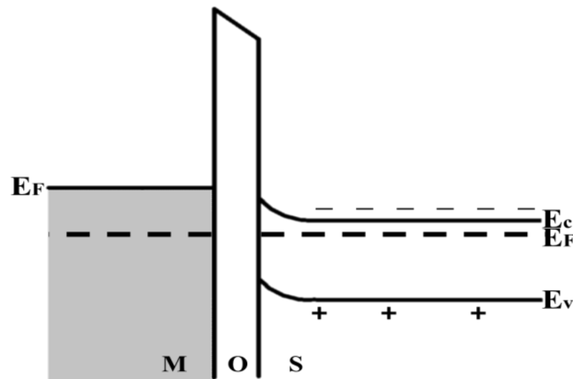

Figure 2.4 Energy band diagram of n-type semiconductor in depletion region ($V_g < 0$) [88].

Further increasing the negative bias ($V_g << 0$) will lead to an inversion condition. As seen in Figure 2.5, the minority carriers, which are holes are more than the majority carriers (electrons) near the oxide-semiconductor interface. Thus, the surface region will change from n-type to p-type. The E_F of the semiconductor substrate becomes lower than the E_F of the metal as compared to that of depletion condition.

Figure 2.5 Energy band diagram of n-type semiconductor in inversion region (V_g << 0) [88].

2.3.2 Defects in MOS

The reliability of MOS devices is very much reliant on the quality of the oxide layer, which is however, not immune to defects. The presence of defects allied with oxide charges and interface traps in MOS will impact the aforementioned MOS operation. An understanding of these defects and their origins is pivotal for the development of reliable MOS devices. Figure 2.6 depicts an example of MOS structure in which the oxide layer is comprised of SiO_2-SiO_x that will be used to discuss in detail the various defects found in MOS devices.

Figure 2.6 Possible defects in Si-based MOS device [89].

2.3.2(a) Oxide Charges

The performance and reliability of MOS devices are intricately linked to the quality of the oxide layer and the presence of defects within it. Understanding the nature, origin and impact of various oxide charges is essential for the continued advancement of semiconductor technology. Through improved fabrication techniques, effective passivation methods and stringent process controls, it is possible to mitigate the adverse effects of these defects, thus paving the way for more reliable and high-performance MOS devices. As the semiconductor industry continues to evolve, addressing the challenges posed by oxide charges will remain a critical area of focus, ensuring the continued progression of electronic technology.

Oxide charges that can be found in MOS devices can be categorized into four distinct categories as follows:

i) Mobile ionic charge (Q_m)- It is distributed throughout the oxide layer and can be linked to the presence of alkali ions, including sodium (Na^+), potassium (K^+) and lithium (Li^+). The interactions can be generated by high temperatures and the application of a bias voltage. It can lead to instability in device characteristics, such as threshold voltage shifts over time, particularly in high-temperature environments [89].

ii) Oxide trapped charge (Q_{ot})- It originates from charges trapped in the oxide due to defects, such as oxygen vacancies or other imperfections, which are introduced during device fabrication, particularly under high electric fields or radiation. The Q_{ot} can be a negative or positive charge depending on either trapped holes or electrons. The detection of Q_{ot} will

cause threshold voltage shifts and affect device reliability, particularly under stress conditions, such as bias temperature instability [89].

iii) Fixed oxide charge (Q_f)- The Q_f exists as a positive charge and it is situated at few nanometers away from the interface between SiO_2 and Si. The charging and discharging of Q_f are not easily altered during device operation. It is often associated with imperfections in the oxide growth process or contamination, which may cause a shift in the flat-band voltage or the threshold voltage [89].

iv) Interface trapped charge (Q_{it})- This Q_{it} is found at the interface between Si and SiO_2, which can be positively or negatively charged. The presence of these trapped charges can be attributed to several factors, including structural defects, oxidation-induced defects and impurities. It can produce trivalent Si, broken Si-H bonds, oxygen-related defects and Si impurities. In addition, Q_{it} is electrically active and causes the stretch-out of the capacitance-voltage (*C-V*) curve, as shown in Figure 2.7. It also creates additional states within the E_g, resulting in a premature E_B [89].

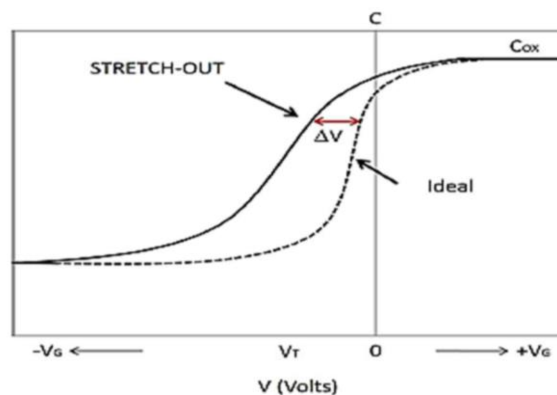

Figure 2.7 The typical ideal and non-ideal *C-V* curve for MOS device using n-type substrate [90].

2.3.2(b) Interface State Density (D_{it})

Interface state density (D_{it}) is used as an estimation to evaluate interface quality between the oxide and semiconductor layer. For Si-based MOS devices, the presence of Si dangling bonds at the interface between Si and SiO_2 has been identified as a significant factor contributing to a decrease in the accumulation capacitance and the degradation of the ideal *C-V* characteristics. The existence of the interface states has led to an increase in states within the Si E_g, resulting in charge trapping and Coulomb scattering at the interface, thus inducing premature E_B. The enhancement of the Si-SiO_2 interface can be achieved through the reduction of Si dangling bonds. Consequently, researchers have proposed that the diffusion of hydrogen atoms to form the Si-H bond can effectively address this issue [91]. The introduction of hydrogen was done by annealing process where SiO_2 was post annealed in forming gas ambient (80% N_2, 10% H_2) and in-situ annealing in hydrogen gas ambient [92]. The results showed that the hydrogen had successfully passivated the Si dangling bonds and reduced D_{it} of Si and SiO_2 interface. Nonetheless, the primary concern with the presence of D_{it} in Si MOS is the Si-H bond, which is more vulnerable to breaking than the Si-Si bond, which leads to the lattice mismatch between the substrate and the oxide layer [93].

However, the SiC MOS device is different from that of Si and it is more complicated due to the presence of carbon, which results in a high D_{it} at the SiO_2/SiC interface. Throughout the process of oxidation and SiO_2 growth, the carbon present on the C-face will transform into CO or CO_2 since it possesses the highest oxidation rate compared to Si-face [94,95]. The incomplete CO ejection causes carbon clusters and carbon interstitials that will remain on the interface as interface traps [94]. Furthermore, carbon has the ability to undergo oxidation, resulting in the formation of

many unsaturated carbon atoms on the surface of the oxide. These unsaturated carbon atoms could be the source of the interface traps. In addition, the creation of SiO_2 during the oxidation process had probably produced incomplete oxidized Si, which induced to the increase in D_{it}. Therefore, in order to effectively mitigate D_{it} in SiC MOS capacitors, it is essential to properly investigate the underlying causes of the presence of interface traps.

In order to address these issues, the researchers found an effective method to reduce the residual carbon element that affects the interface quality of SiO_2 and SiC by improving the conventional Si-MOS-based annealing process [96]. This was done by introducing re-oxidation annealing after the typical annealing process at the same or lower temperature. The primary objective of the first annealing stage is to facilitate the oxidation of the incomplete carbon element, while the subsequent annealing step aims to further oxidize the SiC at the interface between SiO_2 and SiC substrates [97]. Another approach is to anneal the SiC-MOS based in nitrogen ambient. The nitrogen atoms were able to go into the SiC and SiO_2 interface to repair the Si dangling bond by creating the N-Si bond, thus reducing the D_{it} [98]. In addition, researchers also reported that introducing the nitrogen atoms during the first stage of the annealing process can help to reduce D_{it} near the conduction band edge. Nevertheless, the presence of nitrogen ions had detrimental effects by increasing the effective oxide charge and subsequently causing the shifting of the flat-band voltage [99]. It was also proposed that the substitution of the PL material SiO_2 with a lower conduction offset of high-k material can help to reduce the D_{it} value. The utilization of SiO_2 as the gate material would also contribute to reliability issues since the SiC-based devices are supposed to operate at high electric field. This problem is not only because of the poor quality of SiO_2/SiC interface but also because of the relatively low-k of SiO_2.

2.4 Limitations of SiO_2 as an Oxide Layer in MOS Technology

SiO_2 has been a foundational material in the development of MOS technology due to its excellent insulating properties, thermal stability and compatibility with Si substrates. However, as semiconductor technology advances and device dimensions continue to shrink, SiO_2 faces several significant limitations. As the SiO_2 layer becomes very thin (< 2 nm), it suffers from increased leakage current due to quantum tunnelling [100]. This leakage current not only raises power consumption but also reduces the reliability of the device, making SiO_2 less suitable for ultra-scale devices. Moreover, as the thickness is reduced, the E_B of SiO_2 also decreases, where the passivating properties are compromised, leading to device failure [101]. This limitation restricts the voltage range over which the device can operate reliably, especially in high-performance applications where high E_B is common. In addition, SiO_2 also possesses a relatively low-*k* of 3.9 [102]. The low-*k* of SiO_2 limits the gate capacitance, which in turn limits the control the gate has over the channel [103]. The SiO_2 PL can also degrade over time due to exposure to high electric fields and radiation [104,105]. This degradation can result in increased leakage currents, shifts in threshold voltage and eventual device failure [104,105]. Ensuring the long-term reliability of SiO_2 in demanding environments is challenging, particularly for applications that require high reliability, such as aerospace, electric transportations and medical devices.

Consequently, research and development are focused on finding alternative high-*k* materials that can better meet the needs of advanced semiconductor devices, providing higher performance and reliability for the next generation of electronics. A higher-*k* is desirable in MOS devices to increase the capacitance without reducing the oxide thickness.