

**ENHANCING EFFICIENTNET-YOLOV4 FOR
INTEGRATED CIRCUIT DETECTION ON
PRINTED CIRCUIT BOARDS**

TAY SHIEK CHI

UNIVERSITI SAINS MALAYSIA

2024

ENHANCING EFFICIENTNET-YOLOV4 FOR INTEGRATED CIRCUIT DETECTION ON PRINTED CIRCUIT BOARDS

by

TAY SHIEK CHI

**Thesis submitted in fulfilment of the requirements
for the degree of
Master of Science**

October 2024

ACKNOWLEDGEMENT

I would like to express my sincere gratitude to all those who supported and contributed to completing this research. First and foremost, I would like to extend my deepest appreciation to my supervisor, Dr. Mohd Nadhir bin Ab Wahab, for his guidance, motivation, immense knowledge, and continuous support throughout the research process. Dr. Ahmad Sufril Azlan Mohamed and Dr. Mohd Halim bin Mohd Noor also provided valuable insights and suggestions during the development of this project. I would like to thank Associate Professor Mohd Azam Osman and Associate Professor Dr. Wan Mohd Nazmee Wan Zainon for their valuable comments and feedback on my reports and presentations.

I would like to acknowledge the financial support provided by Collaborative Research in Engineering, Science and Technology (CREST). Their support has enabled me to carry out this research and present the findings. I would also like to extend my appreciation to the School of Computer Sciences, Universiti Sains Malaysia and SanDisk Storage Malaysia Sdn. Bhd (SDSM) for providing the resources and materials required for this research. Their collaboration was invaluable in facilitating the data collection and experimentation processes. I am grateful to my colleague, Brigitte Liao Wei Jie, for her valuable discussions, insights, and encouragement during this research. Finally, I express my heartfelt appreciation to my family for their encouragement and understanding throughout my academic journey. Their support is what drives me to achieve. My sincere thanks to all of the above and to anyone who contributed directly or indirectly to the completion of this research.

Sincerely appreciate your help and support. Thank you all!

TABLE OF CONTENTS

ACKNOWLEDGEMENT	ii
TABLE OF CONTENTS.....	iii
LIST OF TABLES	vi
LIST OF FIGURES	vii
LIST OF SYMBOLS	ix
LIST OF ABBREVIATIONS	xi
LIST OF APPENDICES	xiii
ABSTRAK	xiv
ABSTRACT	xvi
CHAPTER 1 INTRODUCTION.....	1
1.1 Background	1
1.2 Motivation	5
1.3 Problem Statement	7
1.4 Research Questions	10
1.5 Research Objectives	10
1.6 Expected Contributions	11
1.7 Scope of the Study.....	12
1.8 Thesis Organisation.....	13
CHAPTER 2 LITERATURE REVIEW.....	14
2.1 Introduction	14
2.2 Overview of PCB Inspection and IC Detection	15
2.3 Neural Network Approach	16
2.3.1 Deep Learning-based Object Detectors.....	16
2.3.1(a) One-Stage Detector: YOLO	17
2.3.1(b) One-Stage Detector: SSD	22

2.3.1(c)	One-stage Detector: RetinaNet	22
2.3.1(d)	Two-Stage Detector	23
2.3.2	Other Neural Network-based Methods	25
2.4	Dataset for PCB Inspection	27
2.5	Discussion	29
2.6	Summary	34
CHAPTER 3 METHODOLOGY.....		35
3.1	Introduction	35
3.2	Research Framework.....	35
3.3	Network Design.....	39
3.3.1	Backbone (EfficientNet)	41
3.3.2	Neck	47
3.3.3	Head (YOLO).....	49
3.3.4	Backbone Integration and Architectural Enhancements	51
3.3.5	Fine-Tuning and Optimisation of the EfficientNetv2-L- YOLOv4 Model	56
3.4	Evaluation of the Proposed Method	60
3.4.1	Accuracy.....	60
3.4.1(a)	Confidence Score and IoU Score.....	60
3.4.1(b)	Confusion Matrix.....	62
3.4.1(c)	Precision, Recall, F1-score and mAP	63
3.4.2	Inference Speed	64
3.5	Datasets	65
3.5.1	Original Dataset.....	66
3.5.2	Augmented Dataset	67
3.5.3	Unseen Data	71
3.6	Summary	72

CHAPTER 4	RESULT ANALYSIS.....	73
4.1	Introduction	73
4.2	Experimental Setup	73
4.2.1	Experimental Datasets Collection	73
4.2.2	Hardware and Software details for Experimental Model Training	74
4.3	Experimental Results.....	74
4.3.1	Backbone Comparison	75
4.3.2	Experiment on Anchor Size, Loss Function and BoF Configurations.....	78
4.3.3	Analysis of Unseen Data	83
	4.3.3(a) Test the Robustness of the Model with Different Augmentation Methods	83
	4.3.3(b) Failed Analysis for Unseen Data	86
4.4	Performance Comparison between Different Models	88
4.4.1	IoU Graph.....	93
4.4.2	Confusion Matrix	95
4.5	Summary	97
CHAPTER 5	CONCLUSION AND FUTURE RECOMMENDATIONS.....	98
5.1	Conclusion.....	98
5.2	Recommendations for Future Research	100
REFERENCES.....		102
APPENDICES		

LIST OF TABLES

	Page
Table 2.1 Datasets Related to PCB Inspection.....	27
Table 2.2 Overview of Object Detection Methods and Their Backbone Architectures.	30
Table 2.3 Overview of Backbone Architectures.	31
Table 3.1 Baseline Network Architecture of EfficientNet-B0 (Armughan, 2020).	46
Table 3.2 Baseline Network Architecture of EfficientNetv2-S (Tan & Le, 2021).	46
Table 3.3 Benchmark Analysis of Pre-trained CNN Models from Keras (Keras, n.d.).....	47
Table 3.4 BoF and BoS for Detector in YOLOv4 (Bochkovskiy et al., 2020).	50
Table 3.5 Confusion Matrix Definition.....	62
Table 3.6 Examples of Noisy Images in the Dataset.....	67
Table 3.7 List of Augmentations Used in The Study.....	69
Table 3.8 Number of Datasets.....	70
Table 4.1 Performance Comparison of Different EfficientNet Backbones.	76
Table 4.2 Performance Comparison of Different Settings of the Proposed Model.	78
Table 4.3 Results of Data Augmentation Methods Applied to the Proposed Model.	84
Table 4.4 Examples of Failure Causes in Unseen Data.	87
Table 4.5 Model Evaluation.	89
Table 4.6 Confusion Matrix of the Compared Models.	96

LIST OF FIGURES

	Page
Figure 1.1 Typical Process Flow of PCBA (Khasawneh, 2019).....	2
Figure 2.1 Overview of Literature Reviewed.	14
Figure 2.2 Overall Covered State-Of-The-Art Methods.	15
Figure 2.3 Overall Process of SRCNN with YOLOv3 (H. Chen et al., 2019). ...	19
Figure 2.4 Differences in Detection Processes Between Conventional and Deep Learning-Based Methods (Mehta et al., 2020).	25
Figure 2.5 Workflow of PCBSegClassNet for Segmentation and Classification (Makwana et al., 2023).	26
Figure 3.1 Overall Stages of the Research.	38
Figure 3.2 Scheme for Integrating the Proposed Method into An Industrial Server.	39
Figure 3.3 Type of Model for Object Detectors in Each Part- Backbone, Head and Neck (Bouraya & Belangour, 2021).....	40
Figure 3.4 Compound Scaling Method of EfficientNet (Tan & Le, 2019).	43
Figure 3.5 Structural of MBConv, Fused-MBConv, and SE block (Albattah et al., 2022).	45
Figure 3.6 SPP Block.	48
Figure 3.7 Feature Network Design of FPN and PANet (Tan et al., 2020).	48
Figure 3.8 Components in YOLOv4 Architecture.	49
Figure 3.9 Architecture of the CSPDarkNet-53 Backbone in Original YOLOv4.....	53
Figure 3.10 Architecture of the EfficientNet-B0 Backbone in YOLOv4.....	54
Figure 3.11 EfficientNetv2-L Backbone Architecture in the Proposed EfficientNetv2-L-YOLOv4 Model.	55

Figure 3.12	YOLOv4 Detector Architecture in the Proposed EfficientNetv2-L-YOLOv4 Model.	56
Figure 3.13	9 Anchor Size Set Distribution Diagram for (a) 416 Image Size and (b) PCB Anchor Size Set.	57
Figure 3.14	Ratio of Object Size (Chip) to Image Size Before Augmentation.	71
Figure 3.15	Ratio of Object Size (Chip) to Image Size After Augmentation.	71
Figure 3.16	Example Image from (Fazle, 2021).	72
Figure 4.1	IoU Graph of L-ciou-y3-BoF.	82
Figure 4.2	Loss Graph of L-ciou-y3-BoF.	82
Figure 4.3	Analysis of Failure Causes in Unseen Data Predictions.	88
Figure 4.4	Accuracy Strength Diagram of Evaluated Models.	93
Figure 4.5	Inference Speed Strength Diagram of Evaluated Models.	93
Figure 4.6	IoU Graph of EfficientNetv2-L-YOLOv4 (Proposed Method).	94
Figure 4.7	IoU Graph of EfficientNet-B0-YOLOv4 (Baseline Method).	94
Figure 4.8	IoU Graph of EfficientNet-B7-FasterRCNN.	95
Figure 4.9	IoU Graph of YOLOv4.	95

LIST OF SYMBOLS

β	Variance for each predicted box with an IoU > threshold
e^+/e^-	Additional coefficients that are either greater than or less than 1
m	Total number of objects in the image
n	Number of predicted boxes whose IoU < threshold
$loss_{obj}$	Objectness loss
$loss_{coord}$	Coordinates loss
$loss_{class}$	Classification loss
P_x	Probability associated with a specific class x
γ	A modulating factor used in focal loss to address class imbalance by down-weighting easy examples, 1.5 in the experiment
$S*S$	Number of grid points in the input image
1_{ij}^{obj}	Indicator function that determines whether an object exists in grid cell (i, j)
$t \in classes$	t is a member or element of the set classes
$\hat{P}_i(t)$	Predicted probability for class t at grid point i
$P_i(t)$	Ground truth probability for class t at grid point i
d	Depth of the neural network (number of layers)
w	Width of the neural network (number of channels per layer)
r	Resolution of the input or feature maps in the network
α	Scaling factor for the depth of the network.
β	Scaling factor for the width of the network
γ	Scaling factor for the resolution of the network
Φ	User-specified coefficient controlling resource allocation for scaling depth, width, and resolution
\approx	Symbol indicating approximation or near equality
$s.t.$	Stands for "subject to"

$\rho^2(b, b^{gt})$	Square Euclidean distance between the central points of predicted boxes b and $b^{\text{ground-truth}}$
c	Diagonal length of the smallest enclosing box covering the two boxes
α	Positive trade-off parameter balancing aspect ratio consistency
v	Consistency of aspect ratio
w	Width
h	Height
Δ	Distance cost, which accounts for the angle cost (Λ)
Λ	Angle cost
Ω	Shape cost
x	Ratio related to the angle cost
σ	Euclidean distance between the centres of the predicted and ground truth bounding boxes
C_h	Height difference between the centres of the ground truth and predicted bounding boxes
ρ_x, ρ_y	Normalised squared differences between the x-coordinates and y-coordinates of the centres of the predicted and ground truth bounding boxes, respectively
γ	Trade-off parameter in the distance cost, defined as $\gamma = 2 - \Lambda$
c_w, c_h	Width and height of the smallest enclosing box, respectively
b_{c_x}, b_{c_y}	x-coordinate and y-coordinate of the centre of the predicted bounding box, respectively
$b_{c_x}^{gt}, b_{c_y}^{gt}$	x-coordinate and y-coordinate of the centre of the ground truth bounding box, respectively
ω_w, ω_h	Normalised width and height differences between the predicted bounding box and the ground truth bounding box, respectively
θ	Measure how much the shape costs
n	Number of output detections
k	Number of points at different recall values for which precision is computed
C	The number of classes

LIST OF ABBREVIATIONS

AI	Artificial Intelligence
ANNs	Artificial Neural Networks
AOIs	Automatic Optical Inspection systems
AP	Average Precision
AutoML	Auto Machine Learning
BCE	Binary Cross-Entropy
BiFPN	Bidirectional Feature Pyramid Network
BoF	Bag of Freebies
BoM	Bill of Materials
BoS	Bag of Specials
CAROI	Context-Aware ROI
CIoU	Complete Intersection over Union
CLAHE	Contrast-Limited Adaptive Histogram Equalization
CmBN	Cross mini-Batch Normalization
CNN	Convolutional Neural Networks
CSP	Cross Stage Partial
DIoU	Distance Intersection over Union
DSSD	Deconvolutional Single Shot Detector
ECLAD-Net	Electronic Component Localization and Detection Network
EDSR	Enhanced Deep Residual Networks for Single Image Super-Resolution
E-ELAN	Extended Efficient Layer Aggregation Network
FCOS	Fully Convolutional One-Stage Object Detection
FPN	Feature Pyramid Network
FPS	Frames Per Second
FLOPS	Floating Point Operations per Second
GIoU	Generalized Intersection over Union
GsIoU	Gaussian Intersection of Union
HVCs	Homogeneous Vector Capsules
ICs	Integrated Circuits
IoT	Internet of Things
IoU	Intersection over Union

LB	Loss Boosting
MAM	Multiscale Attention Module
mAP	mean Average Precision
Mask R-CNN	Mask Region-based Convolutional Neural Network
MBConv	Mobile Inverted Bottleneck
ML	Machine Learning
M2Det	Multi-level Feature Pyramid Network for Object Detection
NAS	Neural Architecture Search
NSS	Non-Linear Scale Space
OCR	Optical Character Recognition
PANet	Path Aggregation Network
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PR	Precision-recall
RCNN	Regions with Convolutional Neural Network
ReLU	Rectified Linear Unit
R-FCN	Region-based Full Convolutional Network
ROI	Regions of Interest
RPN	Region Proposal Network
SAT	Self-Adversarial Training
SIoU	SCYLLA-IoU
SE	Squeeze-and-Excitation
SGD	Stochastic Gradient Descent
SMD	Surface-Mounted Device
SMT	Surface Mount Technology
SPI	Solder Paste Inspection
SPN	Similarity Prediction Network
SSD	Single-Shot Multibox Detector
SPP	Spatial Pyramid Pooling
SRCNN	Super-Resolution Convolutional Neural Network
TDD-Net	Tiny Defect Detection Network
THT	Through-Hole Technology
VGG	Visual Geometry Group
YOLO	You Only Look Once

LIST OF APPENDICES

Appendix A	LIST OF PUBLICATIONS
Appendix B	DATASET: NO. OF IMAGES PER FOLDER
Appendix C	PLOT OF MAP, PRECISION, RECALL, LEARNING RATE EPOCH LOSS AND CONFUSION MATRIX
Appendix D	FAILED ANALYSIS FOR UNSEEN DATA

MENINGKATKAN EFFICIENTNET-YOLOV4 UNTUK PENGESANAN LITAR BERSEPADU PADA PAPAN LITAR BERCETAK

ABSTRAK

Pemeriksaan visual automatik papan litar bercetak (PCB) adalah penting untuk memastikan kualiti dan fungsi PCB sepanjang proses pembuatan. Mengesan litar bersepadu pada PCB dengan tepat merupakan cabaran yang signifikan dalam pemeriksaan automatik kerana pelbagai saiz dan jenis komponen, serta pelbagai cetakan dan tanda pada PCB yang menyukarkan pengesanan objek. Tesis ini menangani kerumitan ini dengan mencadangkan algoritma yang dipertingkatkan, EfficientNet-YOLOv4. Metodologi penyelidikan menggabungkan keupayaan pengekstrakan ciri unggul EfficientNet sebagai rangkaian tulang belakang dengan keupayaan penyetempatan objek yang tepat dari YOLOv4—gabungan dua kelebihan yang unik berbanding kaedah lain yang mungkin bergantung pada algoritma penyetempatan yang kurang canggih. Untuk memastikan keupayaan generalisasi model, pelbagai teknik augmentasi data, seperti kabur, penyimpangan grid, dan pelarasan kecerahan rawak, telah digunakan untuk mensimulasikan variasi dunia sebenar. Eksperimen dan penilaian yang meluas menunjukkan keberkesanan dan ketahanan algoritma yang dicadangkan dalam susun atur PCB yang kompleks, serta keupayaannya untuk menyesuaikan diri dengan variasi warna dan kecerahan yang rawak, mengatasi prestasi model pemeriksaan PCB yang lain. Kaedah yang dicadangkan, EfficientNetv2-L-YOLOv4, berjaya mencapai skor F1 yang tinggi iaitu 99.22 dengan kelajuan inferens 0.135 saat. Algoritma ini juga melebihi prestasi EfficientNet-B7-FasterRCNN dan YOLOv4 asal, mencapai skor F1 sebanyak 98.96 dan kelajuan inferens 0.102 saat apabila dilatih dengan saiz kelompok 4. Penemuan

penyelidikan ini menekankan kepentingan rangkaian pengekstrakan ciri yang berkesan dalam pengesanan objek dengan menggunakan teknik penskalaan yang canggih. Pembangunan algoritma EfficientNet-YOLOv4 yang dibentangkan dalam tesis ini bukan sahaja menangani cabaran segera pengesanan litar bersepadu pada PCB tetapi juga menyumbang kepada bidang penglihatan komputer dan pengesanan objek yang lebih luas. Integrasi berjaya algoritma EfficientNet-YOLOv4 yang dipertingkatkan (EfficientNetv2-L-YOLOv4) dalam senario pembuatan sebenar berpotensi untuk membolehkan proses pemeriksaan komponen automatik sepenuhnya dan mengurangkan campur tangan manusia semasa proses pengesanan.

ENHANCING EFFICIENTNET-YOLOV4 FOR INTEGRATED CIRCUIT DETECTION ON PRINTED CIRCUIT BOARDS

ABSTRACT

Automated visual inspection of printed circuit boards (PCBs) is vital for ensuring the quality and functionality of PCBs throughout the manufacturing process. Accurately detecting integrated circuits (ICs) on PCBs presents a significant challenge in automated inspection due to the wide range of component sizes and types, as well as various printing and markings on the PCB, which complicate object detection. This thesis addresses these intricacies by proposing an improved algorithm, EfficientNet-YOLOv4. The research methodology combines the high-performance feature extraction capabilities of EfficientNet as the backbone network with the precise object localisation capabilities of YOLOv4, a dual advantage unique compared to other methods that may rely on less sophisticated localisation algorithms. To ensure the model's generalisation ability, various data augmentation techniques, such as blur, grid distortion, and random brightness adjustments, were employed to simulate real-world variations. Extensive experiments and evaluations demonstrate the proposed algorithm's effectiveness and robustness in complex PCB layouts, as well as its adaptability to varying colour and brightness randomness, surpassing the performance of other PCB inspection models. The proposed method, EfficientNetv2-L-YOLOv4, successfully achieves a high F1-score of 99.22 with an inference speed of 0.135 seconds. The algorithm also surpasses EfficientNet-B7-FasterRCNN and the original YOLOv4, achieving an F1-score of 98.96 and an inference speed of 0.102 seconds when trained with batch size 4. The research findings emphasise the significance of effective feature extraction networks in object detection by utilising advanced scaling

techniques. The development of the EfficientNet-YOLOv4 algorithm presented in this thesis not only addresses the immediate challenges of IC detection on PCB but also contributes to the broader field of computer vision and object detection. The successful integration of the improved EfficientNet-YOLOv4 algorithm (EfficientNetv2-L-YOLOv4) in real manufacturing scenarios has the potential to enable a fully automated component inspection process and reduce human intervention during the detection process.

CHAPTER 1

INTRODUCTION

This chapter provides an overview of the research, including the background of printed circuit board (PCB) inspection in manufacturing and related object detection techniques. It explains the motivation, problem statement, and objectives of the research. Contributions to realising the expectations are stated, and the scope and process for conducting this study are also included. Finally, a brief overview of the structure of this paper is given.

1.1 Background

Since 2016, the world has entered the fourth industrial revolution, "Industry 4.0", which focuses on interconnection through the Internet of Things (IoT), automation, machine learning, and real-time data to provide more comprehensive and more innovative products, processes, and factories (Sharma et al., 2021). In Industry 4.0, smart technologies such as Internet of Things (IoT) and artificial intelligence (AI) are revolutionising the automation and inspection of supply chains (Jahani et al., 2021). Manufacturing is one of the major industries best positioned to leverage artificial intelligence and machine learning technologies to drive the growth of global supply and value chains. Furthermore, it can help the digital transformation of factories by streamlining machine supervision and automating industrial processing tasks that previously had to be handled by human workers. The main idea of Industry 4.0 manufacturing is to develop autonomous and automated industrial processing, which requires high-quality, precise, and reliable electronic production equipment.

Product quality standards serve as the benchmarks to satisfy the high consumption demand for electronic components, with visual inspection playing a

crucial role in maintaining product quality throughout the electronics manufacturing process. Machine vision is widely used in electronics manufacturing, mainly embodied in four aspects: measurement, inspection, identification, and positioning, especially printed circuit board inspection based on intelligent vision technology (J. Li et al., 2019). Printed circuit boards are the heart of electronics; they are circuit boards with lines, copper or gold tracks connected electronically to electronic components. A PCB with mounted components is called an assembled PCB, and its manufacturing process is known as PCB assembly or PCBA (Sasmita, 2018). The two main types of modern PCB assembly technologies are Surface Mount Technology (SMT) and Through-Hole Technology (THT), where SMT is considered more reliable than THT (J. He et al., 2021). Figure 1.1 shows a typical process flow of PCBA.

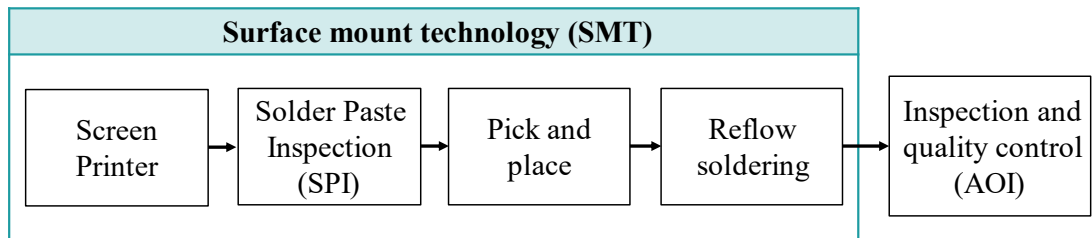


Figure 1.1 Typical Process Flow of PCBA (Khasawneh, 2019).

Various inspection methods, including manual, automatic optical, and X-ray inspection, are employed to check for errors and misalignments (Sasmita, 2018). Traditional manual visual inspection of PCBs is usually performed by human operators. However, this method is inherently inefficient, time-consuming, and susceptible to operator error due to the restrictions imposed by chronic weariness and eye strain limitations; human visual examination can only approximate actual quality levels (Zakaria et al., 2020). Electronic industries need non-contact automation methods to replace traditional manual visual inspection, especially for PCBA (Fan et al., 2021). Therefore, most electronics industries are applying automatic optical

inspection systems (AOIs), an application of machine vision for quality inspection to reduce the false selection of defects in production lines.

Automated visual PCB inspection can solve the difficulties of manual inspection and ensure the functionality and quality of PCBs during the manufacturing process because the performance and reliability of PCBs depend on the quality of the fabrication and assembly of boards. AOI is an inspection method suitable for large batches of PCBs. During the inspection and quality control stage, AOI machines can process a high quantity of PCBs at high speed in a relatively short time by using a series of high-powered cameras arranged at different angles to capture PCB images and view solder connections (Singh et al., 2019).

Component detection is essential in PCB automated production monitoring (J. Li et al., 2019). During the pick-and-place process of SMT, there may be issues such as component shifting or missing components, and the mounted components may deviate from the ideal or designed position on the wet solder paste (Cao et al., 2019). These issues are typical manufacturing defects faced by PCB assemblers. Therefore, there is a need to enhance automated PCB inspection tools to maximise efficiency and enable fast and accurate early fault detection at all stages of production. Identifying the actual location of the component can also be used to identify the characters marked on the PCB component and for PCB recycling. Detecting fine-pitch integrated circuits on PCBs is always challenging due to the increasing complexity of PCB boards containing various semiconductors with traces, vias, and markings. Numerous state-of-the-art techniques for automated PCB detection have been developed using computer vision, image processing, machine learning, and deep learning across the visual spectrum (Mallaiyan Sathiaseelan et al., 2021).

The image processing technique is a straightforward computer vision method for detection, but it may easily be affected by the image quality and background. Referential comparison methods such as template matching and image subtraction often require golden or reference samples for accurate feature comparison. With the advent of the Industry 4.0 era, the AOI algorithms have been further enhanced by combining machine learning and deep learning techniques, which can significantly improve the results and speed of the inspection process (Abd Al Rahman & Mousavi, 2020). Computer vision with machine learning enables higher levels of understanding based on image information and automates analysis. Deep learning is a sub-field of machine learning that encompasses multilayer neural network architectures. Deep learning can use its characteristics to extract deep-level features of objects and identify and locate objects based on these features (Shen et al., 2020). Deep learning has demonstrated excellent performance in research areas such as object detection and character recognition.

Object detection is a fundamental computer vision application that leverages machine learning or deep learning techniques to extract meaningful information from images. It consists of two main parts: image classification (identifying objects in images) and image localisation (determining the precise location of those objects). This localisation capability is particularly relevant in PCB component positioning detection tasks. Deep learning employs supervised learning to train and learn from large amounts of labelled data, allowing it to predict labels without requiring manual feature extraction. Deep learning offers several advantages in PCB component defect detection, with fast detection speed, high accuracy, and strong adaptability (Shen et al., 2020). Another key advantage of using neural network models is that they will continue improving when training data increases. However, a significant challenge lies

in creating a sufficiently large and annotated training database, as mentioned in the work by Dai et al. (2018). Convolutional Neural Networks (CNNs) are among the most popular deep neural networks, comprising multiple convolutional, non-linear, and pooling layers, with feature extraction processes embedded in the hidden layers. Examples of neural network-based object detection algorithms: You Only Look Once (YOLO), Single Shot Detector (SSD), Region-Based Convolutional Neural Networks (R-CNN), Faster R-CNN, and Region-based Fully Convolutional Network (R-FCN). These algorithms leverage the power of neural networks to detect and localise objects accurately in images, enabling efficient and effective object detection in various applications, including PCB inspection.

Most object detection techniques employed in PCB assembly are mainly used to identify and classify various electrical components (resistors, capacitors, integrated circuits) or to detect and localise common defects: soldering defects (open circuits, excess solder), component defects (missing component, misaligned component) on the printed circuit board (Houdek & Design, 2016). This research focuses on detecting the integrated circuit on the PCB. The primary purpose is to find the region of the chip components but not include their pins or soldering parts. Deep learning is well-established in industrial production, but its application in PCB detection is relatively rare (Shen et al., 2020). Therefore, researching and improving deep learning algorithms applied to PCB inspection in industrial production has great scientific and industrial value.

1.2 Motivation

The implementation of artificial intelligence in manufacturing facilities is gaining popularity. According to the 2020 MIT Technology Review Insights Survey,

approximately 58% of manufacturers adopt AI for quality control to increase speed and visibility across the supply chain and create more efficient or innovative manufacturing processes (Denis et al., 2020). The optimisation of PCB design and manufacturing is essential to meet the requirements of Industry 4.0 facilities. In the industry, optical inspection technology can be subdivided into manual inspection performed by human inspectors and automated optical inspection systems (Abd Al Rahman & Mousavi, 2020). However, manual inspection methods are time-consuming and error prone. Therefore, the electronics industry combines artificial intelligence to develop automated printed circuit board inspection systems. Currently, Western Digital-SanDisk Storage Malaysia is also working on using artificial intelligence to enhance AOI for PCB inspection. They need a region-finding algorithm to pinpoint the component of interest that could be judged, filtering out adjacent PCB prints and landmarks.

Automated inspection systems have shown promise in improving inspection speed and accuracy. However, there is still room for improvement, particularly in detecting integrated circuits on PCBs. Most of the target objects have a fixed shape in the manufacturing environment. So, it can develop a neural network to find regions of interest and segregate the images automatically. Implementing neural networks for object detection has become an essential trend with excellent success rates in robotic vision and surveillance. Object detection uses object localisation and classification to localise the presence of objects with bounding boxes and the type or class of localised objects in images applicable to IC detection tasks.

The complexity and component density of PCBs have increased significantly, making manual inspection methods error-prone. The motivation behind this paper is to develop an advanced autonomous inspection technique specially designed for PCBs

to detect ICs accurately. This paper explores deep learning techniques to tackle the detection task for semiconductors in PCB manufacturing. The study of integrated circuit detection has practical significance in industrial production because the production of PCB requires precise detection of electronic substrates to ensure quality. Identifying the position of the integrated circuit facilitates the improvement of inspection machines to identify defects and determine the polarity of chip components in printed circuit boards. Additionally, it can help develop applications that recognise and inspect characters printed on components connected to the PCBs (Gang et al., 2021). By leveraging deep learning approaches and state-of-the-art object detection algorithms, the aim is to improve detection accuracy, reduce false positives, and increase the efficiency of autonomous PCB inspections.

1.3 Problem Statement

Accurate detection and localisation of integrated circuits (ICs) on PCBs remain critical challenges within automated inspection systems due to the intricate variability in component sizes, orientations, and layouts. Existing object detection models encounter limitations in precisely localising these components, impacting detection precision and reliability. The field of object detection in PCB inspection faces substantial scope for improvement. Crucial object detection components, such as feature learning, backbone architecture, and proposal generation, demand focused attention (X. Wu et al., 2020). Challenges persist in handling feature scale issues and mastering multi-scale feature learning, which is essential for accurately identifying diverse ICs (X. Wu et al., 2020). Techniques such as Spatial Pyramid Pooling (SPP) or adaptive pooling facilitate analysis at multiple scales, enabling diverse object size and aspect ratio capture for object detection.

In industrial applications, where both speed and precision are crucial, one-stage detectors like YOLO offer significant processing speed advantages. However, this speed often comes at the expense of accuracy, especially compared to two-stage detectors (Cazorla & Hussain, 2024; Yao et al., 2021). YOLOv4, a popular one-stage detector, struggles to balance speed and precision in high-demand environments due to its traditional feature extractor, which loses spatial information as the resolution decreases, leading to inaccuracies in target localisation (H. Zhao et al., 2021). As a result, YOLOv4's trade-offs may not meet the stringent accuracy and efficiency requirements of modern industrial applications, highlighting the need to explore alternative backbone architectures to improve detection performance.

Pursuing a detection-aware backbone architecture that is learned directly from datasets becomes a compelling research avenue, particularly in addressing the inefficiency of current feature extraction networks in capturing the intricate details of ICs across diverse PCBs (X. Wu et al., 2020). The backbone network acts as the fundamental feature extractor for object detection, significantly influencing the model's performance (Jiao et al., 2019). However, the intricacies of identifying an ideal backbone architecture specifically tailored for object detection within the PCB datasets pose a critical challenge. Achieving an optimal equilibrium between speed and accuracy requires adaptive multi-level features and a well-designed backbone architecture (Jiao et al., 2019). The design of an optimal backbone architecture yields substantial enhancements in results but demands substantial engineering effort (X. Wu et al., 2020).

Exploration of strategies focusing on optimising backbone architectures represents a pivotal avenue in the quest for superior neural network designs tailored explicitly for distinct object detection tasks. Techniques such as Neural Architecture

Search (NAS), a fundamental aspect of Automated Machine Learning (AutoML), or adapting existing architectures, exemplified by models like EfficientNet, offer promising prospects in automating the search for optimal network structures. However, despite the efficiency-driven design of EfficientNet models, larger variants, while achieving higher accuracy, require increased memory and computational resources, leading to slower training processes (Tan & Le, 2021). This challenge underscores the need for developing models that strike a better balance between accuracy and computational efficiency, ensuring both high-performance and practical applicability in real-world scenarios.

Object detectors leveraging AutoML techniques have become a significant research focus, promising to streamline model development by automating processes like architecture search, hyperparameter optimisation, and feature engineering (Masood & Sherif, 2021; X. Wu et al., 2020). Hyperparameter settings significantly influence machine learning models' behaviour, complexity, and efficiency, requiring careful selection for optimal performance (Bischl et al., 2023; Pannakkong et al., 2022). However, iteratively fine-tuning these configurations, involving adjusting parameters like loss functions, anchor sizes, and other relevant techniques within the proposed methodology, remains an ongoing challenge. The lack of research on hyperparameter tuning leads to unexplored dimensions in machine learning and a notable absence of systematic analysis on parameter tuning practices in research papers (Simon et al., 2023). Many studies in machine learning overlook or omit explicit reporting on hyperparameter tuning, neglecting the fundamental role these settings play in shaping model performance across diverse datasets and tasks.

Factors contributing to this lack of emphasis on tuning may include the absence of suitable experimental setups, limited understanding of specific hyperparameters'

effects, time constraints, or knowledge gaps. Moreover, the computational demands inherent in training and tuning large-scale machine learning models pose additional challenges (Simon et al., 2023). This gap in comprehensive understanding and systematic exploration hinders the full realisation of machine learning algorithms' potential. Therefore, there is a need for systematic exploration and refinement of these configurations to improve object detection models' accuracy, robustness, and computational efficiency, particularly when applied to PCB datasets.

Exploration of advanced algorithms and techniques is essential to accurately locate and classify integrated circuits in challenging environments. Additionally, emphasis should be placed on creating diverse datasets, establishing standardised evaluation protocols, and exploring novel techniques to bolster the robustness and efficiency of detection models.

1.4 Research Questions

These research questions aim to uncover difficulties that need to be addressed to improve neural network-based object detection performance. These questions include:

1. Which backbone architecture with object detector yields the highest accuracy for chip detection within Printed Circuit Board (PCB)?
2. What model configurations within the identified backbone architecture maximise object detection performance for integrated circuits (ICs) on PCBs?

1.5 Research Objectives

This research focuses on designing a chip finder to detect components on a printed circuit board. Evaluating the system's robustness is another critical aspect of

assessing the proposed algorithm. To achieve this, here are the objectives to achieve it:

1. To enhance the YOLOv4 architecture's feature extraction capability by integrating the best-performing EfficientNet as the backbone network, aiming to achieve superior accuracy, precision, and recall compared to the baseline model in detecting integrated circuits (ICs) within printed circuit boards (PCBs).
2. To optimise the proposed model's configurations, including variations in loss functions, anchor sizes, and other pertinent techniques, aiming for improved performance metrics such as accuracy, precision, and recall.

1.6 Expected Contributions

This research significantly enhances object detection performance, particularly for ICs on printed circuit boards, by gaining valuable insights into architecture development and selection. Existing object detector architectures are modified and enhanced by building a deeper and more efficient feature extraction network. This achievement leverages EfficientNet, a neural network architecture developed through NAS, known for its ability to deliver optimal performance and efficiency. The evaluation and analysis of various backbone architectures integrated into the YOLOv4 framework for object detection within PCB datasets identify the most efficient variant of the EfficientNet backbone architecture. This identification contributes to the development of optimised architectures tailored specifically for IC detection tasks within PCB inspection.

Furthermore, the research iteratively optimises various model configurations, encompassing loss function variations and training techniques. This systematic refinement process develops a comprehensive understanding of fine-tuning strategies,

explicitly targeting the achievement of heightened accuracy and robustness in object detection tasks. Consequently, these efforts contribute to advancing efficient and reliable neural network-based object detection models within PCB datasets.

Finally, a comparative evaluation between the proposed method and existing PCB inspection algorithms or object detection frameworks is conducted. This evaluation, employing metrics such as F1-score, mean Average Precision (mAP), and inference speed, aims to discern the strengths and weaknesses of the proposed method. The findings provide valuable insights into the performance and efficacy of the developed approach within the context of PCB inspection.

1.7 Scope of the Study

This research explores the application of computer vision in artificial intelligence. The scope of this research covers object detection algorithms using a deep learning approach and delves into how to improve the performance of deep neural networks. The theories of neural networks and image processing techniques are studied and discussed to select appropriate methods for further development and improvement. Implementing the feature extraction network is the focus of this research, and fine-tuning the training setting aims to improve the accuracy of object detectors further. Image augmentation techniques for increasing data variability are also covered. Two types of datasets were trained—one collected from the PCB industry, and one transformed from the former. During the evaluation phase, several methods associated with PCB detection are employed to compare their performance with the proposed approach. The evaluation phase also uses two types of test data—one split from the original dataset and one separated from a different set of part numbers not seen by the model.

1.8 Thesis Organisation

This study is organised as follows. The next chapter reviews the relevant literature on object detection algorithms, particularly those applied to PCB inspection and electronic component detection. CHAPTER 3 describes the research methodology, including the data collection process and the selection and modification of the proposed algorithm. CHAPTER 4 describes the experimental setup and presents the results obtained from the evaluation process. The final chapter summarises the main findings of this study and presents recommendations and future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter explores numerous state-of-the-art electronic inspection techniques in computer vision, covering PCB components and defect detection, as well as inspection methods for non-PCB electrical components. The primary objective is to identify suitable algorithms for the present study. The chapter is organised as follows: Section 2.2 provides an overview of various PCB inspection methods employed in the industry. Section 2.3 discusses PCB inspection algorithms that leverage machine learning techniques, focusing on methods employing neural networks. Figure 2.1 and Figure 2.2 visually represent the fields and areas of literature covered. Section 2.4 compiles available datasets related to PCBs, while Section 2.5 delves into the key findings of the literature review chapter, emphasising insights gained for further research in PCB component detection. The chapter concludes with a summary in Section 2.6.

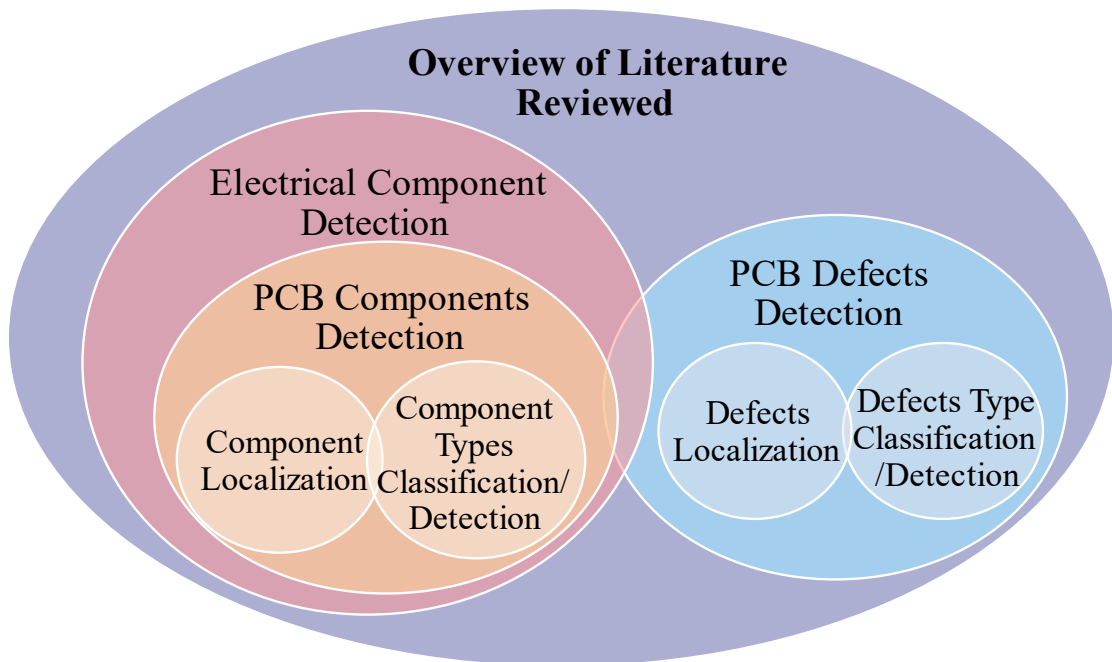


Figure 2.1 Overview of Literature Reviewed.

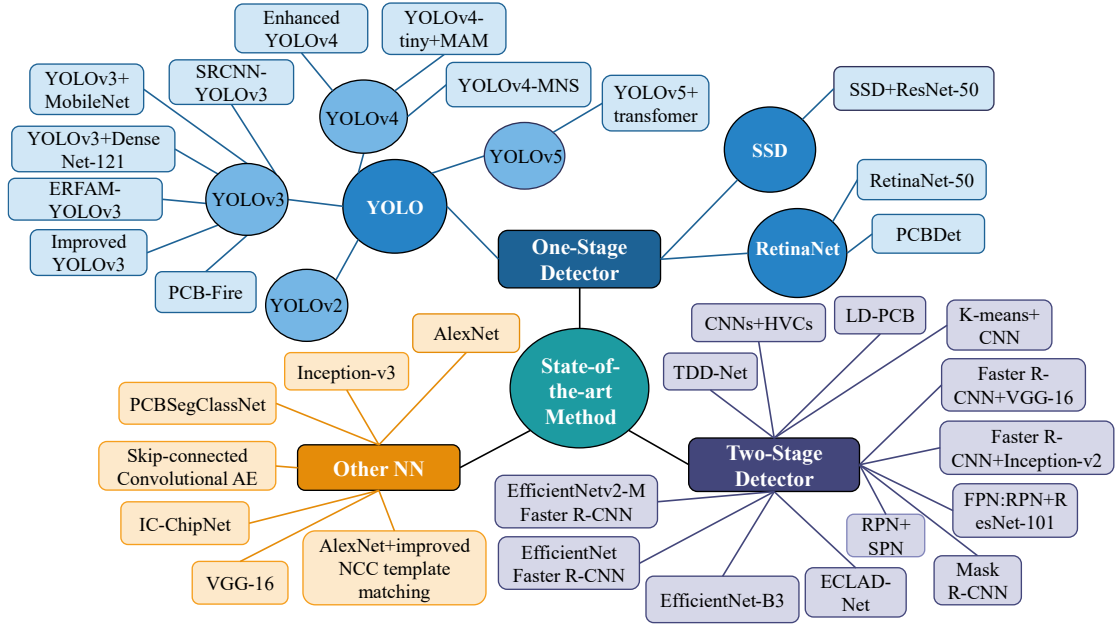


Figure 2.2 Overall Covered State-Of-The-Art Methods.

2.2 Overview of PCB Inspection and IC Detection

PCB inspection is employed to identify any potential defects or abnormalities in the assembly process of PCBs. Missing or misplaced components or incorrect component orientation affect the quality of the final product (D. Li et al., 2020). Integrated circuit detection involves the identification and localisation of ICs on a PCB. This process helps verify that the correct ICs are present on the PCB according to the design specifications to avoid faulty and malfunctioning circuitry. Moreover, identifying the ICs or labels on them can provide a record of the ICs used in a PCB assembly. They can also be utilised to automate PCB recycling processes, where identifying and extracting reusable components from discarded PCBs is essential for resource recovery and environmental sustainability (Mir & Dhawan, 2022).

Machine learning is a subfield of artificial intelligence that has evolved significantly from traditional pattern recognition and image processing methods to more advanced image understanding techniques (Khan & Al-Habsi, 2020). Modern advances in computer vision rely heavily on deep learning, a subfield of machine learning that

utilises multilayer artificial neural networks (ANNs). Deep learning algorithms, also known as deep neural networks, form the foundation for processing and analysing complex visual data. The subsequent section delves into the detection of PCBs through neural network-based approaches, specifically emphasising deep learning techniques.

The focus of the reviewed techniques and algorithms had predominantly centred around component detection, leveraging the capabilities of machine learning approaches. However, work dedicated to PCB component inspection had been relatively limited; therefore, this review also covered studies on PCB defect detection and common electrical component inspection to provide a more comprehensive understanding of PCB inspection.

2.3 Neural Network Approach

Machine learning algorithms, particularly those based on neural networks like deep learning, have the advantage of not requiring explicit programming with specific rules to define input expectations. Object detection is a common application in computer vision that leverages machine learning or deep learning to extract meaningful information from images. Object detection is crucial in determining the precise location and type of target objects, making it especially relevant for PCB component positioning detection. This section explores various types of deep learning-based object detectors and other neural network-based methods used in PCB inspection.

2.3.1 Deep Learning-based Object Detectors

Popular categories of deep learning-based object detectors included two-stage methods and one-stage methods. Two-stage methods tended to be precise in their predictions; they could be relatively slow due to the additional step of identifying regions of interest before classification (Reza et al., 2020). On the other hand, one-stage

methods performed object detection in a single step (Dave et al., 2016). These methods directly predicted the class labels and bounding box coordinates for all potential objects in the image without the need for explicit region proposal generation, which offered advantages in terms of speed and memory efficiency (J. Li et al., 2019).

2.3.1(a) One-Stage Detector: YOLO

The YOLO method, leveraging CNNs, is extensively employed in PCB assembly to facilitate real-time predictions. Lin et al. (2018) presented the YOLOv2 architecture, which enabled the automatic and rapid localisation of capacitors and the identification of their types in captured images. Most electronic component detections in PCB assembly preferred YOLOv3 over YOLOv2 as the object detector due to its Feature Pyramid Network (FPN) architecture, enabling multi-scale prediction and effective detection of small objects (R. Huang et al., 2019). YOLOv3 demonstrated the highest recognition rate of 92.2% compared to SSD, R-CNN, and RetinaNet in PCB component recognition (K. Zhang, 2023). Detecting PCB assemblies is crucial for recycling and defect inspection purposes. Silva et al. (2021) utilised a pre-trained YOLOv3 model, fine-tuned with the PCB DSLR dataset by Pramerdorfer and Kampel (2015), to detect ICs in waste PCBs for recycling.

Missing components were often an issue that needed to be addressed in PCB assembly. Khare et al. (2020) proposed a solution involving object detection (YOLOv3), image subtraction, and pixel manipulation, which achieved an accuracy of 75.48% in solving the problem of missing components in PCBs. To improve the YOLOv3 algorithm's capability of detecting small surface-mounted device (SMD) components on PCBs, a small target-sensitive YOLO output layer could be added (J. Li et al., 2019). This addition helped prevent the loss of feature information. However, it still exhibited weaknesses when the variance within the same category was significant.

In YOLOv3, the bounding box predictions rely on the anchor box concept (J. Li et al., 2021). However, mismatches between anchor and target sizes can impact performance. K-means clustering could address this by generating more suitable anchors based on the bounding boxes in the training dataset (S. H. Chen & Tsai, 2021). J. Li et al. (2019) applied k-means clustering to generate 12 anchor boxes for an improved YOLOv3 model in PCB detection. Another approach that focused on the anchor box concept, also presented by J. Li et al. (2021), was ERFAM-YOLOv3 (Effective Receptive Field Size and Anchor Size Matching in YOLOv3), designed for real-time electronic component detection. This method involves clustering, effective receptive field (ERF) calculation, modular design, and anchor-ERF matching. However, this method faces challenges, especially in effectively matching ERF and anchor size for thin and long items (J. Li et al., 2021).

A backbone network is a pre-trained neural network architecture that serves as the core feature extractor in tasks like image classification, object detection, and segmentation. In object detection, the effectiveness of backbone networks is critical, as they are responsible for accurately identifying objects within an image. For instance, in defect inspection for SMD LED chips, S. H. Chen and Tsai (2021) replaced the Darknet-53 backbone of YOLOv3 with DenseNet-121. DenseNet exhibited superior feature learning capabilities compared to Darknet-53, particularly regarding feature propagation and alleviating the problem of gradient disappearance (S. H. Chen & Tsai, 2021). Another proposed network architecture for electronic component recognition incorporating changes in the backbone network was YOLOv3-MobileNet, which replaced the original Darknet-53 with MobileNet (R. Huang et al., 2019). The MobileNet architecture simplified the network layers by dividing the convolution layer into depthwise and pointwise convolutions, thereby enhancing efficiency.

A study unrelated to PCBs utilised YOLOv3 and the Super-Resolution Convolutional Neural Network (SRCNN) model to accurately detect the location and condition of electrical components, particularly insulators, in diverse scenarios (H. Chen et al., 2019). Figure 2.3 illustrates the steps of SRCNN with YOLOv3. Super-resolution models are effective pre-processing tools, significantly enhancing the feature extraction process. Another super-resolution model was Enhanced Deep Residual Networks for Single Image Super-Resolution (EDSR), specifically designed to obtain high-resolution component images to learn fine-grained details and efficiently perceive features (Makwana et al., 2023).

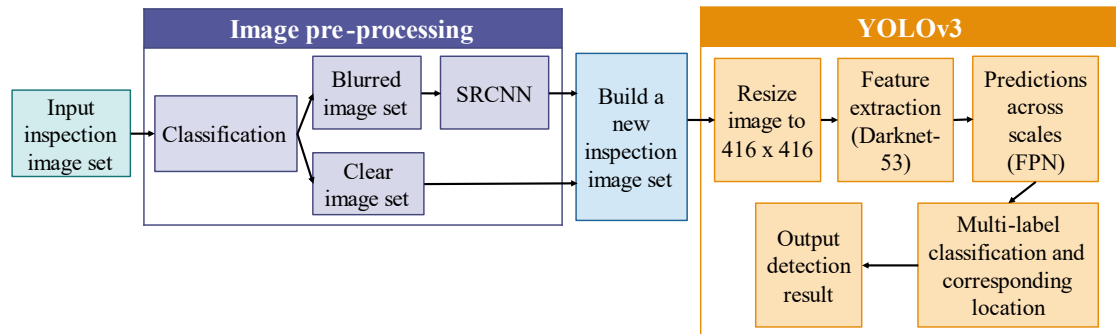


Figure 2.3 Overall Process of SRCNN with YOLOv3 (H. Chen et al., 2019).

The evolution of object detection algorithms has made YOLOv4 a preferred choice for PCB detection, surpassing its predecessor, YOLOv3. While YOLOv3 employed DarkNet53 as its backbone, YOLOv4 integrates CSPDarknet-53, which enhances feature extraction through residual blocks (Bochkovskiy et al., 2020). The incorporation of Cross-Stage Partial (CSP) connections within CSPDarknet-53 improves feature representation while reducing computational complexity (Xin et al., 2021). These optimisations make YOLOv4 particularly effective for tasks such as detecting solder joint defects in PCB assembly lines, as demonstrated by Caliskan and Gurkan (2021). Additionally, YOLOv4 was enhanced and applied in methods for detecting PCB electronic component defects, focusing on small object detection,

making it ideal for identifying small electrical components (Xin et al., 2021). An enhanced version, YOLOv4-MNS, improves efficiency by replacing the original backbone with the lightweight MobileNetv3 and refining the activation function within the prediction network, specifically for PCB surface defect detection (Liao et al., 2021).

Incorporating an attention mechanism into object detection allows neural networks to prioritise and focus on relevant information (objects) rather than irrelevant background details. This concept was integrated with the YOLOv4-tiny algorithm and a Multiscale Attention Module (MAM) to enhance its accuracy as an electronic component detector (Guo et al., 2021). However, this method focuses on inspecting common electronic components rather than specifically on PCB detection. Transformers and attention mechanisms are closely related concepts. Transformer is a specific type of neural network architecture that utilises self-attention mechanisms to capture long-range dependencies and extract intrinsic features (Han et al., 2022). A variant of the YOLOv5 model combined with a transformer was introduced as an end-to-end deep-learning framework to detect and classify PCB manufacturing defect types (Bhattacharya & Cloutier, 2022).

The loss function is responsible for measuring the difference between the predicted and ground truth values and assessing the proximity or dissimilarity of these values. In object detection, the loss function typically comprises three components: classification loss, confidence loss, and bounding box regression loss. The bounding box regression loss aims to refine the localisation accuracy of the detected objects. For instance, the Generalized Intersection over Union (GIoU), as described by Fan et al. (2021), was employed as the bounding-box regression loss to address the issue of non-optimal solutions caused by disjoint predictions and ground truths in solder joint defects

and component detection. Another regression loss function, Gaussian Intersection over Union (GsIoU), which used a Gaussian function to merge boxes across different anchors, was integrated into YOLOv4 for detecting for detecting electronic components on PCBs (X. Liu et al., 2022).

$$GsIoU = \frac{1}{\sqrt{2\pi\beta}} \exp\left(-\frac{(1 - IoU)^2}{2\beta}\right) \quad (1)$$

where β represents the variance for each predicted box with an Intersection over Union (IoU) value that exceeds the specified threshold. Besides, Reza et al. (2020) introduced a novel loss function technique called "Loss Boosting (LB)" incorporated into the YOLOv2 regression model to enhance the detection performance specifically for small integrated circuits. The loss function used the formula below:

$$\begin{aligned} loss = & e^+ \sum_{i=1}^n (loss_{obj} + loss_{coord} + loss_{class}) \\ & + e^- \sum_{i=1}^{m-n} (loss_{obj} + loss_{coord} + loss_{class}) \end{aligned} \quad (2)$$

The symbols e^+/e^- represent additional coefficients either greater than or less than 1, m is the total number of objects in the image, while n represents the number of predicted boxes whose IoU is less than the threshold, $loss_{obj}$, $loss_{coord}$, and $loss_{class}$ represent the objectness loss, coordinates loss, and classification loss, respectively (Reza et al., 2020).

In a separate study, the classification loss employed in the YOLOv4-tiny model is based on Binary Cross-Entropy (BCE) (Guo et al., 2021). The BCE formula is presented in equation (3), while the classification loss is detailed in equation (4).

$$BCE(Px) = -(1 - Px)^y * \log Px \quad (3)$$

$$\begin{aligned}
loss_{class} = & - \sum_{i=0}^{S*S} 1_{ij}^{obj} \sum_{t \in classes} [(\hat{P}_i(t)^\gamma P_i(t) \log \hat{P}_i(t) + (1 \\
& - \hat{P}_i(t)^\gamma (1 - \hat{P}_i(t) \log(1 - \hat{P}_i(t)))]
\end{aligned} \tag{4}$$

Px denotes the probability for class x , $S*S$ represents the grid points, 1_{ij}^{obj} indicates if a target exists in the grid, and \hat{P} is the predicted value. The parameter γ is set to 1.5. The final loss function was composed by summing the classification loss function, the Complete Intersection over Union (CIoU) loss, and the confidence loss (Guo et al., 2021).

2.3.1(b) One-Stage Detector: SSD

SSD is an object detection framework that combines the regression concept from YOLO and the anchoring mechanism from Faster R-CNN. A study to identify the electronic components proposed an enhanced SSD version by incorporating a feature fusion strategy and introducing visual reasoning techniques (X. Sun et al., 2020). By replacing Visual Geometry Group (VGG) with ResNet-50, the proposed SSD model benefited from improved handling of degradation issues. Moreover, it facilitated two-way information transmission within the network (X. Sun et al., 2020).

2.3.1(c) One-stage Detector: RetinaNet

Mahalingam et al. (2019) evaluated various PCB analysis methods, including YOLOv3, RetinaNet-50, and Faster R-CNN. RetinaNet, which employed focal loss for classification, featured a unified network with two subnets—one for classification and another for box regression tasks (Mahalingam et al., 2019). Although RetinaNet exhibited strong performance, it faced challenges distinguishing components resembling ICs, highlighting the necessity for improved differentiation in PCB analysis tasks. A modified RetinaNet, PCBDet, excelled in detecting PCB components (B. Li et al., 2023). It employed a self-attention design influenced by RetinaNet's bounding box

prediction structure and integrated AttendNeXt, a double-condensing attention condenser backbone architecture, to bolster its feature extraction abilities.

2.3.1(d) Two-Stage Detector

Different variants of two-stage object detection networks are available and have been compared based on their speed and accuracy in inspecting electronic components. Mallaiyan Sathiaselalan et al. (2021) developed the Electronic Component Localization and Detection Network (ECLAD-Net) tailored for PCB assembly counterfeit and defect detection. ECLAD-Net involved two stages: the Region Proposal Network (RPN), responsible for suggesting regions, and the Similarity Prediction Network (SPN), functioning as the classifier, distinguishing resistors and capacitors (Mallaiyan Sathiaselalan et al., 2021). In another approach, Kuo et al. (2019) proposed a three-stage object detection pipeline that involved identifying potential components using bounding boxes by the RPN while the SPN addressed imbalanced distribution among different PCB component types (Kuo et al., 2019).

Several methodologies based on Faster R-CNN have been developed for PCB inspection. A comparative study by Chen Yang (2020) explored various electronic component detection and localisation methods. Yang discovered that k-means coupled with CNN classification outperformed Faster R-CNN (Yang, 2020). Additionally, a specific variant of Faster R-CNN Inception-v2 demonstrated promising performance in localising PCB components, particularly in identifying absent resistors (Cheong et al., 2019). Furthermore, in the field of PCB defect detection, a Tiny Defect Detection Network (TDD-Net) was introduced to identify minor defects like missing holes and mouse bites. This TDD-Net followed the Faster R-CNN paradigm, adopted FPN to form a multi-scale feature fusion pyramid, and utilised the ResNet-101 as the backbone. It achieved 98.90% mAP, showcasing its exceptional ability to identify these defects in

PCBs (Ding et al., 2019). Shen et al. (2020) established LD-PCB, a lightweight object detection model for defect detection on PCBs, which enhanced small object detection accuracy by replacing the ROI pooling layer with Context-aware ROI (CAROI) pooling within the Faster R-CNN framework.

Further innovations in PCB defect detection include the development of Efficient Faster R-CNN, introduced by Fan et al. (2021). This algorithm improves the accuracy of detecting solder joint defects and components on PCBs by replacing the original VGG-16 backbone with EfficientNet-B7. In another PCB defect detection study, the EfficientNetv2-M, was integrated into Faster R-CNN with an optimised FPN, leading to an increase in mAP at IoU=0.50 from 99.58% to 99.66% (Bochkovskiy et al., 2020). The versatility of EfficientNet has also made it a valuable tool in various PCB-related applications. For instance, EfficientNet-B3 was employed to develop a robust classification system for PCB recycling (Soomro et al., 2022).

Beyond defect detection, PCB assembly examination serves various purposes, including identifying recyclable components and generating a crucial bill of materials (BoM) for manufacturers. Mehta et al. (2020) presented an automatic bill of materials (AutoBoM) for PCB component detection. The paper encompassed traditional image analysis employing colour thresholding and a deep learning-based method utilising a Mask Region-based Convolutional Neural Network (Mask R-CNN). Mask R-CNN, an extension of the Faster R-CNN architecture, integrated a mask prediction branch to produce pixel-level segmentation masks (K. He et al., 2017). The experiment identified critical factors influencing accuracy, including board colour, texture/material, lighting conditions, and component density (Mehta et al., 2020). Figure 2.4 shows the disparity in detection processes between conventional and deep learning-based methods.