THE DESIGN OF HIGH-SPEED CMOS PIPELINED ADC AND HYBRID DAC FOR WIRELESS COMMUNICATION

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THE DESIGN OF HIGH-SPEED CMOS PIPELINED ADC AND HYBRID DAC FOR WIRELESS COMMUNICATION

by

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You know who you are!

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LIST OF ABBREVIATIONS

1G	First Generation
2G	Second Generation
3G	Third Generation
4G	Fourth Generation
5G	Fifth Generation
CDAC	Capacitive DAC
CMOS	Complementary Metal-Oxide-Semiconductor
DEC	Digital error correction
DNL	Differential Non-Linearity
ENOB	Effective-Number-of-Bit
FOM	Figure-of-Merit
GSM	Global System for Mobile
GS/s	Giga Sample per second
IC	Integrated Circuit
INL	Integral Non-Linearity
IoT	Internet-of-Things
LSB	Least Significant Bit
LTE	Long Term Evolution
MDAC	Multiplying Digital-to-Analog Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
MSB	Most Significant Bit
MS/s	Mega Sample per second
NMOS	N-typed Metal-Oxide Semiconductor
PMOS	P-typed Metal-Oxide Semiconductor
PVT	Process, voltage and temperature
S/H	Sample and Hold
SAR	Successive-Approximation-Register
SDR	Software-defined Radio
SFDR	Spurious-free Dynamic Range
SNDR	Signal-to-Noise Distortion Ratio

SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
Wi-Fi	Wireless Fidelity

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REKA BENTUK ADC SALURAN PAIP DAN DAC HIBRID CMOS BERKELAJUAN TINGGI UNTUK KOMUNIKASI TANPA WAYAR

ABSTRAK

Peningkatan kadar *data* yang diperlukan oleh sistem komunikasi tanpa wayar terkini meningkatkan permintaan terhadap *ADC* dan *DAC* berkelajuan tinggi. Oleh itu, penyelidikan ini memperkenalkan *ADC* saluran paip dan *DAC* hibrid *16-bit 400 MS/s* yang baharu, direka menggunakan proses *CMOS 65 nm* dan voltan *1 V*. Dalam *ADC* saluran paip, resolusi dan kadar pensampelan dihadkan oleh gandaan *DC* gelung terbuka dan frekuensi unit-gandaan penguat kendalian sebagai komponen teras. Walau bagaimanapun, penguat kendalian berprestasi tinggi disertai penggunaan kuasa yang tinggi. Justeru, *ADC* yang dicadangkan mencirikan penguat kendalian dua kali gandaan mencapai frekuensi unit-gandaan melebihi *5 GHz* dan gandaan *DC* gelung terbuka *100 dB*. *ADC* ini menggunakan kawasan aktif *0.83 mm²* dan kuasa *50 mW*. *ADC* ini mencapai *SNDR 73.0 dB* dan *Schreier FoM 168 dB*. Sistem yang berkelajuan tinggi juga memperkenalkan *glitch* dalam *DAC*, yang ketara menjejaskan lineariti dan prestasi keseluruhan *DAC*. Teknik pengurangan *glitch* telah meningkatkan prestasi *DAC*, tetapi dengan kuasa yang tinggi. Oleh itu, penyelidikan ini mencadangkan *DAC* hibrid yang baharu, menggunakan mekanisme penapisan digital yang direka untuk menghapuskan *glitch*. *DAC* ini menggabungkan seni bina-seni bina arus kemudi *6-MSB* dan rintangan berwajaran binari *10-LSB*, dengan kuasa *8.36 mW* dan kawasan aktif *0.06 mm²*. *DAC* ini mencapai *SFDR 74.68 dB*, dengan *FOM 23.57×10¹² VHz/W*. *ADC* saluran paip dan *DAC* hibrid yang baharu ini menyediakan penyelesaian yang sangat cekap, pantas, dan tepat untuk sistem komunikasi tanpa wayar moden yang memerlukan penukaran *data* berkelajuan tinggi dan beresolusi tinggi.

THE DESIGN OF HIGH-SPEED CMOS PIPELINED ADC AND HYBRID DAC FOR WIRELESS COMMUNICATION

ABSTRACT

The increasing data rates required by cutting-edge wireless communication systems have intensified the demand for high-speed ADCs and DACs. Therefore, this research presents an innovative 16-bit 400 MS/s pipelined ADC and hybrid DAC, designed using the 65 nm CMOS process and a supply voltage of 1 V. In pipelined ADCs, resolution and sampling rate are primarily constrained by open-loop DC gain and unity-gain frequency of operational amplifier (op-amp) as their core component. However, achieving high-performance op-amp comes at the cost of increased power consumption. Therefore, the proposed ADC features an inventive dual gain boosting op-amp that surpasses a unity-gain frequency of 5 GHz and an open-loop DC gain of 100 dB. The ADC occupies an active area of 0.83 mm^2 and consumes 50 mW of power. The ADC exhibits an SNDR of 73.0 dB, resulting in a Schreier FoM of 168 dB. The high-speed systems also introduces glitches in DACs, which severely impair the linearity and overall DAC performance. Glitch-reduction techniques enhance the performance of DACs, with the trade-off in power consumption. Hence, this research proposes a novel hybrid DAC, incorporates a digital filtering mechanism designed to eliminate glitches. The DAC combines a 6-MSB current-steering and a 10-LSB binary-weighted resistor architectures, resulting a total power consumption of 8.36 mW within an active area of 0.06 mm^2. The DAC achieves an SFDR of 74.68 dB, with a FOM of 23.57×10^{12} VHz/W. The innovative pipelined ADC and hybrid DAC provide a highly efficient, fast, and accurate solution for modern wireless communication systems that require high-speed and high-resolution data conversion.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Wireless communication has experienced substantial progressions throughout its history, encompassing multiple generations. Every succeeding generation signifies a significant advancement in technology, introducing novel functionalities and enhancements to data rates, capacity and dependability. An overview of the evolution of wireless communication is shown in Figure 1.1.

Each advanced generation has led to higher speed and more reliable networks. During the 1980s, the First-Generation (1G) of technology facilitated communication using a mobile phone. The Second-Generation (2G), the subsequent iteration, facilitated enhanced and protected voice communication, while also introducing the concept of text messaging. The advent of the Third Generation (3G) and the subsequent introduction of the Fourth Generation (4G) have ushered in a new era of smartphones and faster data transmission rates, as stated by [1]. The Fifth-Generation (5G) is the next-generation mobile network that integrates many wireless technologies like Global System for Mobile Communications (GSM), Wireless Fidelity (Wi-Fi), and Long-Term Evolution (LTE). It enables connectivity with a wide range of entities, including machines, objects and devices [2]. Simultaneously, the 5G network facilitates expedited data download and transfer [3]–[5], smoother dissemination of online content and enhanced audio and video call quality [6] and more reliable mobile connections [7]–[9].

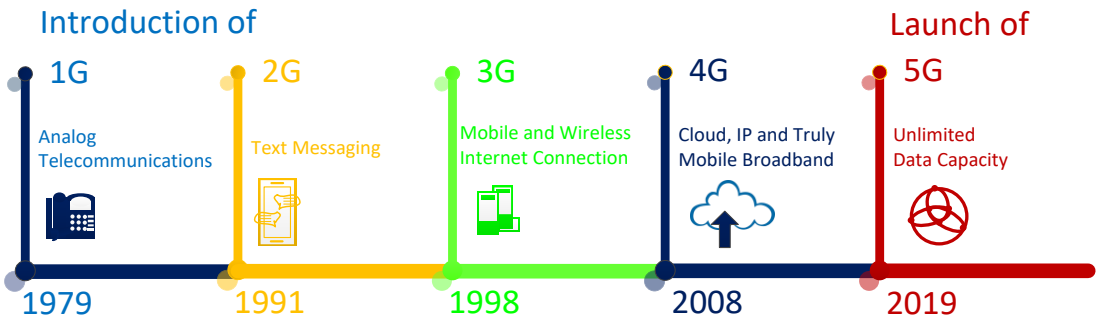


Figure 1.1: The evolution of 5G [10].

Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) play an essential role in wireless communication systems by making possible the conversion of digital to analog signals and vice versa [11]. The significance of these conversions lies in the fact that digital devices, including microcontrollers and computers, process data exclusively in digital format, whereas analog signals are frequently employed during the transmission and reception of signals over wireless media.

Analog signals such as voice, video or sensor data produced by microphones, cameras or sensors must be converted into digital signals [12] before transmission and processing in wireless communication. ADCs play a crucial part in applications such as voice communication over cellular networks, video streaming and wireless systems that rely on sensors. The ADC periodically captures the continuous analog signal, converts each sample into a digital format and generates a sequence of binary values that correspond to the amplitudes of the original analog signal at each sampling point. In a wireless microphone system, the microphone records analog sound waves. The ADC translates these analog impulses into digital signals that are capable of being processed, encoded and transmitted wirelessly.

The persistent and rapid growth in wireless modern communication develops the need of devices that operate at an expedient rate and consume minimal power [13], [14]. Pipelined ADCs in [15]–[17] offer a more favourable balance between speed and resolution compared to the other ADC architectures such as Successive-Approximation-Register (SAR), time-interleaved and flash. Thus, the use of pipelined ADCs is recommended for ADCs with sampling rates ranging from hundreds of Mega-Samples per second (MS/s) to Giga-Samples per second (GS/s) [18]–[20].

Pipelined ADCs can achieve high resolution and high linearity in the entire Nyquist band [15]. When the sampling rate of pipelined ADC reaches hundreds MS/s, the settling time of operational amplifier (op-amp) is limited to less than 1 ns. It is challenging to obtain high sampling rate implementing a single-channel ADC in higher node Complementary Metal-Oxide-Semiconductor (CMOS) technology. In contrast, as CMOS technology is scaling down, the parasitic capacitance of metal-oxide-semiconductor field-effect transistor (MOSFET) has been greatly reduced. Thus, the unity-gain bandwidth will be higher as compared to that in higher node process.

In pipelined ADCs, op-amp utilizes most of the power [21], [22]. In order to prevent undesirable effects that may reduce the accuracy of the residue, it is necessary for the op-amp to have an adequate open-loop DC gain and unity-gain frequency to meet the accuracy requirements of the back-end stages. The shrinkage of CMOS technology has enhanced the unity-gain frequency. However, it has also resulted in a decrease in the inherent device gain due to the reduced supply voltage [23]–[25].

Researchers have conducted a number of studies to date in an effort to strike a balance between gain, which can be seen clearly through differential non-linearity (DNL) and power consumption of ADC. ADC operating at the sampling rate of 500 MS/s presented in [16] utilized Class C slew-rate boosting technique that provided

high dynamic current up to 12-bit with power consumption of 18.16 mW. Furthermore, a gain calibration scheme was utilized to improve the DNL from +1.58/-1.17 LSB to +0.41/-0.42 LSB, which translated to Schreier Figure-of-Merit (FoM) of 165.3 dB at Nyquist.

Besides, ADC described in [26] operated at the sampling rate of 1 GS/s has implemented 2-channel cascaded SAR architecture for 12-bit, which mitigated the need of intra-stage multiplying-DACs (MDACs) and consumed 230 mW. At Nyquist, the Schreier FoM is 149.4 dB with peak DNL of -0.7/+0.8 LSB. ADC reported by [27] employed two-stage op-amp with positive feedback to attain high open-loop DC gain for 14-bit resolution operating at the sampling rate of 1 GS/s. Nevertheless, a background calibration scheme was introduced to enhance the DNL from -1 LSB to -0.3/+0.3 LSB, thus led to huge power consumption, i.e. 1.2 W, which equals to Schreier FoM of 155.2 dB at Nyquist.

Apart from that, ADC described in [28] applied multi-channel time-interleaved to reduce the number of op-amps in 12-bit 400 MS/s operation. As a result, the power consumption of the ADC is low, i.e. 74 mW, which translated to 150.8 dB Schreier FoM at Nyquist. Nonetheless, timing skew existed between the channels was corrected by a digital calibration and has improved the DNL from 1.2 LSB to 0.56 LSB.

Another ADC reported in [17] utilized low-gain op-amp to guarantee reasonable power consumption, i.e. 105 mW for 12-bit resolution operating at the sampling rate of 800 MS/s. However, they have used digital calibration to solve offset error in the op-amp, which resulted satisfying DNL, i.e. -0.4/+0.3 LSB. The measured Schreier FoM at Nyquist is 154.4 dB. A study in [13], which developed the ADC by pipelined-SAR architecture also implemented low-gain op-amp and resulted low

power consumption, i.e. 10.71 mW, which gave 160.6 dB Schreier FoM for 12-bit 125 MS/s operation. By adding off-chip digital calibration to eliminate gain error, the DNL has improved to -0.55/+0.55 LSB.

Application of digital calibration in ADC has been conventional in lower node technology (40 nm and lower) recently to solve low device gain issue and maintain reasonable power consumption of ADC, i.e. lower than 100 mW. Nevertheless, design complexity and speed are the trade-offs [28], [29]. Therefore, ADC described in [15] employed a dual-supply op-amp, which are 1.2 V and 2.5 V to achieve high open-loop DC gain for 12-bit resolution at the sampling rate of 1 GS/s. As a result, the ADC provided excellent measured DNL, i.e. -0.5/+0.5 LSB and consumed 350 mW, which translated to Schreier FoM of 147.5 dB at Nyquist.

Furthermore, ADC reported by [30] which operated at the speed of 400 MS/s has used pipelined-SAR architecture to ensure low power consumption, i.e. 5.9 mW. Nevertheless, the resolution is limited to 7-bit and achieved low DNL, i.e. -0.124/+0.188 LSB. At Nyquist, the measured Schreier FoM is 146.1 dB.

The digital signals that have been processed must be converted back to analog form prior to transmission over the airways in wireless communication [31]. For instance, when digital data must be modulated into analog signals for transmission over Radio Frequency (RF) channels, DACs are indispensable. The DAC accepts binary integers as input, generates a continuous analog output and reconstructs the original analog signal based on the digital samples [32]. Illustratively, digital audio data is wirelessly transmitted within a wireless speaker system. A DAC is employed by the receiver to transform the digital audio signal back into an analog format. This analog signal is subsequently amplified and transmitted through the speaker.

Recently, battery-powered devices have been used extensively in various wireless communication applications, such as telecommunication [33], medical and healthcare devices, Internet-of-Things (IoT) [34] as well as transportation [35]. Power consumption is a significant parameter to enable these portable systems. This motivates researchers to provide a DAC, which acts as an important interface device [36], operating at low power supply voltage and low power consumption [37], [38].

Extensive research has been conducted over the years to reduce the power consumption of DAC. In the work by [39], the current-steering DAC implemented dynamic-element-matching (DEM) to provide better dynamic performance, i.e. spurious-free dynamic range (SFDR) of 68.3 dB at 100 MHz operating frequency. Nonetheless, this DAC consumed 18 mW power for a 12-bit resolution with integral non-linearity (INL) error between -0.7 to +1.3 LSB and has a small die area of 0.21 mm^2. Unlike the study in [40], binary-weighted DAC architecture has been developed for a 10-bit resolution with a die area of 0.8 mm^2. Operating at 400 MHz, the DAC consumed 20.7 mW power for data conversion. This DAC operated with DNL and INL within 2.6 LSB and 1.5 LSB, respectively.

Another study in [41] also employed current-steering architecture for higher operating frequency, i.e. 3.5 GHz and provided low DNL and INL, which are 0.03 LSB and 0.06 LSB, respectively. With medium resolution, i.e. 6-bit, this DAC consumed 10 mW at the mentioned frequency. Besides, [36] in their work who developed DAC based on current-steering architecture was also for 6-bit resolution with a die area of 0.46 mm^2. This DAC had both DNL and INL within -0.7 to +0.7 LSB and consumed 19.1 mW power at 1 GHz operating frequency.

To further reduce the power consumption whilst maintaining the good performance of DAC, a hybrid architecture, which has the most advantages and the

least disadvantages has been explored comprehensively. The study conducted in [42] describes a 10-bit hybrid DAC that utilized a time-mode architecture for the 5 most-significant-bit (MSB) and a current-steering architecture for the 5 least-significant-bit (LSB). The implementation of this hybrid design has resulted in a significant reduction in the die area, specifically to 0.00463 mm^2. However, an approach for compensating errors has been implemented in order to enhance the DNL and INL at a lower operating frequency of 3.4 MHz. Specifically, the DNL has been improved from 4.5 LSB to 0.5 LSB and the INL has been improved from -5 LSB to -0.6 LSB.

[43] in their work have developed a 12-bit hybrid DAC employing a 6 MSB-by-6 LSB design. The MSB component is based on a resistor-string while the LSB part uses current-steering. The DAC has a die area of 0.16 mm^2. At a frequency of 20 MHz, this DAC had a significant DNL of 6.38 LSB and INL of 7.55 LSB. However, it required only 1.74 mW of power. In addition, a 12-bit hybrid DAC as explained by [44] has the capability to operate at a frequency of 500 MHz. This is achieved by employing a combination of a 4 MSB by 8 LSB current-steering setup with a delta-sigma modulator. However, this DAC has a die area of 1.94 mm^2 and a power consumption of 430 mW.

1.2 Problem Statements

The advent of ADCs in wireless applications mark a significant technological leap, enhancing the performance and efficiency of modern communication systems [45]. Attaining high resolution and speed in ADCs while simultaneously minimizing DNL is a formidable challenge, particularly in advanced process technology nodes where reduced voltage supplies are employed. The difficulty intensifies as high-resolution ADCs, operating at sampling rates in the range of hundreds of MS/s, often

demand substantial power consumption and provide only moderate signal-to-noise-distortion ratio (SNDR), as reflected in the Schreier FoM. Several key parameters in evaluating the performance of ADCs are DNL and SNDR. Lower DNL enables higher SNDR value, which signify better performance, as they reflect a clearer and more accurate signal conversion.

However, achieving a high SNDR often comes at the cost of increased power consumption. Power consumption is a critical factor in the state-of-art wireless communication applications due to the need for devices to be energy-efficient while maintaining high performance [46]–[48]. Engineers strive to design ADCs that balance the trade-off between maintaining a high SNDR and minimizing power consumption, which is typically indicated by the highest Schreier FoM. This balance is essential for ensuring that 5G devices can deliver high-speed and reliable communication without draining battery life excessively [49].

In pipelined ADCs, the stage gain and residue amplifier are pivotal in determining the overall SNDR [28], [50]. Deviations from the ideal gain, due to component mismatches or variations, introduce gain errors that affect the residue signal, resulting in inaccurate digital output and a diminished SNDR [51]–[55]. Additionally, the residue amplifier must settle to its final value within a defined time frame. If the amplifier's bandwidth is insufficient, the residue signal will not settle accurately, leading to errors that manifest as distortion and noise, ultimately reducing the SNDR [14].

The power consumption of a pipelined ADC is elevated due to the use of a substantial quantity of intricate and power-intensive op-amp [56]. The op-amp plays a vital role in the advancement of pipelined ADCs as it is an essential component of the MDAC in the ADC [57]. The speed and accuracy of a closed-loop sample-and-hold

(S/H) circuit implemented are determined by the performance of the op-amp utilised, as stated in [58]. Hence, it is crucial to prioritise the necessity of op-amp's gain, bandwidth and settling time.

The primary considerations in the design of the pipelined ADC are attaining an adequate open-loop DC gain while meeting the necessary unity-gain frequency and settling precision. This is because criteria guarantee both high resolution (10-bit or above) and speed [59]. In recently published works on pipelined ADCs, op-amp can be categorised based on their bandwidth and gain. To meet the demand for a high open-loop DC gain, a pipelined ADC was developed by the op-amps using a gain-boosting technique and triple cascading [60].

Figure 1.2 illustrates the primary stage op-amp used in the design, while Figure 1.3 represents the N-section and P-section gain-enhanced op-amps. The primary stage and the gain amplifying op-amps have been implemented using a fully differential folding cascode configuration with current source loads. The primary stage drove a load capacitor of 16 pF, while the gain amplifying stage drove a load capacitor of 2 pF. The folded cascode design was preferred over the telescoping cascode design to meet the high input and output swing requirements [60].

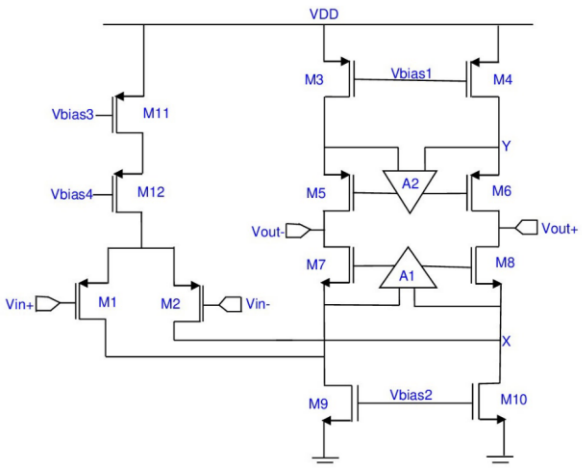
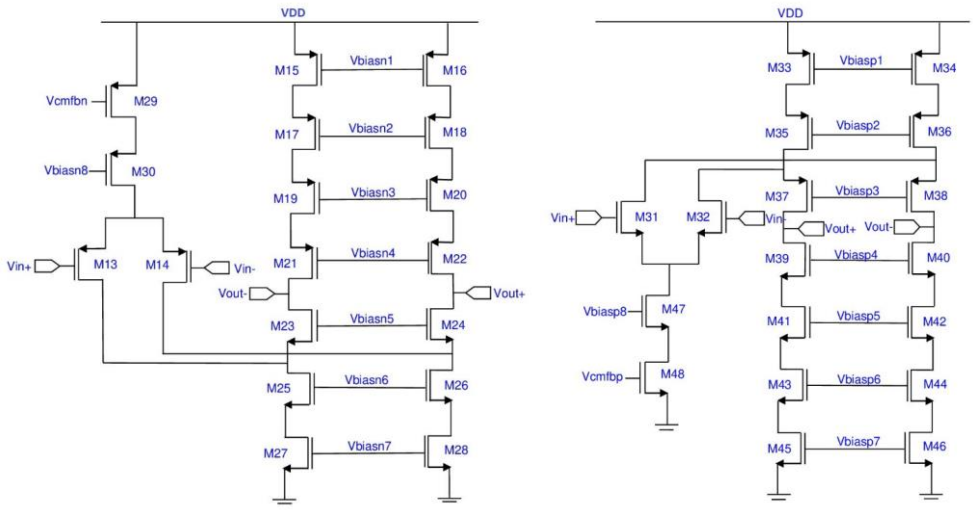


Figure 1.2: Primary op-amp [60].



(a) (b)

Figure 1.3: (a) N-section and (b) P-section gain-enhanced op-amp [60].

Depicted in Figure 1.4 is the residue op-amp reported in [15], comprising two stages that are powered by distinct power sources. For achieving fast speeds, thin-oxide devices are utilised. The initial phase comprises a straightforward low-voltage pre-amplifier that serves the dual purpose of diminishing power consumption and ensuring that the metal-oxide-semiconductor (MOS) devices function within a safe operating range. High voltage telescopic cascode amplifier constitutes the second stage. The V_{gs} and V_{ds} voltages of every MOSFET in the second stage amplifier should be meticulously designed to prevent the breakdown of any transistors to guarantee that they all function within a safe operating range. Comparing the first and second stages, which have significantly reduced gain and higher bandwidth, respectively, reveals that there is no need for a compensation technique between them. By applying high voltage to the second stage to broaden the output swings and utilising thin transistors to increase speed, the signal-to-noise ratio (SNR) can be enhanced. In the second stage op-amp, a positive feedback circuit is linked between the two cascode nodes. This op-

amp can attain gain of more than 80 dB with unity-gain frequency of higher than 5 GHz. The ADC using this op-amp resulted an active area of 1.6 mm^2.

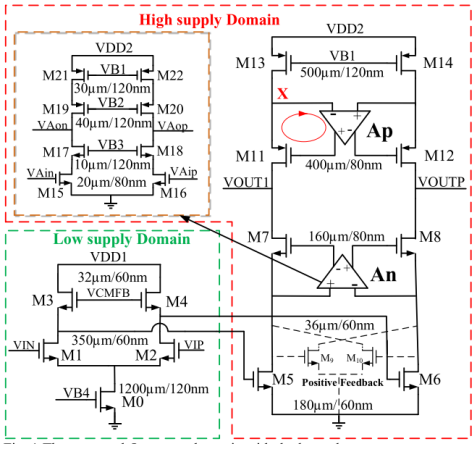


Figure 1.4: The op-amp schematic with dual supply [15].

Apart from that, a Gm-based amplifier that operates at low power levels and has a seamless transition from a comparator-like semi-digital operation to a continuous-time high-gain operation without the need for digital control or calibration was proposed by [61]. The authors presented a low-voltage Gm-based class-AB amplifier, as illustrated in Figure 1.5 that not only reduces common-mode bias current but also enhances a differential-mode signal. Additionally, a self-biased cascode output stage is suggested for low-voltage operation to attain a high level of amplification. The proposed amplifier is utilised in the design of a low-power 11-bit 2.5 MS/s pipelined ADC with an active area of 0.83 mm^2, without the need for calibration techniques or digital control. With this configuration, the op-amp achieved gain and unity-gain frequency of more than 80 dB and 38 MHz, respectively.

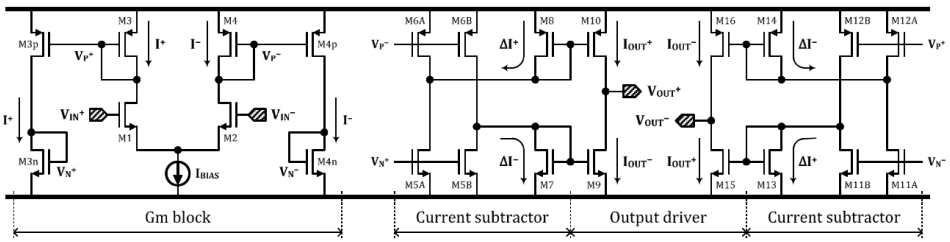


Figure 1.5: Basic structure of Gm-based amplifier [61].

Op-amps within the MDAC block of pipelined ADCs are a significant source of power dissipation due to the fact that their design must satisfy the MDAC stage's gain and bandwidth requirements [62]. Significant power savings are achieved in pipelined ADCs via the op-amp sharing method. Op-amp sharing reduces the quantity of op-amps by half by utilising an op-amp to share between two adjacent MDAC stages. The ADC as described in [62] employs three op-amps that are alternately utilised between stages 1 and 2, 3 and 4, and 5 and 6, respectively. The primary obstacle in op-amp sharing is to prevent the accumulation of residual charge in op-amp input capacitors caused by the absence of reset op-amp input terminals. Two distinct input pairs of N-channel metal-oxide semiconductor (NMOS) transistors are employed, with each pair operating as input transistors during alternating phases.

Figure 1.6 illustrates that V_{inp} and V_{inn} serve as the input pairs for phase 1, whereas V_{inp1} and V_{inn1} serve as the input pairs for phase 2. The unused input pairs in each phase are reset by being connected to a common mode voltage. One notable benefit of employing this method is the absence of any decrease in output swings. The fully differential op-amp is constructed utilising a telescopic topology, with a switched capacitor common mode feedback circuit. This op-amp has been employed for a 10-bit ADC. The gain boosting approach is employed to enhance and fulfil the gain demand. The op-amp provides a DC gain of 78 dB, which fits within the necessary range for achieving a 10-bit resolution.

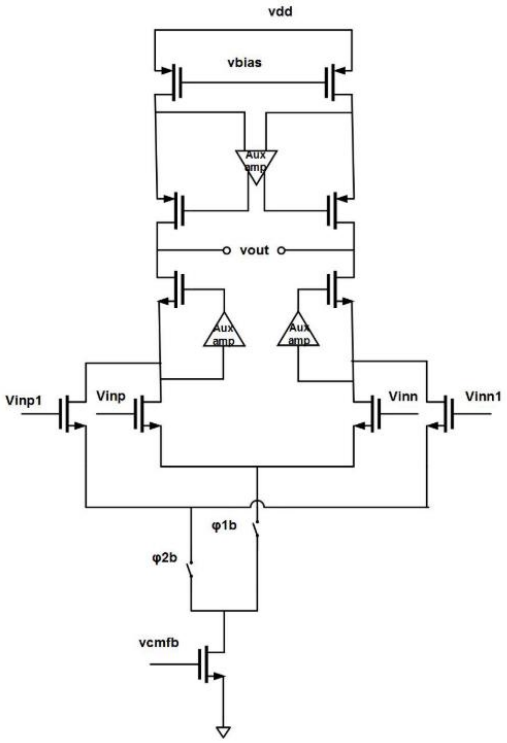


Figure 1.6: Telescopic op-amp with dual input pairs [62].

In addition, the study conducted in [57] introduced the Recycling Folded Cascode (RFC) op-amp. This op-amp design effectively redirects the tail current back into the input differential pair, resulting in a doubling of the input transconductance at its unity-gain frequency. In addition, this design provides moderate improvements in slew rate, DC gain and input referred noise. In order to accomplish the needed settling time while minimising current utilisation, it was necessary to incorporate gain boosting. The ADC employed the traditional folded-cascode op-amps to enhance gain. The supplementary op-amps, which are responsible for increasing the amplification, were also designed utilising the folded-cascode architecture for the first two stages, as shown in Figure 1.7. The auxiliary op-amps, AUX-N and AUX-P were used to enhance the output resistance of the cascodes in the main amplifier by employing a fully-differential configuration.

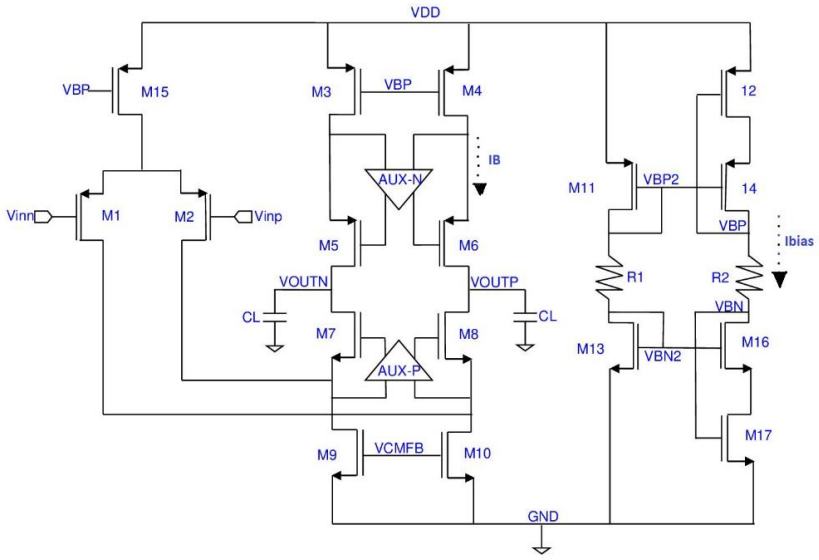


Figure 1.7: Schematic of the traditional gain-enhanced folded-cascode op-amp employed during the initial two stages [57].

In comparison to the conventional gain-boosting architecture, the final phases implemented with the novel gain-boosting structure, which consumed less power, are depicted in Figure 1.8. Gain-boosting was accomplished in the proposed architecture via four straightforward common-source amplifiers by increasing the resistance of individual cascode of the main amplifier. The input differential pair is divided into two equal halves, M1a, M1b, and M2a, M2b, in contrast to the conventional folded-cascode amplifier. Additionally, the tail current-source transistors M3 and M4 are divided in a 3:1 ratio, resulting in the formation of two current mirrors, M3a-M3b and M4a-M4b. This ADC can operate at a sampling rate of 70 MS/s while requiring approximately 41 mW.

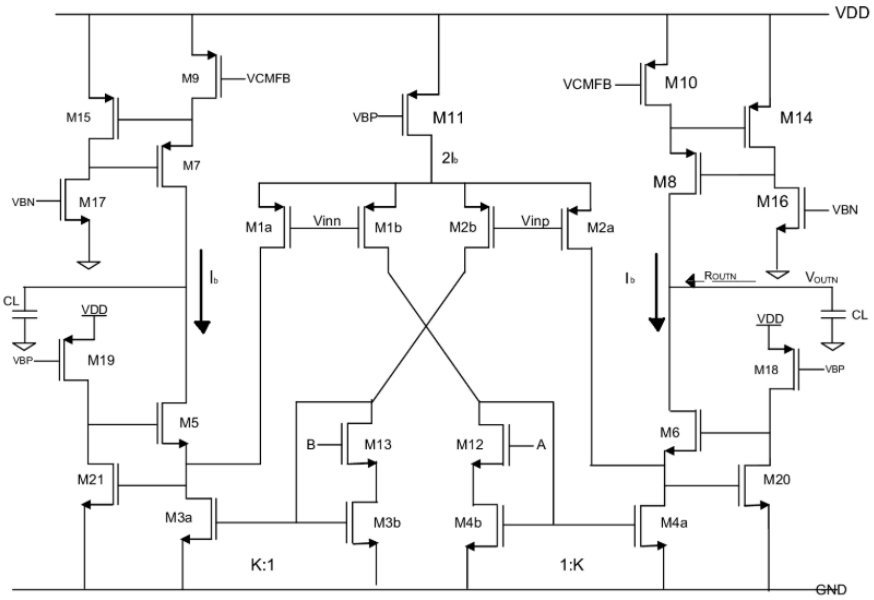


Figure 1.8: Schematic of the op-amp employed in the stages 3, 4, 5, and 6 [57].

As illustrated in Figure 1.9, the study in [63] implemented folded triple-cascode and common-source structures for the op-amp utilised in the first stage. Meanwhile, the amplifiers in the second to fourth stages utilise a conventional folded cascode configuration. Capacitive level shifters were inserted between the first and second stages to guarantee that the transistors in the first stage operate in the saturation area. The implementation was performed in the 0.18 µm CMOS process technology. According to the data gathered, the pipelined ADC, which incorporates this amplifier configuration, is capable of operating effectively at a sampling rate of 40 MS/s while consuming a total power of 23.4 mW with an active area of 0.64 mm^2.

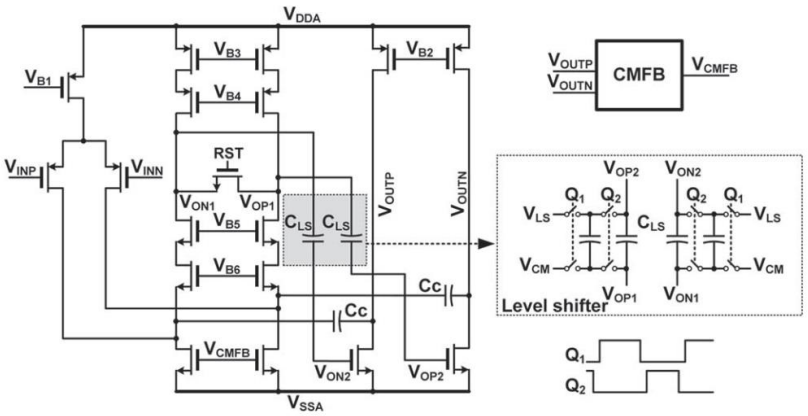


Figure 1.9: Op-amp of the first stage MDAC [63].

In summary, numerous improvements and developments have been implemented in the op-amp's block of pipelined ADC. The objective is to enhance the ADC's overall performance, with a particular focus on speed, linearity (DNL and SNDR) and power consumption. The modification is crucial to guarantee that the ADC operates at its peak efficiency while minimising costs.

Similarly, designing DACs with high bandwidth and speed, along with low power consumption and minimal DNL, presents another significant hurdle. One of the key factors in achieving low DNL is the elimination of glitches. However, the incorporation of glitch-reduction techniques in DACs tends to increase power consumption. This heightened power usage makes such DACs unsuitable for cutting-edge applications, which typically rely on battery-operated devices.

Among the various DAC architectures, current steering DACs are particularly well-suited to achieving low DNL, making them a popular choice for high-speed applications [64]–[66]. However, the high-speed operation inherent in these systems introduces challenges notably the occurrence of glitches, especially at MSBs [67]. These glitches can significantly degrade the linearity of the DAC, undermining the overall performance. To mitigate these effects, several glitch reduction mechanisms have been developed and employed in DAC designs. One such technique is the use of

return-to-zero (RZ) switching, where the output is briefly set to zero between successive digital code changes [68], [69]. This method helps to reset any residual charge that could cause glitches, particularly during high-speed transitions and resulted an active area of 1.49 mm^2 [69].

Another approach is the use of dummy switches, which are introduced to pre-charge nodes before the actual switching occurs [70]. This technique ensures that the switching action is smoother, reducing the potential for glitches during transitions. A newer technique, dynamic element matching (DEM), has gained attention for its ability to minimize glitches in high resolution DACs [71]. DEM works by dynamically rotating or scrambling the elements of the DAC to average out errors over time, reducing the impact of glitches on linearity and improving overall performance. This resulted the active area of 0.48 mm^2. Additionally, a diode-bridge current steering deglitches has been proposed to mitigate glitches; however, this approach is associated with the drawback of increased power consumption [72], [73] and huge active area, i.e. 1.2 mm^2 [73]. Finally, glitch cancellation circuits are sometimes added to directly counteract the effect of glitches, using complementary signals or differential architectures to cancel out the errors introduced by glitches [74]. Additionally, high-speed ADCs and DACs generally necessitate a large chip footprint, often surpassing 1 mm^2, to house the intricate circuitry required for optimal performance.

1.3 Objectives

The objectives of this research are:

1. To design a high resolution 16-bit high-speed 400 MS/s pipelined ADC in CMOS 65 nm process achieving DNL less than ±1 LSB and Schreier FoM more than 150 dB with V_{DD} of 1 V.

2. To design a high resolution 16-bit high-speed 400 MS/s hybrid DAC in CMOS 65 nm process achieving DNL less than ±1 LSB and FOM higher than 20×10^{12} VHz/W with V_{DD} of 1 V.
3. To design the active layout to be within 1 mm^2 each and fabricate the high-speed ADC and DAC in CMOS 65 nm process.

1.4 Thesis Outline

To accomplish the established objectives of the research, this thesis is outlined as follows:

Chapter 2 provides an extensive literature study of ADC and DAC, including their trends in wireless communication in terms of several key parameters, overviews, performance metrics and conventional architectures. Several significant requirements have been described as well to guarantee the design of the ADC and DAC a success.

Chapter 3 explains the detailed methodology of the designed ADC and DAC. A comprehensive analysis has been conducted through schematic and post-layout simulations to verify the functionality. Layout design has also been presented adequately to ensure the schematic performance is achieved.

Chapter 4 reports the measurement results of the designed ADC and DAC. The fabricated chips and measurement setup are also provided in this chapter. Lastly, the measurement results are compared to the other recently published works.

Chapter 5 gives a conclusion from this research and some recommendations for future studies of this research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Integrating digital signal processing devices with the external environment, ADC and DAC are crucial components in transceiver systems. Due to its diminutive size and reasonable power consumption, the development of integrated circuits (ICs) that integrate electronic systems onto a single chip, also known as a System-on-Chip (SoC), has recently become a subject of interest. As a result, SoC is regarded as an excellent component for wireless communication applications, irrespective of the technical obstacles that may arise.

Presently, there is considerable attention being paid to wireless communication applications, including but not limited to cellular networks, mobile communication and the IoT. These applications facilitate video broadcasting, wireless internet access and integration with smart home systems, respectively. Smart health, smart home, smart transportation and smart cities are a few of the applications that have enhanced our daily lives [34], [75], [76]. The need for devices that are both fast and power-effective has escalated due to the immeasurable demands of industry.

A key application driving the need for high-speed ADCs and DACs is the state-of-the-art wireless communication applications, particularly in sub-6 GHz bands, where the processing of high data rates is essential [77]. One of the fundamental performance metrics for both ADCs and DACs in these contexts is the SFDR, which measures the ratio of the desired signal strength to the strongest spurious signal or distortion component present in the output spectrum [78]. High SFDR is essential in the systems to minimize spurious emissions, reduce interference with adjacent channels, and optimize spectrum utilization [79]. The high utilization density of the sub-6 GHz bands

requires precise control to maintain communication integrity and reliability [80]. By optimizing SFDR, cleaner signal transmission is facilitated, enhancing overall system performance and increasing data throughput in 5G networks [81]. Achieving SFDR of more than 70 dB is commendable for the state-of-the-art wireless communication applications [82] and is contingent on minimizing DNL and INL [83], which translated to noise-figure lower than 0.3 dB [84], as depicted in Figure 2.1.

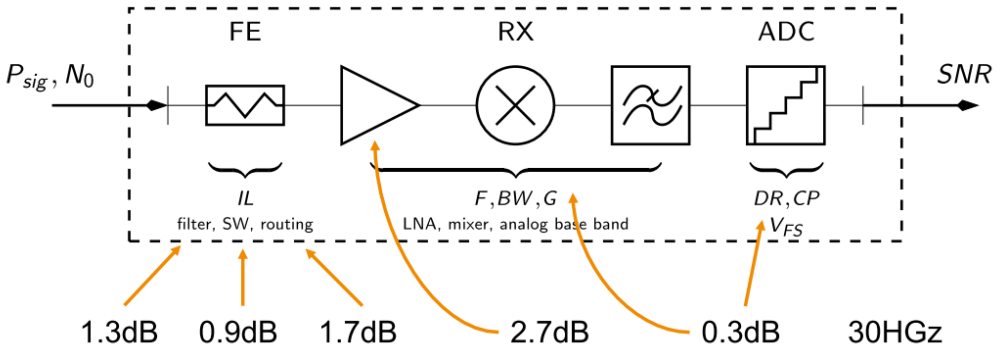


Figure 2.1: Simplified receiver model with an exemplary noise figure distribution [84].

High-resolution ADCs and DACs are critical in the architecture of advanced modern wireless communication systems to achieve the required SFDR. Their applications span across a wide range of fields, including radar and sonar systems, high resolution video and image display technologies, military and medical imaging, as well as high-performance controllers and sensors. Furthermore, these converters are integral to various detection and control systems, and their significance is poised to grow as they continue to play an indispensable role in the development of next-generation electronic systems [85].

Despite this, to achieve the required performance, high-speed ADCs [86] and DACs [87] must compromise on power consumption. As shown in Figure 2.2, the plot demonstrates a clear trend where the power consumption of both ADC and DAC increases as the sampling rate increases. The approximation lines provide a good fit for

the observed data, indicating that power consumption scales predictably with sampling rate, especially at higher sampling frequencies. At the sampling rate of hundreds MS/s, the power consumption of each ADC and DAC is more than 20 dBm, which translated to higher than 100 mW [88].

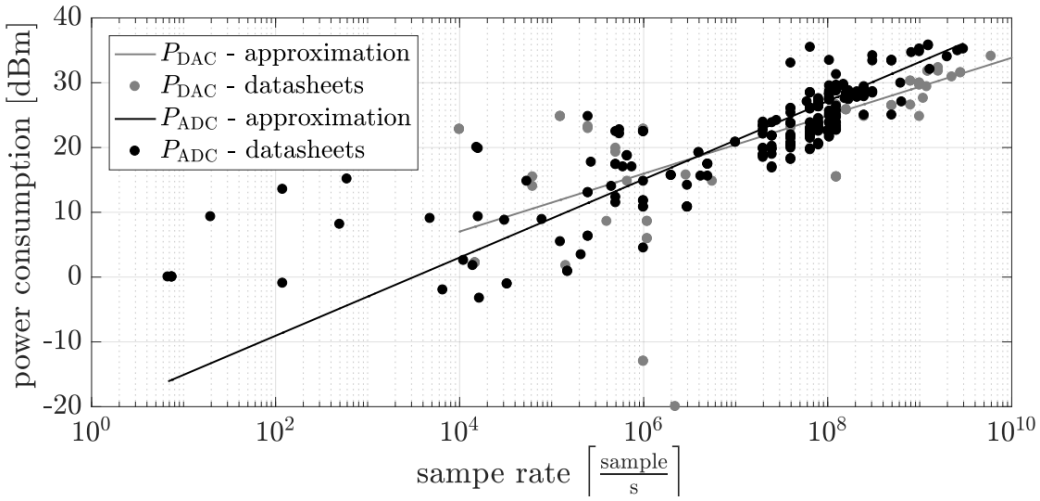


Figure 2.2: The powers consumed by the ADC and DAC based on datasheets of Analog Devices chips [88].

The following equations (2.1) and (2.2) are grounded on the undersampled signal criterion within a Nyquist zone, which was proposed in [89] and is depicted in Figure 2.3.

$$f_s \geq 2\Delta f \tag{2.1}$$

$$f_s = \frac{4f_c}{2NZ-1} \qquad ; NZ = 1, 2, 3, \ldots \tag{2.2}$$

where

f_s is sampling frequency

Δf is bandwidth of its signal

f_c is carrier frequency

NZ is the Nyquist zone in which the carrier and its signal fall

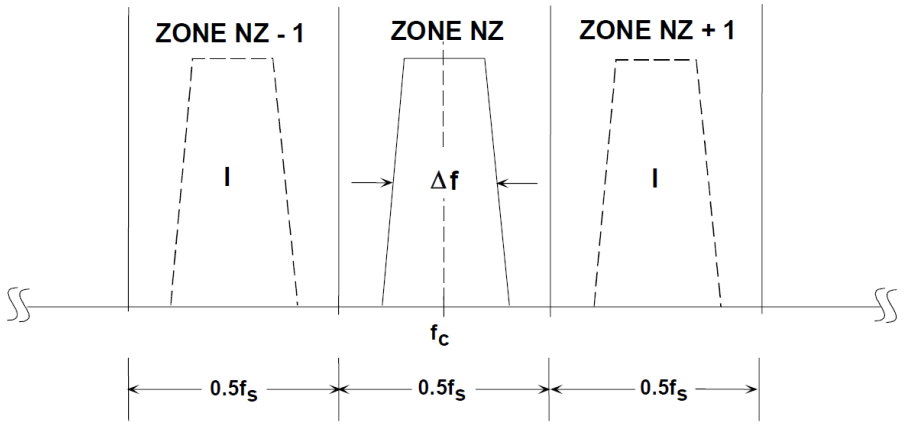


Figure 2.3: Centering an undersampled signal within a Nyquist zone [89].

In the context of this research, the value of f_c is considered to be 4.2 GHz (n77) encapsulating the 5G New Radio frequency band, as indicated in Table 2.1.

Table 2.1: Time Division Duplex (TDD) Frequency Bands [90].

Band	Duplexing Mode	Uplink/Downlink (MHz)	Total Bandwidth (MHz)
n34	TDD	2010 – 2025	15
n38	TDD	2570 – 2620	50
n39	TDD	1880 – 1920	40
n40	TDD	2300 – 2400	100
n41	TDD	2496 – 2690	194
n48	TDD	3550 – 3700	150
n50	TDD	1432 – 1517	85
n51	TDD	1427 – 1432	5
n77	TDD	3300 – 4200	900
n78	TDD	3300 – 3800	500
n79	TDD	4400 – 5000	600
n90	TDD	2496 – 2690	194
n96	TDD	5925 – 7125	1200
n101	TDD	1900 – 1910	10
n102	TDD	5925 – 6425	500
n104	TDD	6425 – 7125	700

Based on this, the calculation of bandwidth, Δf is derived as follows:

$$f_s = \frac{4f_c}{2NZ-1}$$

$$f_s = \frac{4(4.2\ G)}{2(22)-1} = 390\ MS/s$$

$$f_s \geq 2\Delta f$$

$$\frac{f_s}{2} \geq \Delta f$$

$$\frac{390\ M}{2} \geq \Delta f$$

$$195\ MHz \geq \Delta f$$

2.2 ADC Overview

ADCs serve an essential role in the process of acquiring data and converting it from real-world signals to digital codes [91]–[93]. An ADC is used to convert a continuously changing analog signal, characterized by its amplitude and time, into discrete digital signals. Figure 2.4 displays a block diagram of an ADC, which comprises of three foundational components - sampler, quantizer and coder. The sample circuit converts input signals into discrete time sampled signals, with the sampling clock controlling the process. Hold circuits function as circuit elements that preserve the sampled value without alteration during the transformation process.

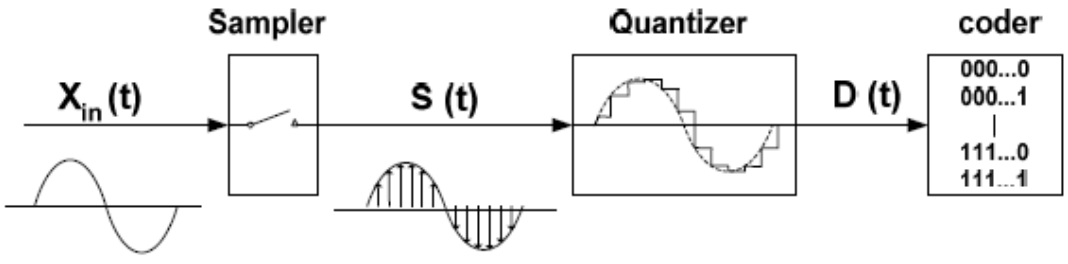


Figure 2.4: ADC block diagram [94].

A sampler translates an analog signal into a discrete representation in the time domain. The discrete-time continuous amplitude signal is converted into a discrete level by a quantizer, which transforms the signal into one of several quantization levels by

approximation. Uniform quantization minimizes quantization error for signals that are statistically evenly distributed, whereas non-uniform quantization is more suitable for signals, such as audio that have unevenly distributed amplitudes within the input range. Each quantization level, whether uniform or non-uniform, is allocated a distinct digital code. The process of analog-to-digital conversion is accomplished by assigning a sequence of digital codes to represent the discrete-time and discrete-amplitude analog signal [94].

ADC can be categorized into high-speed ADCs and high-accuracy ADCs based on their performance [95]. In addition, ADCs are classified as sub-sampling ADCs, oversampling ADCs and Nyquist ADCs, according to the correlation between sampling rate and signal frequency.

- **Sub-sampling ADCs**: Given that the input signal only fills a narrow range inside the band pass frequency, it is feasible to reduce the sampling frequency below the maximum frequency of the signal [96]. However, it is crucial to ensure that the sampled spectrum does not overlap.
- **Oversampling ADCs**: The sampling frequency exceeds the Nyquist frequency. The subsequent section of the digital filter circuit serves the purpose of eliminating extraneous interference beyond the signal's designated frequency range. The implementation of an oversampling technique can effectively decrease the level of quantization noise, hence enabling the attainment of a higher degree of precision [97].
- **Nyquist ADCs**: In order to achieve accurate restoration of the initial value, the ADC must comply with the sampling theorem, which dictates that the sampling frequency should be at least twice the maximum frequency of the input signal [98]. The anti-aliasing filter is unable to provide a perfect low-pass characteristic