KSCP Examination
2024/2025 Academic Session

September 2025

EBB525 – Electronic Materials and Devices

Duration : 2 hours

Please check that this examination paper consists of SIX (6) pages of printed material before you begin the examination.

Instructions: Answer **FOUR (4)** questions. Answer **TWO (2)** questions from PART A and **TWO (2)** questions from PART B. All questions carry the same marks.

The answers to all questions must start on a new page.

All questions must be answered in English.

Should any candidate be caught cheating or in possession of materials not authorised to be brought into the Examination Hall during the examination, appropriate disciplinary action will be taken against the candidate concerned. In the event a candidate is found guilty of cheating, he/she can be expelled from the University.

PART A

(1). A silicon wafer is doped with boron (acceptor) and phosphorus (donor). Answer the following questions:

(a). Explain carrier generation when such dopant atoms are added to silicon, use energy band diagrams in your answer. Differentiate the types of semiconductors

(5 marks)

(b). What is drift current in semiconductors? Explain how drift conductivity differs between intrinsic (undoped) and extrinsic (doped) silicon, and describe the influence of temperature on their conductivities.

(5 marks)

(c). A drift current density of J_{drift} = 100 A/cm^2 is required in a device using n-type silicon when an electric field of E = 15 V/cm is applied. Determine the required donor doping concentration to achieve this specification. Assume complete ionization and mobility of electron in this silicon is 1000 cm^2/Vs (n_i= 1.5 x 10^{10} cm^{-3}) at 300 K.

(10 marks)

(d). State the total current density equation for electrons and holes in a semiconductor including both drift and diffusion components. Explain under what condition the diffusion component dominates over drift.

(5 marks)

(2). (a). At 300 K, pure copper exhibits a conductivity of 5.96 x 10^7 S/m, while annealed copper has a slightly reduced value of 5.8 ×10^7 S/m. When alloyed with zinc to form brass, copper's conductivity decreases further to around 28% of IACS (International Annealed Copper Standard). Discuss these observations in terms of the fundamental laws governing electron scattering in metals

(10 marks)

(b). Indium tin oxide (ITO) is the most widely used transparent conductor in today's devices. Discuss the concept of transparent conductors by defining their dual characteristics of conductivity and transparency, citing examples such as ITO, FTO, and graphene.

(5 marks)

(c). Describe the key electronic properties of graphene, including its band structure and carrier transport behavior. Discuss, why graphene is being considered a promising alternative to ITO for applications in flexible and wearable electronics.

(5 marks)

(d). CuO is a p-type semiconductor, whereas the CuO_2 planes in cuprate superconductors are responsible for high-temperature superconductivity. Differentiate the mechanism of electron (or hole) conduction in CuO as a semiconductor and in the CuO_2 planes of cuprate superconductors when operated below the critical temperature.

(5 marks)

(3). A p–n junction is a fundamental element in many electronic devices. Consider a p–n junction under equilibrium, forward and reverse bias. Answer the following questions:

(a). Explain the sequence of steps that lead to the formation of the depletion region in a p–n junction.

(5 marks)

(b). By using Poison equation, describe the distribution of the electric field and built-in potential across the junction at equilibrium then compare to when the junction is forward biased.

(5 marks)

(c). Draw the energy band diagram of the p–n junction under reverse and forward bias. Compare the band diagram with junction in equilibrium and relate with diode formation.

(10 marks)

(d). If the junction has $N_D = 10^{17}$ cm and $N_A = 10^{16}$ cm^{-3} and if $n_i = 1.0 \times 10^{10}$ cm^{-3} calculate the built-in potential for the junction at equilibrium. Why is this value important?

(5 marks)

PART B

(4). (a). Sketch and discuss growth of silicon ingot using the Czochralski (Cz) method.

(9 marks)

(b). List **TWO (2)** vacancy-type crystal defects and **TWO (2)** interstitial-type crystal defects that can be found in a silicon ingot grown using the Czochralski (Cz) method.

(4 marks)

(c). Describe the distribution of these crystal defects in a silicon ingot grown by the Cz method at the axial (along the ingot length) and radial (across the ingot diameter).

(6 marks)

(d). Explain how the presence of vacancy- and interstitial-type crystal defects in silicon ingots can influence defect density, device performance, and ultimately the yield in IC fabrication.

(6 marks)

(5). (a). How do printed electronics differ from conventional semiconductor fabrication techniques?

(4 marks)

(b). (i). List **THREE (3)** common printing techniques used in printed electronics.

(3 marks)

(ii). Sketch and discuss the working principle of **ONE** printing technique that you proposed in (b)(i).

(8 marks)

(c). What are the current challenges and prospects for large-scale commercialization of printed electronics?

(10 marks)

(6). (a). With the aid of a sketch, describe the structure and explain the operation of an n-MOS transistor in enhancement mode.

(10 marks)

(b). Consider a p-type silicon substrate at T 30^{o}C doped to $N_a = 10^{17}$ cm^3. The oxide is silicon dioxide with a thickness of t_{ox} = 7 nm, and the gate is p^+-polysilicon. Calculate C_{ox}, C_{min}, and C_{FB} for this MOS capacitor.

(9 marks)

(c). **Figure 1** shows a cross-sectional view of a nanoribbon field-effect transistor (FET). Discuss **TWO (2)** advantages of the nanoribbon FET compared to conventional planar FETs.

(6 marks)

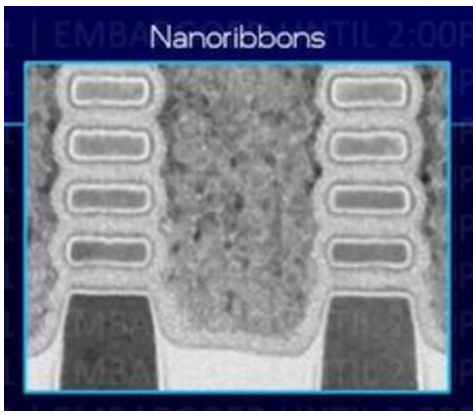

Figure 1 : Nanoribbon FET (source: Intel)

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