THERMAL INVESTIGATIONS OF FLIP CHIP MICROELECTRONIC PACKAGE WITH NON-UNIFORM POWER DISTRIBUTION

by

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June 2004

Thesis submitted in fulfillment of the requirements for the degree of Doctor of Philosophy

DEDICATED TO

MY BELOVED PARENTS

FOR THEIR YEARS OF SACRIFICE

ACKNOWLEDGMENTS

The research work is the result of several discussions I had with my research supervisors Prof. K.N. Seetharamu, Assoc. Prof. G. A. Quadir, and Assoc. Prof. Z. A. Zainal, School of Mechanical Engineering. I would like to express my deepest gratitude to them for their fine technical guidance and for the support rendered by them.

I would like to thank Dr. Chia-Pin Chiu and Dr. Abhay Watwe, Assembly Technology Development Department, Intel Corporation, as well as Assoc. Prof. Gary Solbrekken, Department of Mechanical Engineering, University of Missouri at Columbia for providing their guidance on the thermal modeling and validations.

I thank Dr. Martin Tay, Dr. Chandra Jayaram, and Dr. Ravi Mahajan, my managers in Intel, for their support and motivation in my thermal research. I am also thankful to Kin Gan, my department manager in Intel Malaysia, for taking keen interest in my research work.

I wish to express my sincere thanks to Mr. Ahmad Nordin Amir, Mr. Chee Kan Lee, and many other members of my thermal group in Intel for providing the data collection support in various stages of the research.

I am also grateful to Mr. K. Jeevan and Mr. Parthiban Arunasalam for sharing their knowledge on Genetic Algorithm.

I sincerely thank Mr. Kor Onn Lee for helping me to translate the abstract into Bahasa Malaysia.

I wish to thank Ms. Yin Peng Cheong and her family for their encouragement in the last seven years of my life.

Lastly, I take this opportunity to express my deep sense of gratitude to my family members for their patience, understanding, motivation, and support throughout the course of this work.

ABSTRAK

Arah aliran pempakejan sistem-sistem dan subsistem mikroelektronik adalah ke arah pengurangan saiz dan peningkatan prestasi, di mana kedua-duanya menyumbang kepada peningkatan kadar penjanaan haba. Bukti arah aliran tersebut boleh diperhatikan daripada peningkatan tahap integrasi pada aras pakej/alat mikroelektronik. Penempatan lebih banyak fungsi dalam pakej/alat mikroelektronik yang lebih kecil menyebabkan taburan kuasa yang tidak seragam dengan kepadatan haba yang ekstrem. Keadaan ini memberi mandat supaya pengurusan terma diberi keutamaan yang lebih tinggi dalam kitar rekabentuk demi mengekalkan prestasi dan keutuhan sistem.

Dalam kajian ini, metodologi untuk analisa terma dan pencirian pakej mikroelektronik *flip chip* dengan taburan kuasa tidak seragam telah dibina. Walaupun topik ini adalah penting untuk industri mikroelektronik, jarang terdapat sebarang karya dalam penerbitan ilmiah. Untuk analisa terma, kaedah analitikal, penggunaan regresi linear berbilang (MLR), superposisi suhu, dan teknik interpolasi Lagrangian telah diperkenalkan untuk menjangka taburan suhu bagi peralatan mikroelektronik berkuasa tidak seragam. Untuk pengoptimuman, algoritma genetik telah digunakan. Kaedah-kaedah tersebut adalah berguna untuk menyelidik interaksi terma antara punca-punca haba dalam cip silikon. Parameter-parameter terma kritikal seperti jarak perletakan punca haba, tahap pelesapan haba, dan magnitud pemindahan haba perolakan telah dikaji dalam lebih daripada 900 simulasi. Perletakan optimum punca-punca haba di dalam cip silikon telah ditentukan melalui algoritma genetik. Lokasi-lokasi perletakan tersebut telah ditentusahkan dengan analisa unsur terhingga.

Berdasarkan analisis yang telah dijalankan, tatacara rekabentuk yang komprehensif, serta panduan dan syarat-syarat untuk pakej ujian terma *flip chip* telah dirangka. Keperluan-keperluan dan proses-proses terperinci yang terlibat dalam

rekabentuk cip ujian telah dibincangkan. Kajian terma telah dijalankan untuk menyelidik keupayaan dan batasan rekabentuk pakej ujian terma dalam pembangunan panduan rekabentuk. Prosedur-prosedur pengesahan dan penentukuran bagi struktur rekabentuk yang diperihalkan untuk aplikasi-aplikasi pakej ujian terma yang berbeza telah dibincangkan secara mendalam.

Kajian ini juga mendirikan satu metodologi eksperimen yang sistematik untuk mengira dan menciri prestasi terma peralatan/pakej mikroelektronik *flip chip* dengan taburan kuasa tidak seragam. Prosedur terperinci untuk menghasilkan data yang tepat, boleh-ulang, dan yang boleh dihasilkan semula serta kaedah untuk menampal termokupel dalam eksperimen telah dijelaskan. Sistem pengukuran yang dibina khas untuk mengukur prestasi keadaan mantap suatu penyelesaian terma pakej telah dijelaskan dengan terperinci. Keunikan analisa keupayaan mengukur (MCA) pada metrologi terma, untuk mendemonstrasikan kestabilan dan keupayaan sistem dalam penyediaan metrologi dengan menggunakan artifak yang stabil telah diperkenalkan. Metodologi eksperimen tersebut telah didemonstrasikan selanjutnya dalam pencirian terma dan pengoptimuman pakej melalui proses perhimpunan dua rekabentuk pakej mikropemproses Pentium® *!!!* Xeon™ dengan taburan kuasa tidak seragam.

ABSTRACT

The trend in packaging microelectronic systems and subsystems has been to reduce size and increase performance, both of which contribute to increase heat generation. Evidence of this trend can be observed in higher level of integration in the device/package level. Placing more functions in a smaller microelectronic device/package has resulted in non-uniform power distribution with extreme heat density, mandating that thermal management be given higher priority in the design cycle in order to maintain the system performance and reliability.

In the present work, the methodology for thermal analysis and characterization of a flip chip microelectronic package with non-uniform power distribution has been developed. Though this topic is important to the industry, hardly any paper has been published in the literature. Analytical methods, employing multiple linear regression (MLR), temperature superposition, and Langrangian interpolation techniques, to predict the temperature distribution of non-uniform powered microelectronic devices for thermal analysis and genetic algorithms for optimization are introduced. These methods are useful in investigating the thermal interactions of heat sources within the silicon chip. Critical thermal parameters i.e. the heat source placement distance, level of heat dissipation, and magnitude of convection heat transfer are examined in more than 900 simulations. Optimal placement of heat sources within silicon chip is being carried out using genetic algorithms. The locations of this placement have been verified with the finite element analysis.

Based on the analyses, comprehensive design procedures, rules and guidelines for flip chip thermal test vehicles are developed. The requirements and the detailed processes involved in the test chip design are discussed. Thermal studies have been carried out to investigate the capability and limitations of thermal test vehicle designs

in support of developing design guidelines. The validation and calibration procedures of the described design structures for different thermal test vehicle applications have been discussed in detail.

The present work also establishes a systematic experimental methodology to quantify and characterize the thermal performance of flip chip microelectronic device/package with non-uniform power distribution. The detailed procedures for accurate, repeatable, and reproducible data and the method of attaching thermocouple used in thermal experiments are outlined. The custom built measurement system for gauging steady state performance of a given package thermal solution is described in detail. The unique measurement capability analysis (MCA) on the thermal metrology to demonstrate the stability and capability of the system and metrology set-up using stable artifacts is introduced. The experimental methodology has been further demonstrated in the package thermal characterization and optimization (through manufacturing process) of two Pentium® *!!!* Xeon™ microprocessor designs with non-uniform power distribution.

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NOMENCLATURES

f	Processor frequency, MHz or GHz
f	Number of fireball heater trace
g	Trace-to-trace pitch, μm
h	Coefficient of convection heat transfer, W/m^2.K
h_{eff}	Effective coefficient of convection heat transfer, W/m^2.K
j	Number of resistance temperature sensor/detector trace
k_{TE}	Thermal conductivity of TEC element, W/m.K
n	Number of heater legs
m	Number trace per heater leg
p	Dissipated power of a single cell/region within the silicon die, W
q	Heat flux leaving the boundary, W/m^2
w	Trace width, μm
w_{max}	Maximum allowable trace width, μm
$\bar{x}$	Mean or average value
x_c	X-coordinate at the center of Lagrangian Element
y_c	Y-coordinate at the center of Lagrangian Element
A	Heat generation or die surface area, cm^2
A_{base}	Heat sink base area, cm^2
A_{heater}	Heater area, cm^2
A_{RTD}	Resistance temperature sensor/detector area, mm^2
COP	Coefficient of performance
COP_{OPT}	Optimum COP
D	Distance from the center heat source to the corner heat source, m or mm

G	Area/length ratio of TEC element, m
G	Heat generation of the element per unit volume, W/m^3
I	Current requirement, A
I_{bump}	Current carrying capability of a bump, A/bump
I_{max}	Current limit for current control thermal measurement setup, A
I_{via}	Current carrying capability of a via, A/via
K	Thermal Conductivity, W/m.K
L_{heater}	Heater leg length, mm
L_{FB}	Fireball heater length, mm
L_{RTD}	Resistance temperature sensor/detector length, mm
MC	Metal coverage or ratio of metal and non metal in test die
N	Number of matrix cells in chip
N_c	Number of couples
N_{bump}	Number of flip chip bump
N_{via}	Number of flip chip via
N_{RTD}	Number of resistance temperature sensor/detector
$N_i^{(e)}$	Shape function for Lagrangian 9-node element
P	Total dissipated power, W
$\overline{P}$	Heat flux, W/cm^2
P_{cache}	On-die integrated cache power, W
P_{cell}	Single cell dissipated heat, W
P_{core}	Core processor power, W
P_{in}	Work input to the refrigeration, W
$P_{non\text{-}unif}$	Total non-uniform dissipated power, W
P/T	Precision to tolerance ratio, %

Q	Refrigeration capacity or cooling power, W
R	Cache and Core power ratio
R_{heater}	Electrical resistance of the serpentine metal resistor heater, Ω
R_{jc}	Junction-to-case thermal impedance, ^{o}C cm^2/W
R_{jp}	Junction-to-plate thermal impedance, ^{o}C cm^2/W
$R_{jp,\ max}$	Maximum allowable junction-to-plate thermal impedance, ^{o}C cm^2/W
$R_{jp,spec}$	Junction-to-plate thermal impedance specification, ^{o}C cm^2/W
R_{leg}	Electrical resistance of individual heater leg, Ω
R_{RTD}	Electrical resistance of the serpentine metal resistance temperature sensor/detector, Ω
R_s	Metal layer sheet resistance, Ω/square
R_{shunt}	Resistance of the shunt, Ω
T	Temperature, ^{o}C
T_a	Ambient temperature, ^{o}C
T_c	Case temperature, ^{o}C
T_{exp}	Measured temperature from experiment, ^{o}C
T_i	Nodal temperature, ^{o}C
T_j	Junction temperature, ^{o}C
$T_{j,\ actual}$	Actual junction temperature, ^{o}C
$T_{j,\ i}$	Junction temperature of the *i* th region or cell of the die
$T_{j,\ max}$	Maximum die temperature, ^{o}C
$T_{j,\ predict}$	Predicted junction temperature, ^{o}C
T_m	Melting temperature, ^{o}C

T_{model}	Predicted temperature from model, ^{o}C
T_p	Thermal plate temperature, ^{o}C
T_{AV}	Average temperature of TEC, K
T_C	Cold side temperature of TEC, K
T_H	Hot side temperature of TEC, K
T_{room}	Room temperature, K
V_{max}	Voltage limit for voltage control thermal measurement setup, V
V_{shunt}	Voltage drop across the shunt, V
W_{FB}	Fireball heater width, mm
W_{RTD}	Resistance temperature sensor/detector width, mm
Z	Figure of merit, 1/K

Greek letters:

α_s	Seebeck coefficient
ρ_{TE}	Resistivity of TEC element
σ	Standard deviation of thermal data
ΔT	Temperature differential, ^{o}C
ΔT_{max}	Maximum temperature differential, ^{o}C
ΔV	Voltage or potential difference, V
Ψ_{jp}	Junction-to-plate thermal relation resistance, $^{o}C\ cm^2/W$
Ψ_{cp}	Case-to-plate thermal relation resistance, $^{o}C/W$
Ψ_{jc}	Non uniform power junction-to-case thermal relation resistance, $^{o}C/W$
Ψ_{jc}'	Uniform power junction-to-case thermal relation resistance, $^{o}C/W$
Ψ_{jp}	Junction-to-plate thermal resistance, $^{o}C/W$

$\Psi_{jp,spec}$	Junction-to-plate thermal resistance specification, ^{o}C/W
Θ_{ja}	Junction to ambient thermal resistance, ^{o}C/W
$\Theta_{ja,\ avg}$	Average junction to ambient thermal resistance, ^{o}C/W
$\Theta_{ja,\ i,}$	Chip-location-specific junction-to-ambient thermal resistance, ^{o}C/W
ζ_i	Cell specific thermal resistance, ^{o}C/W

CHAPTER 1 – INTRODUCTION

The invention of the bipolar transistors by John Bardeen, Walter Brattain, and William Shockley at Bell Laboratories in 1947 foreshadowed the development of generations of microelectronics. The invention of the silicon integrated circuit (IC) by Jack Kilby of Texas Instruments in 1958 and the planar process technology that was used to commercialize IC by Robert Noyce and Jean Hoerni of Fairchild Semiconductor in 1959 further excited the development of generations of scale integrations: small (SSI), medium (MSI), large (LSI), very large (VLSI), ultra large (ULSI), giga (GSI), and many others yet to come.

The IC chip is not an isolated island. It must communicate with other IC chips in a circuit through an input/output (I/O) system of interconnects. Furthermore, the IC chip and its embedded circuitry are delicate, requiring the package to both carry and protect it. Consequently, the major functions of the microelectronic package are: (1) to provide a path for electrical current that powers the circuits on the IC chip; (2) to distribute the signals onto and off the IC chip; (3) to remove the heat generated by the circuits on the IC chip; and (4) to support and protect the IC chip from hostile environments.

Figure 1.1 shows a schematic representation of microelectronic package hierarchy. Packaging focuses primarily on how chips may be packaged cost effectively and reliably. Packaging is an art based on the multi-disciplinary sciences of establishing interconnections ranging from zero level packages (i.e. chip level connections e.g. gold bond wire and solder bumps), to first level packages (either single- or multi-chip modules), second–level packages (e.g. printed circuit board (PCB)), and third-level packages (e.g. motherboard). It should be recognized that in this four-level hierarchy, a transistor on an IC might communicate by means of an electrical or optical signal to another IC. This signal communication poses a whole set of electrical, mechanical, thermal, chemical, and

environmental challenges which if not properly engineered and manufactured, may result in either poor communication or no communication at all. Each of theses challenges involves several key parameters or characteristics which often counteract with each other i.e. improvements in one often leads to deterioration in another. Furthermore, the current technologies are approaching numerous fundamental limits set by the properties of materials and by the structural geometries of packaging.

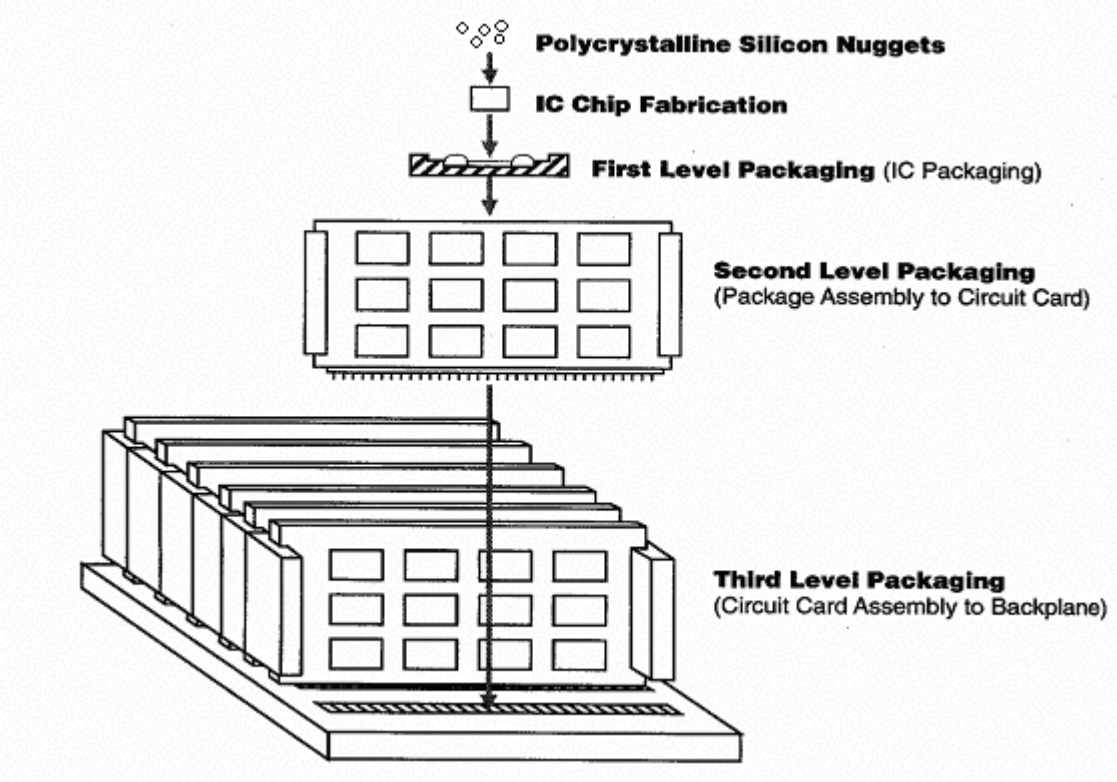

Figure 1.1 Microelectronic Package Hierarchy

In this chapter, the IC background and trends are briefly discussed, followed by a brief update of microelectronics packaging technologies. Driving factors of packaging performance from the electrical, mechanical, and thermal design perspectives are briefly discussed. Background on thermal management as one of the key enabling elements to microelectronics packaging development is also elaborated.

1.1 IC Background and Trends

The past decade has witnessed an explosive growth in IC density i.e. number of transistors per chip and chip size. One of the key reasons is the advancement of the CMOS (complementary metal-oxide-semiconductor) process as depicted in Figure 1.2, which has very fine feature sizes and high yields (Figure 1.3.) Today, 0.13 μm is in volume production. According to International Technology Roadmap for Semiconductor (ITRS) (Semiconductor Industry Association, 2001), 90 nm technology is required for volume production in the year 2004 (Table 1.1).

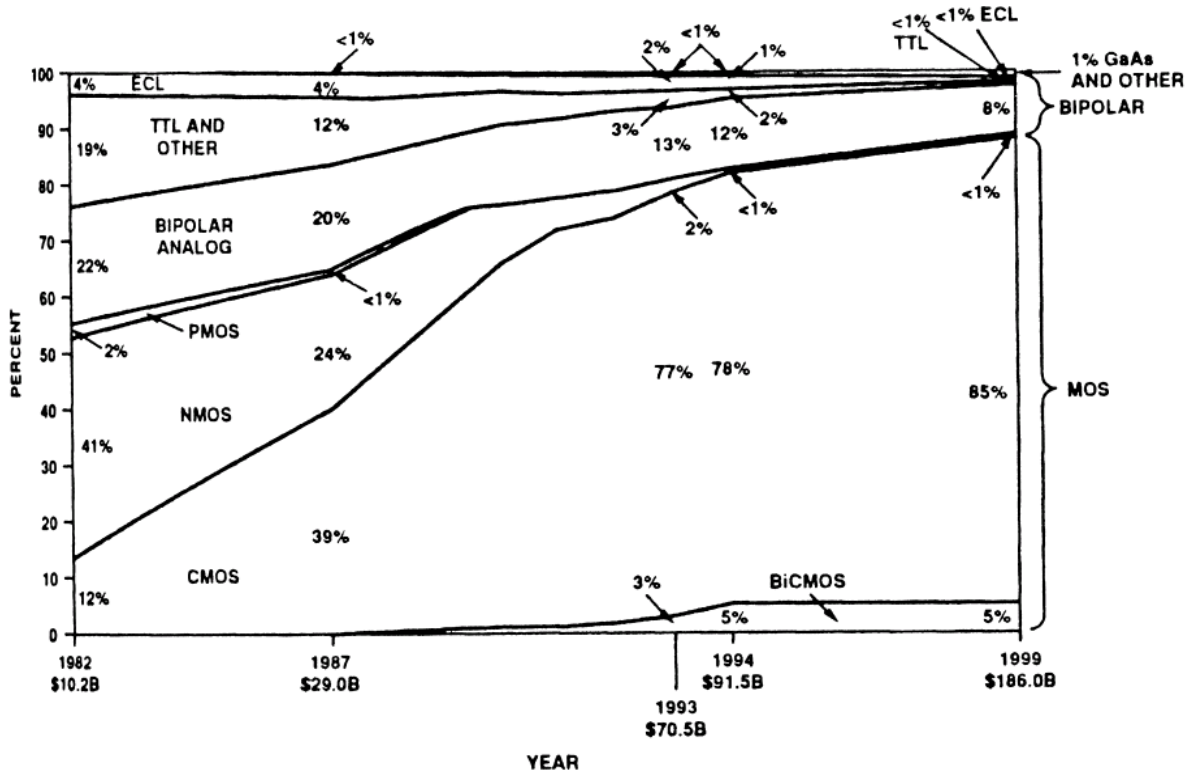

Figure 1.2: IC Process Technology Trends (Tummala, 2001)

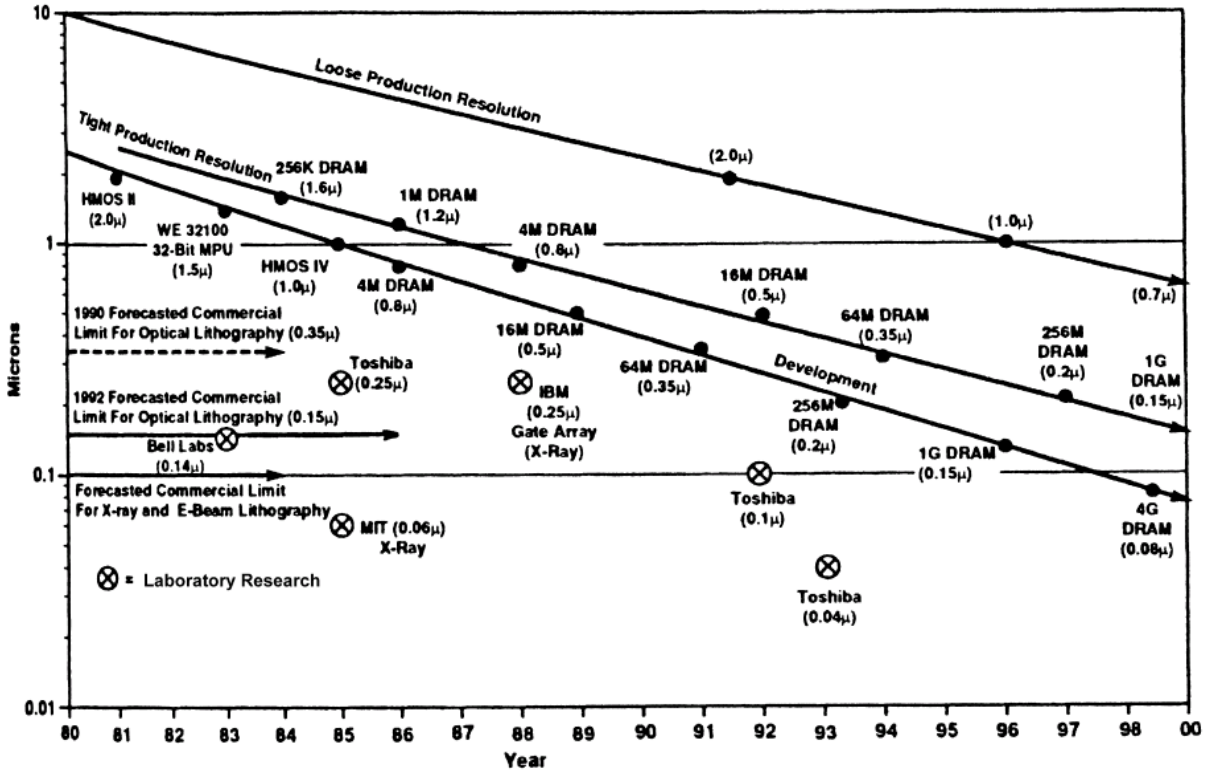

Figure 1.3: IC Feature Size Trends (Tummala, 2001)

Table 1.1 Lithography Technology Requirements for High Performance Logic Devices (Semiconductor Industry Association, 2001)

Year of Production	2001	2002	2003	2004	2005	2006	2007
Line Width (nm)	130	115	100	90	80	70	65
Gate Length (nm)	65	53	45	37	32	28	25
Gate Oxide Thickness (nm)	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1
Power Supply (V)	1.2	1.1	1.0	1.0	0.9	0.9	0.7

Because of the explosive growth in portable microelectronic products, the operating voltage (power supply) on the IC chip has been reducing from 5 V in the '90s to 1.0 V now, and to 0.9 V in 2005, then 0.7V in 2007 as can be seen from Figure 1.4 and Table 1.1. One of the key reasons is that the power consumption is proportional to the square of the

operating voltage – that is, the lower the operating voltage the longer the battery life for portable microelectronic products.

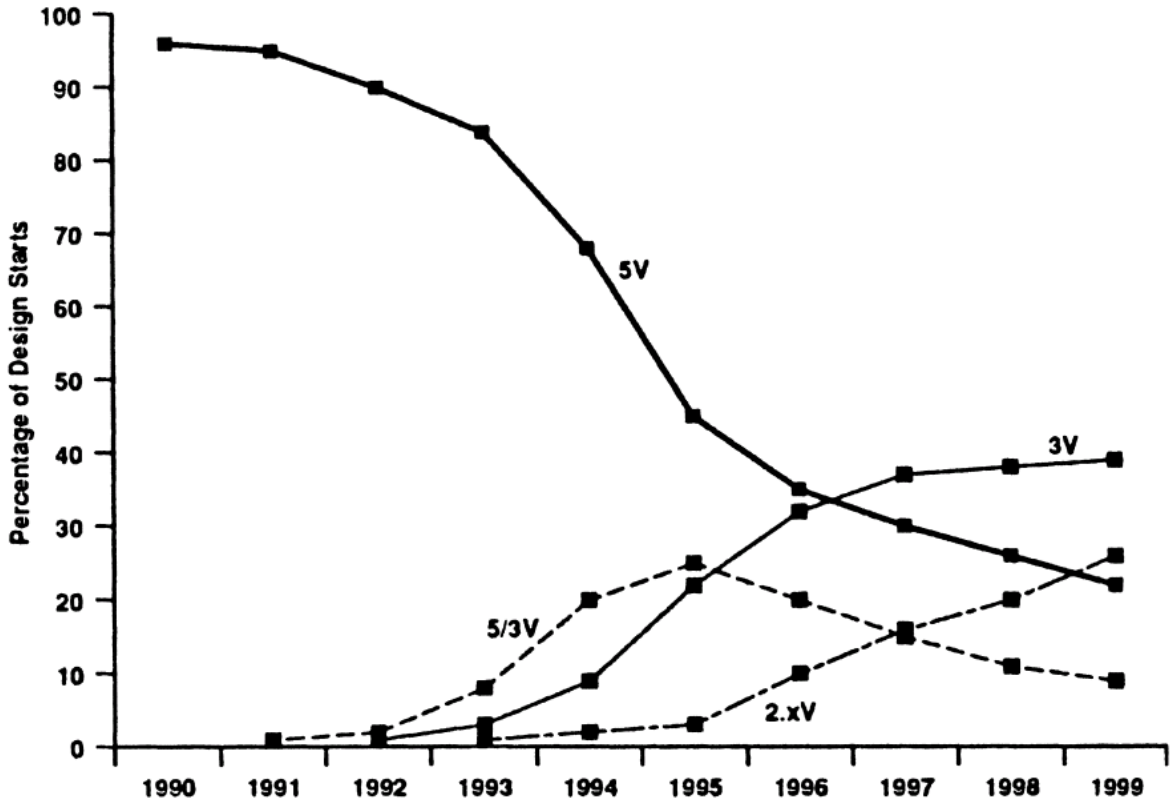

Figure 1.4: Transition of Operating Voltage (Tummala, 2001)

In most microelectronic products, there are four major IC devices: the microprocessor, the ASIC (application-specific IC), the cache memory, and the main memory. For example, the personal computer usually has one microprocessor; a few cache memories [e.g., fast SRAM (static random access memory)]; a few ASICs (e.g. video, sound, data path, high speed memory controller, NuBus controller, I/O controller); and many system memories such as ROM (read only memory), which contain permanent code used by software applications, and DRAM (dynamic random access memory) to store the information while power is turned on.

The microprocessor is the brain of a computing system. Some of the well known ones are: Intel's CISC (complex instruction set computing)-based microprocessor family (e.g. Pentium IV); Intel's RISC(reduce instruction-set computing)-based

microprocessor(e.g. StrongArm, Xscale, etc.); Intel's RISC-based microprocessor (e.g. Itanium and Itanium2) IBM, Motorola, and Apple's RISC-based PowerPC microprocessors; Hewlett-Packard's RISC-based PA8000; Digital Equipment Corporation's RISC-based Alpha microprocessor; Silicon Graphics' RISC-based MIPS; AMD's CISC-based K6 and Athlon; Cyrix's CISC-based 6x86; and Sun Microsystem RISC Ultra Sparc. Both RISC-based and CISC-based microprocessors are expected to require over 1000 package pin counts and to perform over 400 MHz on chip clock frequency as shown in Figure 1.5.

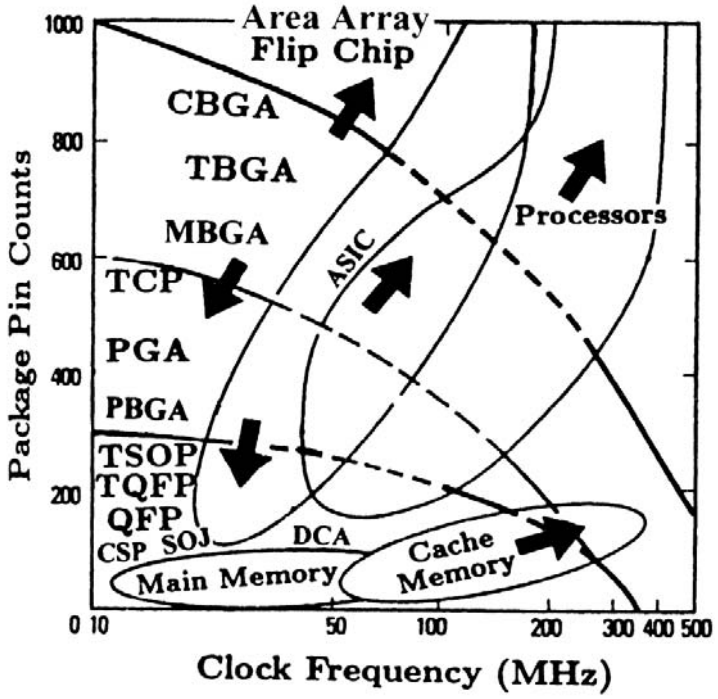

Figure 1.5: IC Devices and Packaging Trends (Tummala, 2001)

The SRAMs for cache memories are expected to perform at high speed similar to that of microprocessors to prevent system data bottle necks. Even the ASICs are already running faster than 500 MHz on chip clock frequencies and have more than 1000 package pin counts.

Packaging technology is hard-pressed to meet all these requirements. Packaging becomes the bottleneck of high speed computing if advancement in packaging technologies

cannot keep pace with the semiconductor IC technologies. Thus, there is a golden opportunity to make a major contribution to the microelectronics industry by developing innovative and useful microelectronic packages.

1.2 Packaging Technology

For many years, the microelectronics industry has been concentrating on increasing the performance of ICs (i.e., more circuitry/silicon area operating at higher speeds) with little consideration of the fact that ICs in a microelectronic system must communicate with each other through the package containing them. As a result of the trend towards higher circuit densities and operating frequency on a chip, many effects become important considerations for packaging technology development such as: I/O requirements increasing sharply; signal transition time between ICs becoming a limiting factor to system speed; signal integrity between ICs degrading; power requirements per IC increasing thus creating a problem of heat dissipation in microelectronics packaging. All of these factors have forced microelectronics packaging technology into the spotlight in reconsideration of how ICs are being packaged. From these reconsiderations, many variants of packaging technologies have evolved to cater for different semiconductor IC devices and applications. Figure 1.5 shows some common packaging technologies available to date for the above mentioned four major IC devices: Microprocessor, ASIC, cache memory, and system memory.

Figure 1.5 is divided into four regions (with three lines) of applications. The first region is for low-pin count IC devices, and the packaging technologies are, for example, PQFP (plastic quad flat pack), SOP (Swiss outline package), SOJ (Swiss outline J-leaded), SOIC (small outline IC), PLCC (plastic leaded chip carrier), DCA (direct chip attach on PCB), and CSP (chip scale package). Some examples of DCA are shown in Figures 1.6 through 1.9. Figure 1.6 shows a solder bumped flip chip on PCB. Figure 1.7 shows a stud

gold bumped flip chip on PCB with isotropic conductive adhesive. Figure 1.8 shows a stud gold bumped flip chip on PCB with anisotropic conductive adhesive (ACA) which has different conductivity in different directions. Figure 1.9 shows a gold bumped flip chip with anisotropic conductive film (ACF). ACA consists of thermosetting adhesive and conductive particles and it looks like paste. ACF consists of thermosetting adhesive, conductive particles, and release film and it looks like paper as can be seen from Figure 1.10. Figure 1.11 shows an example of a 3-D stacked CSP.

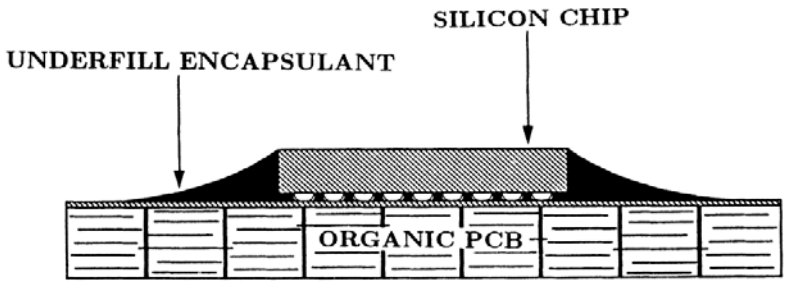

Figure 1.6: Solder Bumped Flip Chip on PCB (DCA)

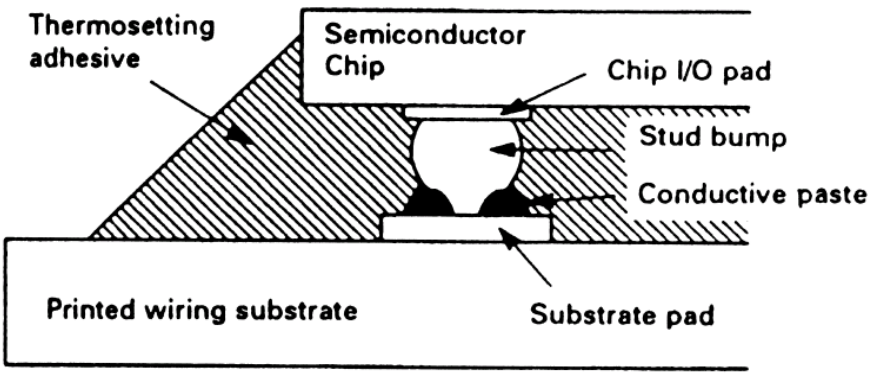

Figure 1.7: Solderless Flip Chip with Stud Bumps and Conductive Paste (DCA)

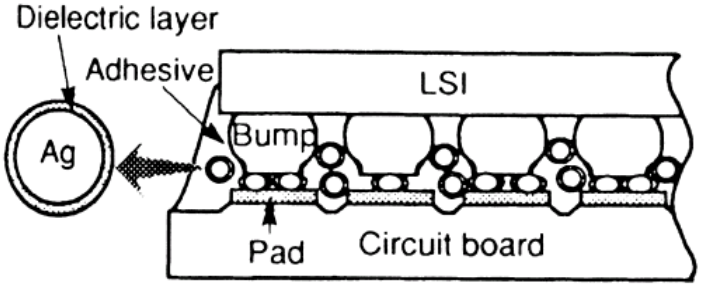

Figure 1.8: Solderless Flip Chip with Anisotropic Conductive Adhesive (ACA) on PCB (DCA)

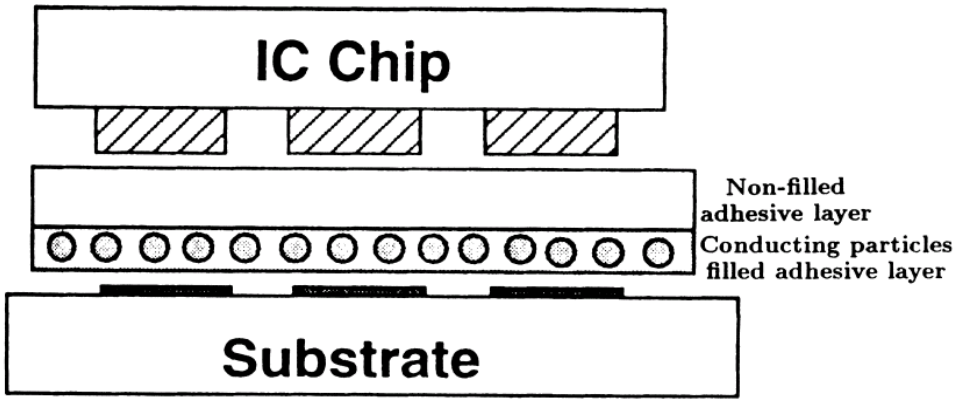

Figure 1.9: Solderless Flip Chip with Anisotropic Conductive Film (ACF) on PCB (DCA)

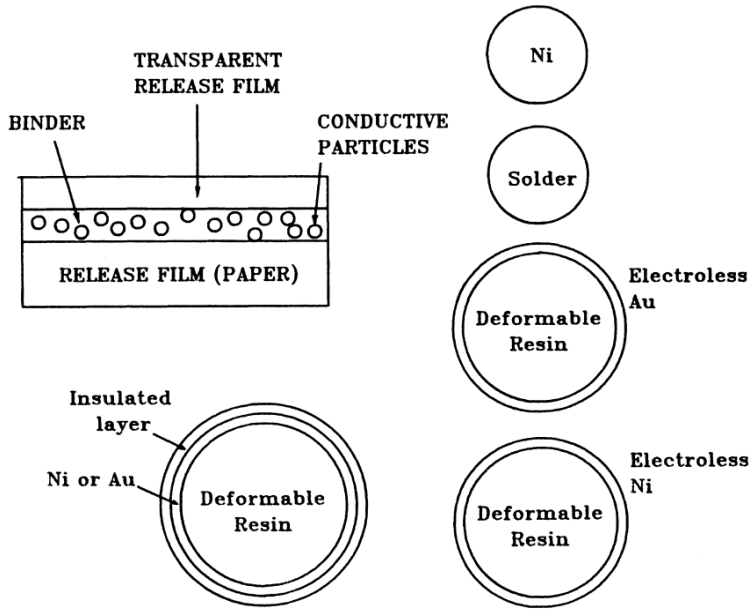

Figure 1.10: Typical Anisotropic Conductive Film (ACF)

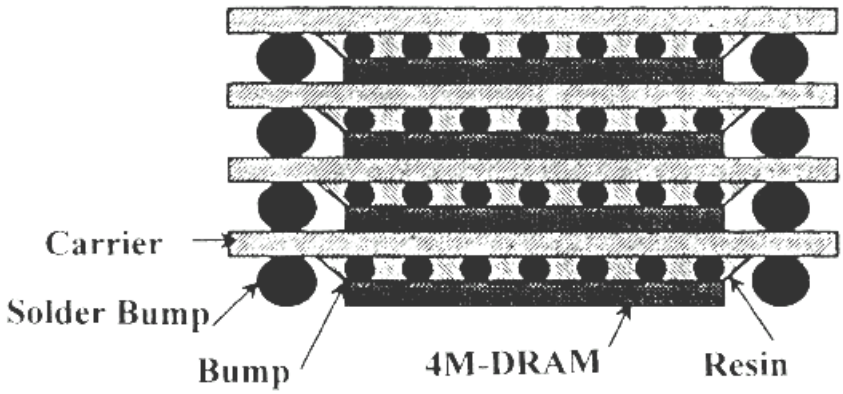

Figure 1.11: NEC 3D Stacked Chip Scale Package (CSP) for Memory Devices

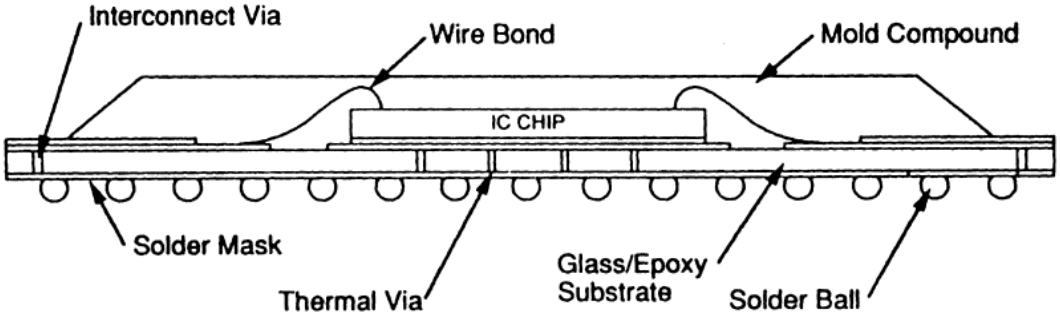

Figure 1.12: PBGA with Wire-bonding Chip on Organic Substrate

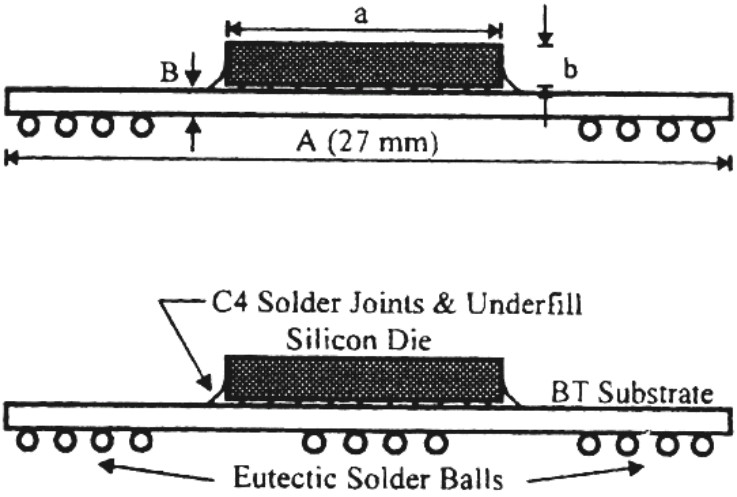

Figure 1.13: PBGA with Solder Bumped Flip Chip on Organic Substrate

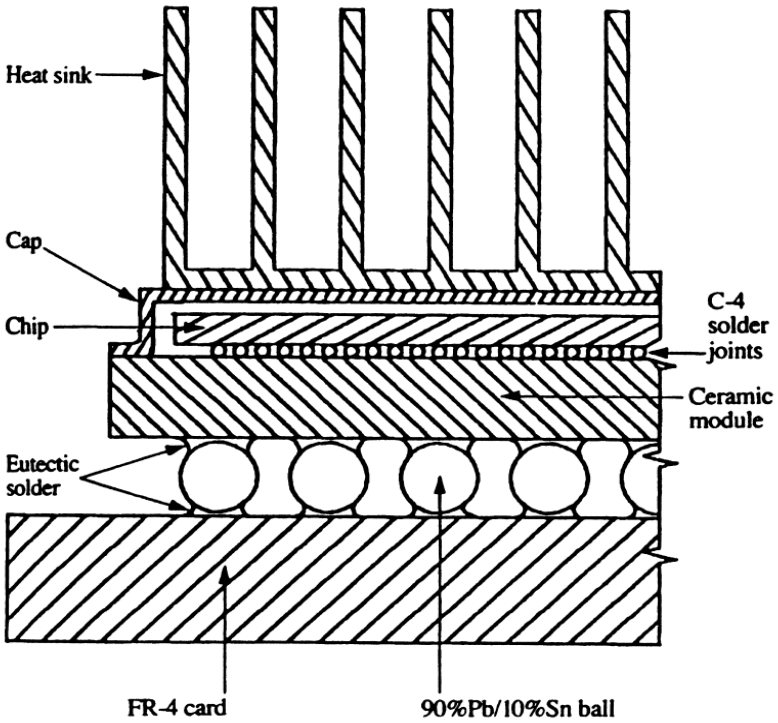

Figure 1.14: CBGA with Heat Sink (C4: Controlled-Collapse Chip Connection)

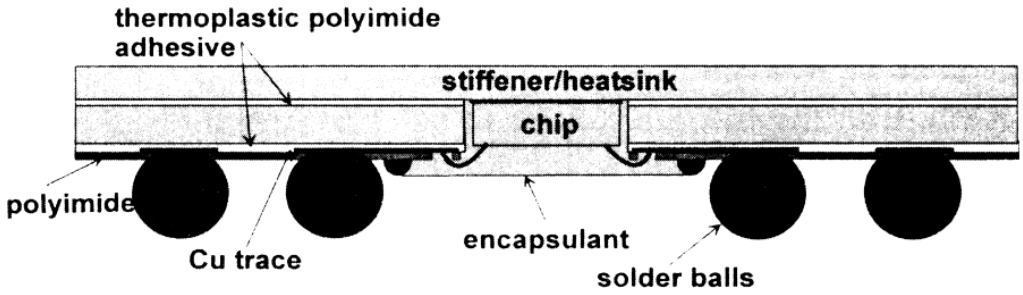

Figure 1.15: 3M Single Metal layer Cavity Down Wire-Bonding TBGA

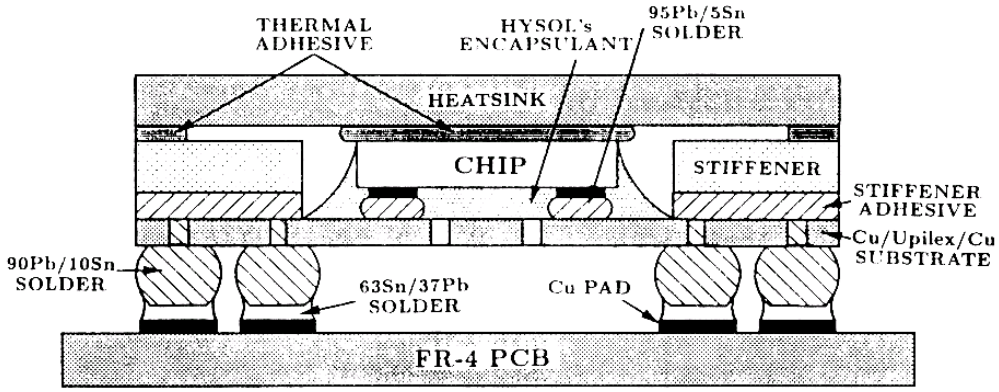

Figure 1.16: IBM Area Array Solder Bumped Flip Chip TBGA

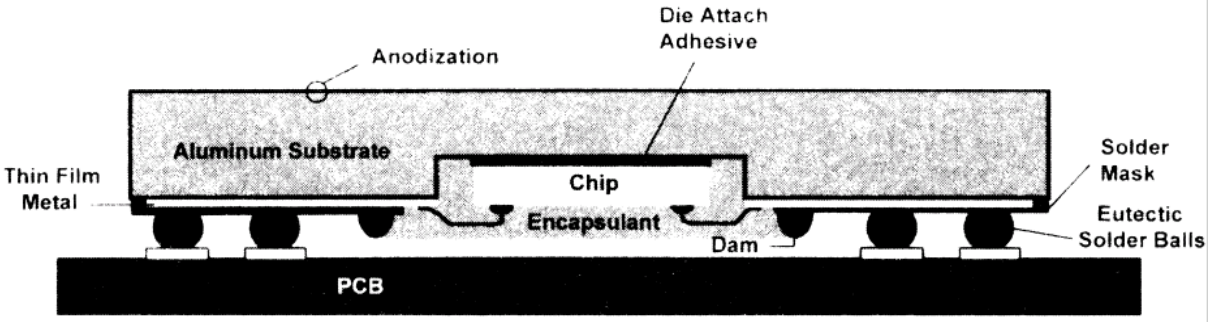

Figure 1.17: Olin Metal BGA (MBGA) with Wire-Bonding

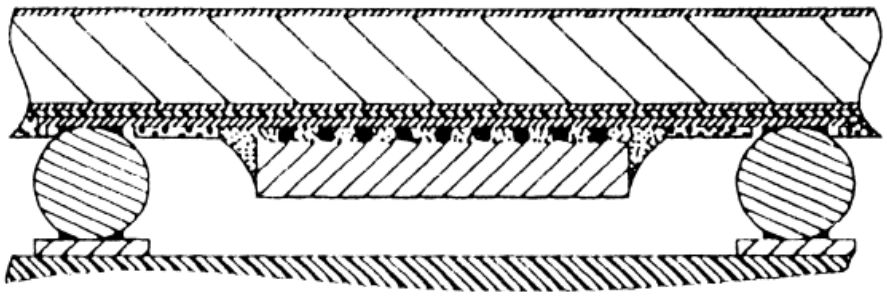

Figure 1.18: IBM MBGA with Solder Bumped Flip Chip

The packaging technologies such as TCP (tape carrier package), PPGA (plastic pin grid array), CPGA (ceramic pin grid array), and PBGA (plastic ball grid array) meets the

needs for the second region of applications. Some examples of PBGA are shown in Figure 1.12 for a wire bonded PBGA whereas a set of solder bumped flip chip PBGAs is shown in Figure 1.13. For higher pin-count and performance IC devices (the third region of applications), CBGA (ceramic ball grid array) is shown in Figure 1.14, TBGA (tape ball grid array) is shown in Figures 1.15 and 1.16, and MBGA (metal ball grid array) is shown in Figures 1.17 and 1.18. All of them are cost-effective packaging technology. For the forth region of applications (very high pin count and performance IC devices), area-array solder bumped flip chip technology is the solution.

1.2.1 Area-Array Flip Chip Technology

For high-price and high performance microprocessor and ASICs, complex IC designs require very high I/O and performance packages. For these types of IC and subsystems, area array solder bumped flip chip technology provides a viable answer to performance needs (Figure 1.15). Usually, they are packaged in a CPGA, a PPGA, a CBGA (Figure 1.14), a TBGA (Figure 1.16), or a MBGA (Figure 1.18) in a single-chip format. Recently, PBGAs with solder bumped flip clip (Figure 1.13), also known as flip chip ball grid array (FCBGA), have been considered for housing the high-price, high-speed microprocessors and ASICs.

1.2.2 Ball Gird Array (BGA) Technology

There are many different kinds of BGA packages (Lau, 1995). Depending on their substrates, there are CBGA (Figure 1.14), MBGA (Figures 1.17 and 1.18), TBGA (Figures 1.15 and 1.16), and PBGA (figure 1.13). Figure 1.15 shows that high I/O and performance ASICs and microprocessors, CBGA, MBGA, and TBGA could meet the high pin count (>500), power, and clock-frequency requirements but with higher costs.

Due to the fine pitch and pin-count limitations of PQFP and high cost of CBGAs, MBGAs, and TBGAs, the PBGA is a cost effective technology for package pin-count lying between 250 and 500. The major difference between PQFP and PBGA is that PQFP has a leadframe and PBGA has an organic substrate. The leadframe has been standardized for fanning the circuitry for more than 15 years, while the PBGA's substrate is still custom-designed. Today, the leadframe is cheaper than the organic substrate. Thus, in order for the PBGA packages to be popular, its substrate has to be standardized at a lower cost.

1.2.3 TCP

TCP offers smaller pitches, thinner package profiles, and smaller footprints on the PCB. TCP can provide moderate-performance solutions for applications such as ASICs and microprocessors with up to about 600 package pin counts (Intel uses TCP to house its previous generation Pentium microprocessors for portable computers). It is noted that unless volume production is very high, TCP may not be cost effective due to the very high development cost of these custom-designed packages. Also, TCPs suffer the same drawbacks (e.g. peripheral chip carrier, long lead length, handling, board level manufacturing yield loss) as the PQFPs.

1.2.4 TSOP and PQFP

Up to 208-pin (0.5 mm pitch and 28 mm body size), 240-pin (0.5 mm pitch, 32 mm body size), and 304-pin (0.5 mm pitch and 40 mm body size), PQFPs (Lau & Pao, 1997, Lau, 1994b) are the most cost-effective packages for SMT (surface mount technology). They have been used extensively for ASICs, and low-performance and low-pin-count microprocessors. Sometimes, they are used to house one or more cache memories. Currently, the price for the PQFP packages is less than one cent a pin. For example, the listing price for the 208-pin PQFP is less than US$1.50.

TSOP is a very low profile plastic package, which is specifically designed for SRAM, DRAM, and flash memory (which retains information even when the power is turned off) devices for space –limit applications. Right now, the price for TSOP is less than one cent a pin.

1.2.5 CSP and DCA

One of the most cost effective packaging technologies is DCA (Lau & Pao, 1997, Lau, 1996, 1994a) as shown in Figures 1.6 through 1.9. However, because of the infrastructure and cost in supplying the known good die (KGD) and the cost and availability of corresponding fine line and spacing PCB (Figure 1.19), many technologists in the industry are still working on these issues. However, it should be noted that with the sequential build-up of PCB technologies such as DYCOstrate, plasma etched redistribution layer (PERL), surface laminar circuits (SLC), film redistribution layer (FRL), interpenetrating polymer build-up structure system (IBSS), high density interconnect (HDI), conductive adhesive bonded flex, sequential bonded films, sequential bonded sheets, and microfilled via technology, 0.5 mm (2-mil) line width and space PCBs should be available in the near future.

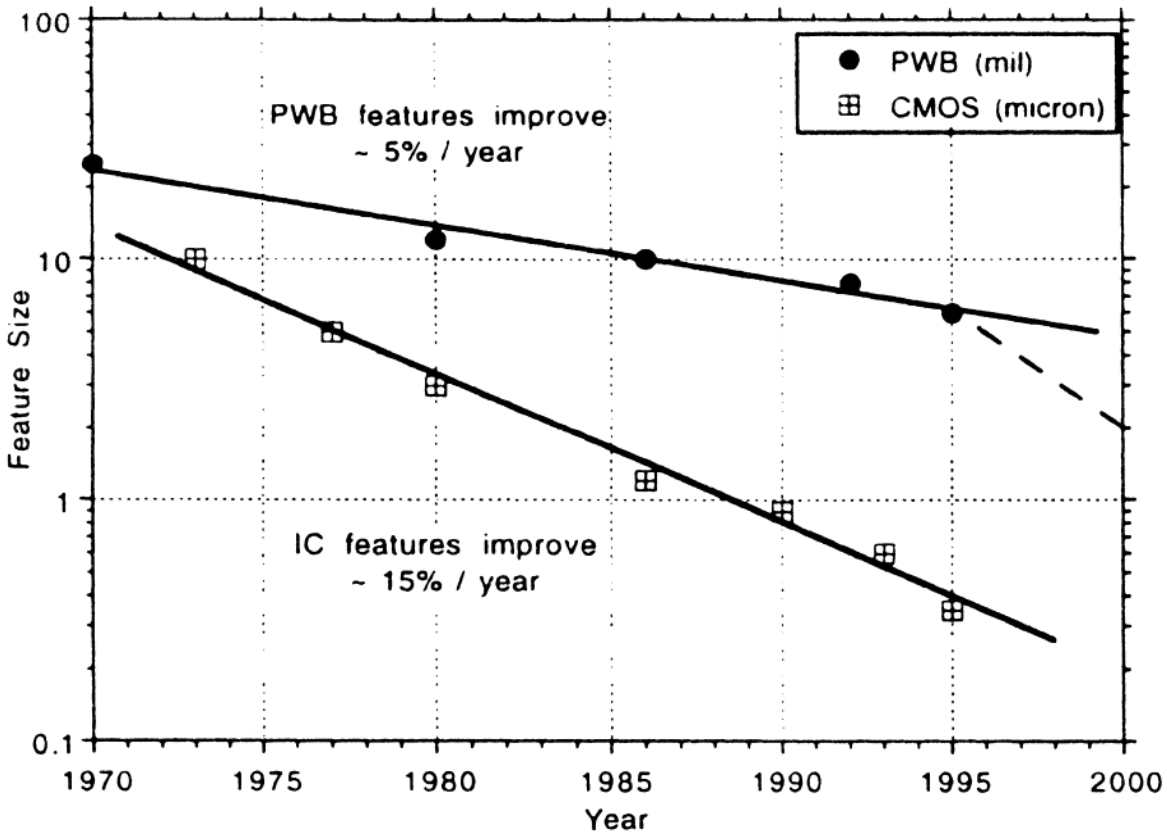

Figure 1.19: PCB and CMOS Feature Size Trends (Tummala, 2001)

In the meantime, a new class of technology called chip scale package (CSP) has surfaced. There are more than 40 different CSPs reported today (Lau & Lee, 1998) and most of them are used for SRAMs, DRAMs, flash memories and not-so-high-pin-count ASICs and microprocessors. The unique feature of most CSPs is the use of a substrate (carrier or interposer) to redistribute the very fine pitch (as small as 0.075 mm) peripheral pads on the chip to much larger pitch (1 mm, 0.75 mm, and 0.5 mm) area-array pads on the PCB.

The main advantages of CSP over DCA are that with the carrier (interposer), the CSP is easier to test-at-speed and burn-in for KGD. Furthermore, CSP is easier to handle, to reassemble, to rework, to standardize, to protect the die, to deal with die size shrinkage and it is subject to less infrastructure constraints. On the other hand, the advantages of DCA are that it has better electrical and thermal performance, and weighs less, smaller in size, and lower in cost.

1.3 Driving Factors on Packaging Performance

Historically, packaging has always been a substantial fraction of the cost of an IC (anywhere from 10% to 50%), and consequently, reducing packaging cost while maintaining reliability and performance has been the focus of packaging technology development. During this time, IC technology has transitioned from small-scale integration (SSI) in the 1960s to submicron feature size very-large-scale integration (VLSI) at the present time. Since packaging technology has not enjoyed anywhere near the performance advancement of ICs over the past 30 years, microelectronic system performance has become increasingly limited by IC packages. Thus, design decisions facing in the packaging technology development today are becoming increasingly driven by device performance.

Given the performance as one of the key primary concerns in microelectronics packaging, it is important to carefully examine the driving factors which relate performance to packaging technology choices. In general, a successful IC package can be gauged from its electrical, mechanical, and thermal performance. Factors for considerations in these areas are briefly discussed below.

1.3.1 Package Electrical Design

The on-chip switching speeds of ICs are continuously increasing. Furthermore, noise margins are generally decreasing at the same time. Unfortunately, chip I/O count and interconnection speed have not kept pace so that packaging interconnects now play a dominant and limiting role in determining overall system performance. Each lead from the chip to the package and each package lead to outside world has some parasitic capacitance, resistance, and inductance that limits the switching speed, distort the shape of signal passing through it, and serves as a source of electrical noise. These leads are also a source

of reliability problems. Likewise, the pattern of metal and dielectric that forms the circuitry between chips and from chips to outside world of a package contributes to the degradation of electrical performance. Consequently, some electrical design factors which must be considered include signal lead length (short parallel runs to minimize mutual inductance and crosstalk, and short runs near the ground plane to minimize the capacitive loading), use of matched impedances to avoid signal reflection, low ground resistance for minimum power supply drop, and power supply spiking caused by signal lines switching simultaneously. All of these factors are functions of geometries and materials used in packaging technology.

1.3.2 Package Mechanical Design

Mismatches in coefficients of thermal expansion (CTE) can cause stresses to be induced in ICs, package substrate, and packages of a microelectronic system as the temperature changes. Such stresses can be very localized, for example, under a small portion of the chip, or universal such as across an entire layer of a package substrate. Thus mechanical design aspect of microelectronic packaging technology is, in general, closely related to changes in temperature. Another mechanical property that may need to be considered is stiffness, characterized by the tensile modulus (E), which is important in area such as the chip attach where three materials (chip, package substrate, and adhesive) form two interfaces. Thermal stresses increase with increasing E and decreasing thickness of the adhesive layer. Thus, for example, a thin layer of high E adhesive material should only be used with larger area chips if CTE of the substrate or package closely matches that of the chip.

1.3.3 Package Thermal Design

The primary objective of thermal design or in a broader term thermal management is to control or remove the heat generated from the junctions of ICs. Heat generation in every microelectronic device and circuit is unavoidable and usually detrimental to its performance and reliability. Heat may be generated by the devices themselves or may present from other sources, both internal and external. Although heat dissipation per gate of ICs has decreased in recent years, the power dissipation per chip has increased during the same time since power per gate scales linearly with feature size, while on-chip circuit power density increases as the square of the feature size reduction ratio. Even CMOS circuit densities and operating frequencies are becoming great enough that thermal management cannot be ignored when packaging these chips.

The trend in packaging microelectronic systems, subsystems, and ICs has been to reduce in size and increase in performance, both of which contribute to heat generation and concentration. Evidence of this trend can be seen in the higher levels of integration in semiconductors and increased usage of hybrids and multichip modules (MCMs). Placing more functions in a smaller package has resulted in higher heat densities, mandating that thermal management be given a higher priority in the design cycle in order to maintain system performance and reliability.

Thermal design in microelectronic packaging involves temperature prediction of the microelectronic device during its performance as a result of operational losses or ambient heat and the application of thermal management principles to keep the temperature below the level which will cause circuit performance to degrade or cause the circuit to fail prematurely. Unfortunately, thermal management is often not well understood by most engineers in microelectronic design except by the regular practitioner. Further, in many cases, the task usually falls to one who does not have the necessary background. In such a

situation, the outcome is usually either the thermal management scheme is woefully inadequate causing the ICs to fail soon after they begin to operate, or the thermal design is massively over-designed, resulting the packaged ICs to be too large, too heavy, and too expensive.

The effect of heat on the performance and reliability of a microelectronics circuit needs to be comprehended in order to optimize the thermal design. Each circuit behaves differently depending on the components, the layout, the materials, and must be analyzed on an individual basis. Virtually every parameter of every component is a function of temperature to some extent, and the cumulative effect must be known in order to establish a maximum operating temperature for the circuit. Changing the temperature of passive devices typically changes their material properties. For example, film resistors have coefficients of thermal expansion (CTE) that range from several to several hundred ppm/^{o}C. Ceramic capacitors depending on the dielectric material used have CTE variations from less than 30 ppm/^{o}C to as much as 60% over the military temperature range (-40^{o}C to 140^{o}C). The gain in bipolar transistors may change by a factor of more than three over the same range, and leakage currents may double for every 10^{o}C rise in temperature.

Heat also has detrimental effect on the reliability of an IC. Following the same mathematical pattern as leakage currents, the rate of chemical reaction doubles with every 10^{o}C temperature rise, accelerating such failure mechanisms as junction failure, metallization failure, corrosion, and electromigration diffusion. The rise in leakage currents may ultimately result in thermal runaway and catastrophic failure. Excess heat also accelerates the drift mechanisms in resistors and may ultimately result in circuit failure.

Clearly, thermal management is one of the most important tasks in microelectronics packaging. Developing a systematic process leading to a thermal design meeting the

requirements of the IC without being excessive will result in IC meeting not only the performance requirements, but the cost and reliability requirements as well.

In general, there are three fundamental aspects which have to be taken into consideration in thermal management of microelectronics packaging. First aspect is on how and where the heat is generated. There are many sources of heat in microelectronics system, all of which must be considered. It is common to consider only the heat created by the operation of the active devices, but other components such as resistors, conductors, and even small wire bonds can generate significant heat. The location of heat is just as important as its amount. Heat generating components in the proximity may cause a temperature rise greater than the heat generated by the component or device itself.

Second aspect of thermal management involves the determination of the temperature at any given point in the circuit. Generally, temperature can be either predicted analytically through thermal analysis or determined experimentally via thermal characterization/measurement. Heat conduction is reasonably well defined, but most thermal models relating to radiation and convection are empirically determined for all but the simplest of geometries. Approximate methods solvable on a calculator or computer exist which are reasonably accurate for single device, but fall short when applied to multiple devices, complex geometries, or when convection and/or radiation must be considered. Further, they serve only to determine where the trouble spots are. To achieve the requisite degree of accuracy needed for optimal thermal management, more sophisticated approaches requiring more computational power such as workstation or supercomputer must be employed. These methods utilize finite element analyses (FEA) or finite volume analysis (FVA) and require a degree of mathematical expertise by the users. More discussions on these and other methods are presented in the subsequent chapters.

Characterization/measurement is an integral part of thermal management where measurements of thermal and flow fields in microelectronic system are conducted for the following purposes: 1. confirmation of thermal design in both product development phase and routine product screening/rating; 2. diagnosis of overheating also known as troubleshooting in the field or for prototype products; 3. monitoring of thermal state during operation. The requirements for accuracy, spatial and temporal resolution of data vary depending on the purpose of measurement. Detailed and accurate measurements of temperature are required during the product development phase. One of the ways is to use thermal sensor embedded in thermal test chip. Thermal test chip is specifically designed to determine the thermal resistance, an important parameter to characterize thermal performance of the packaging technology. The thermal test chip consists of heater elements and sensors. It is a convenient tool to evaluate the packaging design in the product development phase. Detailed challenges and design rules on thermal test chip are elaborated in the later chapters.

Last aspect of thermal management is on the heat removal by means of thermal design. The generated heat must be carried away from the junction of IC and dissipate safely. This requires the design and construction of an efficient heat path from the device through mounting surface(s) to the atmosphere can be as simple as clip-on heat sink with circulating cooling fluid both gas or liquid. An extensive knowledge of material properties and thermodynamics is required for this discipline.

1.4 Summary

A brief overview of IC devices (e.g. microprocessor, ASIC, cache memory, and system memory) background and trends has been presented. Also, various packaging technologies such as flip chip, BGA, TCP, CSP, and DCA for IC devices have been briefly discussed.

The area-array solder-bumped flip chip technology is gaining momentum to displace other interconnect technologies for very high I/O and performance single –chip modules for the microprocessors and ASICs. Usually, the area solder bumped flip chip is packaged in a CBGA, a MBGA, a TBGA or a PBGA, making them cost effective packages for microprocessors and ASICS for more than 500-pin counts and high-power dissipation. In general, PBGAs are cost effective for packaging the ASICs (and sometimes the microprocessors) with 250 to 500 pin counts and not-so-high power dissipation (less than 3 W). In some cases, PBGA with lower than 200 pin counts are also very cost effective (for performance purpose) for housing a cache or a few fast SRAMs. For thermal-enhanced PBGAs, the back of the chip is attached to a heat spreader, which can be mounted with a heat sink. In this case, its power dissipation can be as high as 30W and could be used to house microprocessors and ASICs. CSPs are usually used to package memories and low power (<1 W) and high pin-count (<200) ASICs, even though higher-pin-count and power are currently being developed in major semiconductor companies and laboratories. Except in a handful of vertically integrated companies, DCAs are still waiting for their time when KGD and high density micro-via build up PCBs will be commonly available at reasonable costs.

Packaging technology development is becoming increasingly driven by device performance. The driving forces which relate electrical, mechanical, and thermal performance to packaging technology choices have been briefly discussed. Electrical design factors that must be considered include signal lead length to minimize mutual inductance, crosstalk and the capacitive loading, use of matched impedances to avoid signal reflection, low ground resistance for minimum power supply drop and power supply spiking caused by signal lines switching simultaneously. CTE and E are important parameters in the mechanical design of packaging to minimize stresses induced

mechanically or thermo-mechanically. Thermal design in microelectronic packaging involves temperature prediction of the microelectronic device during performance as a result of operational losses or ambient heat and the application of thermal management principles to keep the temperature below the level which causes circuit performance to degrade or cause the circuit to fail prematurely. A systematic thermal management process leading to a thermal design meeting the requirements of the IC without being excessive is needed not only to meet the performance requirements, but the cost and reliability requirements as well.

CHAPTER 2 – LITERATURE SURVEY

2.1 Thermal Management Hardware

According to the ITRS (Semiconductor Industry Association, 2001), microprocessors will generate more than 200 W by the year 2005. During this period, the industry is facing major challenges in multi-chip integration, such that reducing the chip-backside volume occupied by any cooling solution is a major objective. Conventional macroscopic air-convection fin array heat sinks with fans or blowers are becoming impractical and obsolete for these levels of heat generation and integration. Moreover, conventional technology is not well suited for solving the problem of highly localized on-chip hotspots, which result from extreme heat generation within confined regions.

These developments are motivating research on novel cooling technologies. Conventional heat pipes and vapor chambers have been attractive for microprocessor cooling because they do not require an external electrical power supply and the working fluid is contained within a closed chamber (Faghri, 1995, Prasher *et al.*, 2001). However, these capillary-driven devices are not optimal for chip power exceeding a few tens of watts because of the associated increases in heat pipes cross sectional area and limitations in the wick thickness. Recent research on fully micro-machined capillary-driven loops in the silicon promises to improve heat spreading within the chip. This approach addresses the hotspot problem, but does not solve the problem of heat removal to the environment (Greif, 2001).

Another proposed solution for dissipating high heat fluxes is the use of dielectric liquid-vapor convection cooling also known as two phase cooling. Vaporization of working fluid in an evaporator attached to, or enclosing, the heat source can be employed to obtain

very high heat transfer coefficients. The added process of condensing the vapor and bringing it back to the evaporator can be accomplished in a closed loop system.