PEDOT:PSS POLYMER-BASED HETEROJUNCTION EMITTER FOR TEXTURED MONOCRYSTALLINE SILICON SOLAR CELLS

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UNIVERSITI SAINS MALAYSIA

2024

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by

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Thesis submitted in fulfilment of the requirement
for the Degree of
Master of Science

January 2024

ACKNOWLEDGEMENT

First and foremost, I would like to thank Allah because of Him, I am able to continue my academic journey until today and letting me finish my project and thesis as planned. I would like to thank my beloved parents, Rosle bin Awang and Farizan binti Mohamed @ Ismail, for believing in me and motivating me. Their blessing for letting me to study at Universiti Sains Malaysia and finish my project gives me a peaceful mind and heart.

First of all, I would like to express my deepest gratitude to my great, positive, and generous supervisor, Associate Professor Ts. Dr. Mohd Zamir bin Pakhuruddin, for providing me an opportunity to pursue this research under his supervision. His expertise in every aspect of photovoltaics (PV) has helped me to complete this thesis. His ideas, suggestions and advices really helped me when I faced problems and confusions. Thanks for giving me a lot of guidance from designing my experiments until my thesis completion.

Besides, I am deeply indebted to En. Yushamdan bin Yusof (Research Officer), Madam Ee Bee Choo, Madam Aznorhaida binti Ramli and Mr. Abd Jamil bin Yusuf as Assistant Science Officers at Nano Optoelectronics Research and Technology (NOR) laboratory, School of Physics, for giving me training and assisting me to use lab equipments. Without their help and patience, all my experiments would not have been possible. I also would like to extend my sincere appreciation to the members of Photovoltaic Materials and Devices (PVMD) group, especially Halo Dalshad Omar. I

really owe them a huge acknowledgement because of their immense support throughout my MSc journey. Thank you for being patient with me throughout this journey. I feel so grateful to be in the team. Thank you for all prayers, motivation and helps that encourage me to complete my MSc studies.

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LIST OF SYMBOLS

A	absorption
I	current
J_{SC}	short-circuit current density
min	minute
R_S	series resistance
R_{sh}	sheet resistance
R_T	total reflection
t	thickness
T	transmission
V	voltage
V_{OC}	open-circuit voltage

LIST OF ABBREVIATIONS

A.M	Air mass
AFM	Atomic Force Microscope
Al-BSF	Aluminium Back Surface Field
ARC	Anti-reflective coating
CdSe	Cadmium selenide
c-Si	crystalline silicon
CuPc	phtalocyanine
DARC	double anti-reflective coating
DI	deionised
DMF	dimethylformamide
DMSO	dimetylsulfoxide
EDP	ethylenediamine
Eg	ethylene glycol
FESEM	Field Emission Scanning Electron Microscope
FET	field-effect transistor
FF	fill factor
H_2O	water
H_2SO_4	sulfuric acid
HCl	hydrochloric acid
HF	hydrofluoric acid
HHSC	Hybrid Heterojunction Solar Cell

HNO_3	nitric acid
HOMO	highest occupied molecular orbital
IPA	isopropyl alcohol
IR	infrared
ITO	indium tin oxide
ITRPV	International Technology Roadmap for Photovoltaic
KOH	potassium hydroxide
LED	light emitting diode
MARC	multi anti-reflective coating
MoO_x	Molybdenum oxide
N.O.R	Nano Optoelectronic Research
N_2	nitrogen gas
NH_4OH	ammonium hydroxide
OH^-	hydroxide ion
P_3HT	poly-3(hexylthiophene)
PA	polyacetylene
PCE	power conversion efficiency
PE	polyethylene
PEDOT:PSS	poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate)
PERC	Passivated Emitter and Rear Cell
PSC	polymer solar cell
PV	photovoltaic
RCA	Radio Corporation of America
rpm	rotation per minute

SDR	saw damage removal
Si	silicon
TCO	transparent conductive oxide
TiO_2	titanium dioxide
TMAH	Tetramethylammonium hydroxide
UVVISNIR	UV-Visible-Near Infrared
WAR	weighted average reflection

PEDOT:PSS PEMANCAR HETEROSIMPANG BERASASKAN POLIMER UNTUK SEL SURIA SILIKON MONOHABLUR BERTEKSTUR

ABSTRAK

Kini, dominasi sel suria silikon monohablur (mono c-Si) adalah berasaskan homosimpang, di mana bahan dop fosforus jenis-n diresapkan sebagai lapisan pemancar atas wafer c-Si jenis-p untuk membina simpang p-n. Kecekapan penukaran kuasa (PCE) pada tahun 2022 dalam industri mono c-Si adalah pada 20%. Satu masalah dengan sel suria c-Si homosimpang ialah bajet terma semasa proses resapan pemancar yang menggunakan suhu yang tinggi (800-950^{o}C) untuk membina lapisan pemancar hadapan. Proses bajet terma yang tinggi menyebabkan kecacatan dalam sel suria yang merendahkan PCE. Untuk mengatasi masalah ini, sel suria heterosimpang hibrid (HHSC) dengan pemancar berasaskan polimer telah diselidik. Baru-baru ini, HHSC poli (3,4-etilinadioksithiophene):poli(stirenasulfonate) (PEDOT:PSS)/c-Si telah menunjukkan hasil yang memberangsangkan. PEDOT:PSS ialah calon yang berpotensi tinggi sebagai pemancar jenis-p untuk sel suria heteropemancar kerana mempunyai kekonduksian yang tinggi, kelutsinaran yang tinggi, keberkesanan sebagai salutan anti-pantulan (ARC), di samping boleh diproses pada suhu yang rendah. Projek ini mengkaji sifat optikal, morfologi dan elektik pemancar jenis-p PEDOT:PSS atas mono c-Si bertekstur jenis-n untuk aplikasi sel suria. Wafer mono c-Si telah ditekstur menggunakan larutan natrium hidroksida (NaOH) untuk menghasilkan pyramid tegak yang rawak di atas permukaannya. Parameter yang diubah ialah kepekatan NaOH (1%-3%), suhu pengteksturan (70^{o}C-90^{o}C) and masa (40 min-60 min). Sampel terbaik ialah 2% NaOH dengan 50 min pada 80^{o}C, yang menghasilkan

purata pantulan wajaran (WAR) 18.06%. Kekasaran RMS (R_{RMS}) sampel ialah 2.01 µm. Seterusnya, pemancar PEDOT:PSS telah disalut atas wafer bertekstur dengan kelajuan salutan yang berbeza (250-1000 rpm) untuk membentuk ketebalan lapisan pemancar yang berbeza di atas piramid. Apabila kelajuan salutan tinggi, ketebalan lapisan pemancar PEDOT:PSS berkurang. Ketebalan optimum setelah dipertimbangkan sifat optikal dan elektrik PEDOT:PSS ialah 110 nm. PEDOT:PSS atas wafer bertekstur mengurangkan WAR kepada 4.91% berbanding wafer bertekstur iaitu 17.87%. Dalam sel suria, pemancar PEDOT:PSS optimum menunjukkan kenaikan ketumpatan arus litar pintas (J_{sc}), voltan litar buka (V_{oc}) and PCE apabila dibandingkan dengan pemancar PEDOT:PSS atas wafer rujukan berpermukaan rata. PCE tertinggi yang diperoleh daripada sel suria pemancar PEDOT:PSS atas wafer bertekstur optimum ialah 5.53%. Keputusan ini menunjukkan PEDOT:PSS ialah pemancar heterosimpang dan ARC yang berpotensi tinggi untuk sel suria mono c-Si bertekstur.

PEDOT:PSS POLYMER-BASED HETEROJUNCTION EMITTER FOR TEXTURED MONOCRYSTALLINE SILICON SOLAR CELLS

ABSTRACT

Today, the dominant monocrystalline silicon (mono c-Si) solar cells are based on homojunction architecture, where n-type phosphorus dopants are diffused as an emitter layer on p-type c-Si wafer to form a p-n junction. In 2022, power conversion efficiency (PCE) of the industrial mono c-Si solar cells is about 20%. One problem with the homojunction c-Si solar cells is thermal budget during emitter diffusion process, which utilizes high temperatures (800-1000^{o}C) to form the front emitter layer. The high thermal budget process leads to formation of defects in the solar cells which can badly their PCE. To overcome this problem, hybrid heterojunction solar cell (HHSC) with polymer-based emitter is investigated. Recently, HHSC based on poly (3,4-ethylenedioxythiophene):poly(stryrenesulfonate) (PEDOT:PSS)/c-Si has demonstrated promising results. PEDOT:PSS is a promising candidate as a p-type emitter for heterojunction solar cell because of its high conductivity, high transparency, effectiveness as an anti-reflective coating (ARC), besides being capable of low-temperature processing. This work investigates optical, surface morphological and electrical properties of p-type PEDOT:PSS emitter on n-type textured mono c-Si for solar cell application. The mono c-Si wafers are textured using sodium hydroxide (NaOH) solution to form random upright pyramids on the surface. The parameter change involves concentration of NaOH (1%-3%), texturing temperature (70^{o}C-90^{o}C) and texturing time (40 min-60 min). The best sample is 2% NaOH for 50 min at 80^{o}C, which results in weighted average reflection (WAR) of 18.06%. Root mean square

roughness (R_{RMS}) of the best sample (2% NaOH for 50 min at 80^{o}C) is 2.01 µm. Then, PEDOT:PSS emitter is spin-coated on the textured wafers with varying coating speeds (250-1000 rpm) to form different thicknesses of the emitter layer on the pyramids. The higher the speed of spin-coater, the thinner the thickness of PEDOT:PSS emitter layer. The optimum thickness considering the optical and electrical properties of the PEDOT:PSS is 110 nm. The PEDOT:PSS on textured wafer reduces the WAR to 4.91% when compared to 17.87% for the textured wafer alone. In the solar cell, the optimized PEDOT:PSS emitter on the textured wafer demonstrates improved short-circuit current density (J_{sc}), open-circuit voltage (V_{oc}) and power conversion efficiency (PCE) when compared to the PEDOT:PSS emitter on the reference planar wafer. The highest PCE of 5.53% is achieved for the optimized PEDOT:PSS emitter on the textured solar cell. The results demonstrate that PEDOT:PSS is a promising heterojunction emitter and ARC for the textured mono c-Si solar cell.

CHAPTER 1: INTRODUCTION

1.1 Introduction

Solar or photovoltaic (PV) technology is one of the major branches in semiconductor industry. For the last 10 years, the photovoltaic (PV) industry has grown exponentially with an average rate greater than 35% annually. At the end of 2022, the global crystalline silicon (c-Si) cell and cumulative installed capacities of global PV energy is believed to expand to 1005 GWp due to the capacity increment. The market share still did not change from last year where 95% of total solar cell production was dominated by c-Si while only 5% for thin-film technologies [1]. The cumulative installed capacities of global PV energy in 2020 showed an extraordinary growth up 773 GW as illustrated in Figure 1.1 below. The trend of predicts cumulative installed capacities of PV energy increases exponentially from 2022 to 2030 [2]. This increment is due to cost reduction, solar technology improvement, complementary renewable energy policy, and diversified financing. The increased frequency of dispatchable PV electricity is an indication that the cost of PV coupled with energy storage is now starting to rival conventional fuels [3]. Due to these reasons, many researchers locally and internationally now are paying more attention to the development of the PV industry.

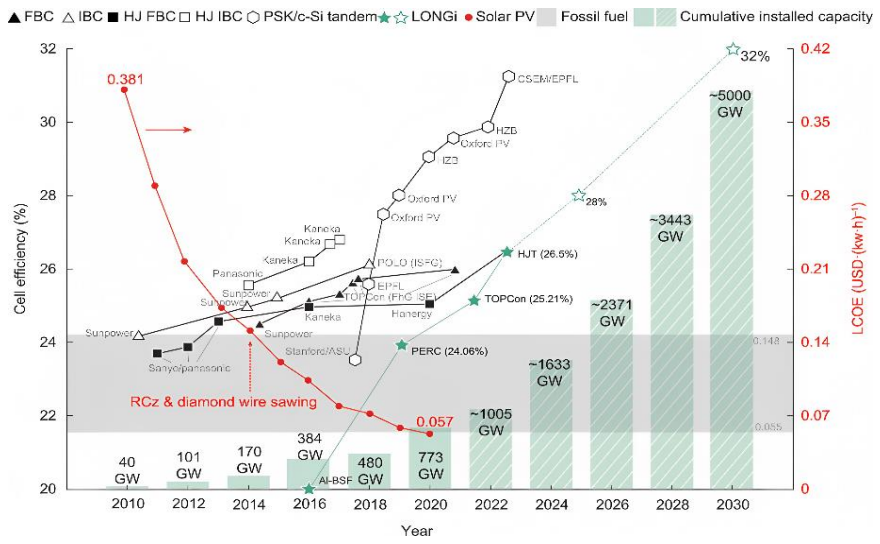

Figure 1.1 Cumulative installed capacities of global PV energy from 2010 to 2020 (green column) and predicted cumulative installed capacities of PV energy from 2022 to 2030 (shadowed green column) [2].

Although the second and third generation of solar cells are booming, the first-generation solar cell which is based on silicon (Si) has the biggest market share worldwide. At this moment, PV is dominated by wafer-based silicon (both mono- and multi-crystalline). It holds more than 90% of the market share worldwide [4]. The domination is due to their non-toxicity, material abundance, advanced fabrication technique, and long-term stability in devices [5]. C-Si has a major disadvantage which is relatively poor light absorption within 300-1100 nm wavelength region. This is due to its indirect bandgap. The absorption coefficient of c-Si is one to two orders of magnitude lower than that of a direct semiconductor in the spectral range of 300-1100 nm [6]. This problem can be mitigated by light trapping. There are several ways to trap the incident light in the c-Si. The most common one is by incorporating pyramid textures on the front surface of the c-Si through wet chemical texturing using potassium hydroxide (KOH), or sodium hydroxide (NaOH) with isopropyl alcohol

(IPA) for mono c-Si. With the pyramid textures, broadband reflection will be reduced, leading to enhanced broadband light absorption in the c-Si absorber.

Within the c-Si latest PV market share, homojunction c-Si solar cell dominates the industry [7]. There are two main technologies that use homojunction as the p-n junction which are aluminium back surface field (Al-BSF) [8] and Passivated Emitter and Rear Cell (PERC) [9]. The problem with the homojunction concept such as in PERC technology is high thermal budget due to high temperature processes during the solar cell fabrication [10]. These high-temperature processes can affect the physical properties of the materials especially the minority carrier lifetime due to formation of defects [11]. The high-temperature processes are specifically during emitter diffusion (doping to form p-n junction), electrodes co-firing, high vacuum chemical vapour deposition, etc. [12].

To overcome this issue, heterojunction solar cell is introduced. One type of heterojunction solar cell is hybrid heterojunction solar cell (HHSC). The main reason why hybrid heterojunction solar cell (HHSC) is attractive is due to the advantage of solution-based processing for organic compounds. This process enables the front emitter (i.e. p-n junction) to be formed at lower temperature (100-150^{o}C), lowering the thermal budget of the fabrication process [13], [14].

1.2 Problem Statement

Silicon is a poor light absorber especially at longer wavelength (approaching near infrared) [15]. About 30-40% of incident light is lost due to reflection. It is obvious in short wavelength range or to be precise in blue wavelength. Therefore, optical loss due

to low absorption at long wavelength and high reflection at short wavelength causes minimum light to be converted to electricity. Approximately 1 cm thick of silicon wafer is needed to fully absorb the incident light within near infrared (IR) wavelength region [15]. Thus, techniques that can prevent both limitations need to be incorporated into the silicon wafer. One of them is by front surface texturing.

Recently, the PV market is dominated by PERC c-Si homojunction solar cells. The problem with the homojunction c-Si solar cell is high temperature process during emitter diffusion process [11], which requires processing temperatures of 800-1000^{o}C to form a high-quality emitter layer. However, the high temperature process results in poor carrier lifetimes and high recombination in the solar cells. These lead to poor solar cell performance [11]. Apart from this, the high temperature process also incurs high processing cost in the fabrication. To mitigate this problem, polymer-based heterojunction emitter can be used in the solar cells. This concept involves low processing temperature for the emitter fabrication [14]. The polymer-based heterojunction emitter concept offers high carrier mobility, high transparency and high PCE to the c-Si solar cells [16]. Most polymers have low lifetime (i.e. shelf life before degradation). However, according to the literature, one key advantage of PEDOT:PSS-based device is it exhibits high stability [17]. In this context, it demonstrates a longer time (lasts up to 7 years) before it degrades, when compared to other polymers [17]. It has been found that hybrid heterojunction solar cell based on PEDOT:PSS exhibits lifetime of 7 years before suffering a degradation in the PCE [18]. This lifetime is considered high if compared to other polymer such as poly(3-hexylthiophene) (P_3HT) which normally demonstrates typical lifetime of around 6-12 months [19],[20]. One promising candidate for the polymer-based emitter is

PEDOT:PSS [21]. In this work, PEDOT:PSS (p-type) will be investigated as a heterojunction emitter on textured mono c-Si silicon solar cells (n-type).

1.3 Objectives

The objectives of this research are as the following:

1. To maximize broadband light absorption in mono c-Si within 300-1100 nm wavelength region by using front upright pyramids.
2. To investigate surface morphological, optical, and electrical properties of PEDOT:PSS emitter on textured mono c-Si.
3. To examine the electrical properties of PEDOT:PSS polymer-based heterojunction emitter in mono c-Si solar cell.

1.4 Thesis Outline

Chapter 1 gives a general overview about this project. This chapter addresses the introduction, problem statement, objectives, and thesis outline.

Chapter 2 provides theoretical background and literature review of the research. The chapters include solar spectrum, silicon solar cell, light trapping, pyramid texturing with wet etching method and polymer-based heterojunction solar cell.

Chapter 3 outlines the methodology involved in this work. This includes process flow for the fabrication of polymer-based heterojunction silicon solar cell from the texturing of n-type c-Si to the formation of metal contact, followed by characterisations of the solar cells.

Chapter 4 presents the results and discussions of the project. The project consists of two main experiments; surface texturing of c-Si and properties PEDOT:PSS emitter on textured mono c-Si for solar cell formation.

Chapter 5 concludes the research based on the results and discussion in Chapter 4. In this chapter, future recommendations for the project are also included.

CHAPTER 2: THEORETICAL BACKGROUND AND LITERATURE REVIEW

2.1 Introduction

In this chapter, theoretical background and literature review related to the work are presented and discussed. The discussion covers solar spectrum, silicon solar cell, silicon as semiconductor material and operation of silicon solar cell. Besides, the concept of light trapping and surface texturing of silicon with wet chemical etching are also discussed. Towards the end of the chapter, the latest literature related to PEDOT:PSS as conductive polymer, PEDOT:PSS as emitter and ARC in heterojunction solar cell are reviewed.

2.2 Solar Spectrum

The solar spectrum contains ultraviolet (UV), visible and infrared (IR) regions as shown in Figure 2.1. From the spectrum, it can be seen most of the energy lies between the ranges of 400 nm to 800 nm wavelength [22]. Sunlight comprises photons,

minuscule particles that carry the electromagnetic waves originating from the sun and traveling through space [23].

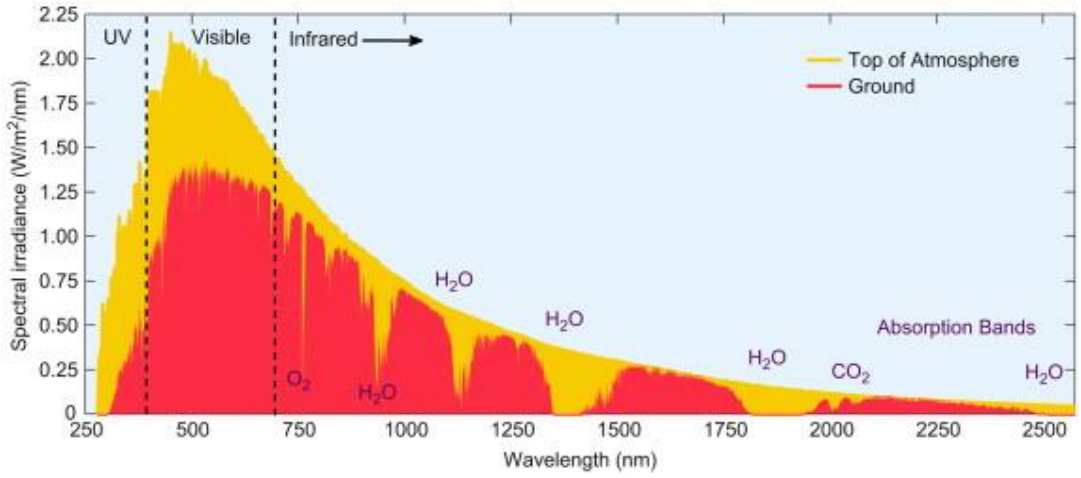

Figure 2.1 The spectral irradiance of AM1.5G solar spectrum on Earth [24].

Global standard spectrum or AM1.5G is introduced due to the terrestrial spectrum varies which cause any reference spectrum has some arbitrariness. Therefore, to make the standard spectrum representative to as many PV applications as possible, it is not derived from a particular measured spectrum, but it is calculated from the reference AM0 spectrum under representative geometric and atmospheric conditions. The settings originate from an analysis of rather sunny sites of a past measuring network in the USA [24]:

1. The air mass is 1.5 (where the sun is about 41° above the horizon)
2. The cell is tilted by 37° from the horizon (so the sun shines at an angle of 11.2° from the cell's normal vector)
3. The cell has no optical concentration system, so the cell faces a hemisphere including the surrounding ground (which is light sandy soil)

4. The site is at sea level under standard pressure (1013.25 millibars)
5. The total irradiance is 100 mW/cm^2.

Any given semiconductor material can only absorb incident photons with energy greater than its bandgap [25]. Therefore, a semiconductor material with a suitable bandgap needs to be chosen as the absorber layer in a solar cell in order to maximise the photons absorption. The most optimum bandgap for a solar cell is between 1.0-1.8 eV, as per Shockley-Queisser limit [26]. A high bandgap material (when compared to the above range) will result in the transmission loss of the photons because the material cannot absorb photons below its bandgap [27]. On the other hand, a low bandgap material (when compared to the above range) will suffer thermalisation loss since most of the incident photons possess too high energy when compared to the bandgap energy of the absorber material.

2.3 Silicon Solar Cell

C-Si solar cells can be divided into several device architectures; aluminium back surface field (Al-BSF), passivated emitter rear cell (PERC), interdigitated back contact (IBC) and heterojunction solar cell [28]–[31]. In the last 10 years, the Al-BSF was the dominant device architecture in the mass production due to its simple design architecture, high performance, robust manufacturing environment with modest power conversion efficiencies (PCE) of 18-20%. The Al-BSF technology is a diffused homojunction cell architecture with a rear side aluminium back surface field and screen-printed contacts [32]. Figure 2.2 shows the schematic diagram of Al-BSF c-Si solar cell that is used before the introduction of PERC technology.

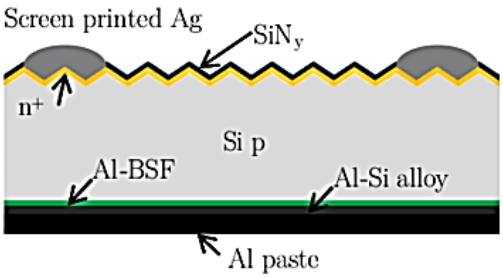

Figure 2.2 Schematic diagram of Al-BSF solar cell [33].

Later, PERC technology started to dominate the PV market due to its higher efficiency potential (above 20%). As International Technology Roadmap for Photovoltaic (ITRPV) stated, PERC cell technology will continue to dominate the current and future technology mix due to increased energy output/efficiency with minimal investment from manufacturing standpoint [1]. The PERC technology achieves a higher PCE by adding a localised dielectric passivation layer on the rear side of the cell, as shown in Figure 2.3 below. This cell technology was developed at the University of New South Wales (UNSW), Australia, in 1980s, and achieves superior PCE, owing to improved rear surface passivation by localised silicon dioxide (SiO_2) layer and increased rear reflection due to combination of SiO_2 dielectric layer and aluminium (Al) back contact design [34]. While the PERC solar cells yield conversion efficiencies of beyond 20%, there is a heavy reliance on high-temperature processing such as for front emitter diffusion process to form a p-n junction. To date, PERC solar cells reach PCE up to 23% [35].

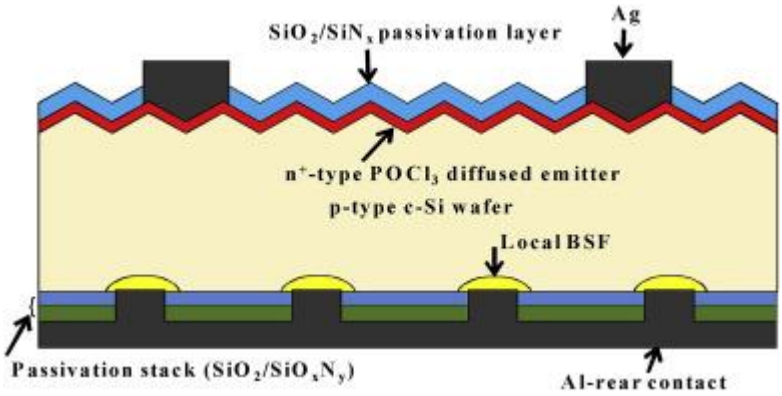

Figure 2.3 Schematic diagram of PERC solar cell [34].

The high-temperature processing leads to formations of defects in the solar cells. Besides, it incurs a high cost in the process due to the high temperature requirement. As a result, there is a need to change the device architecture such as switching to a cell technology like heterojunction with intrinsic thin layer (HIT/HJT) [36]. The HIT cells adopt a heterojunction approach to realizing a solar cell by using amorphous silicon (a-Si) on c-Si absorber material. These cells have attracted attention of photovoltaic research community due to its low processing temperature (up to 200°C), superior passivation quality, and relatively high efficiencies.

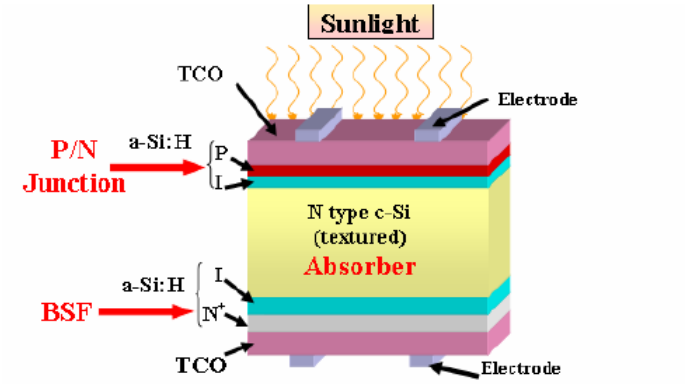

Figure 2.4 Schematic diagram of heterojunction c-Si solar cell [37].

The heterojunction such as shown in Figure 2.4 approach arises from band engineering and relative band-alignment of materials. a-Si possesses a larger band gap than c-Si and this results in formation of a natural valence band offset. From reported studies on a-Si and HIT cells, based on the electron affinity value of 3.93±0.07 eV below vacuum, the conduction band and valence band offsets would be 0.1 eV and 0.4 eV respectively [38]. The HIT cell device architecture implements an intrinsic amorphous silicon layer (i-a-Si) on the front which is responsible for achieving superior passivation and very low surface recombination velocities.

On the front of the cell, on top of the i-a-Si layer is the p^+ doped hydrogenated a-Si layer while the rear side implements a n^+ hydrogenated a-Si layer. The doped a-Si layers provide the necessary band alignment, electric field, and aids charge transport. This cell architecture attains maximum PCE of 25.6% with open circuit voltages in the range of 750 mV [39]. In HIT cells, the conduction and valence band offsets behave as carrier selective layers preventing the flow of electrons and holes to travel towards p-type and n-type layers respectively, whereas the valence and conduction band continuities help a smooth diffusion and tunnelling of the holes and electrons towards the p-type and n-type layers, respectively.

Despite the high efficiencies and superior passivation quality advantages, HIT cell manufacturing is quite complex and expensive. The bigger concern for HIT cells is absorption in ITO and p-layer as well which has gained attention recently [40]. In addition, the HIT process (adopted by market leader Panasonic) requires low temperature fired silver [41]. The low temperature means that the metal retains considerable porosity and is therefore not as conductive as would be conventional,

high temperature firing silver inks. Consequently, the amount of silver used has to be increased, which is a big cost factor.

2.3.1 Silicon as Semiconductor Material

Semiconductor materials can be found from different groups in the periodic table. However, they share similar traits. The properties of semiconductor materials are related with their atomic number which varies from each group. For examples, such as in the group IV or combination of group III and group V (III-V semiconductors). Thanks to this variation, the researchers are able to take the opportunity to refine the design and to study the optimum material for PV devices.

Silicon (group IV) is used commonly in solar cell technology [42]. Silicon (27.2%) is the most abundant element in the earth's crust after oxygen (45.5%), and together, these 2 elements comprise 4 out of every 5 atoms available near the surface of the globe. It shows the abundance of Si on Earth [43].

In general, Si is produced by the thermal reduction of SiO_2 (crushed quartz) in presence of carbon in an arc furnace. After the thermal reduction process, the molten Si and CO_2 gas are formed and collected in a tank. The produced metallurgical grade Si (MG-Si) contains 1-2% impurity. Over 2 million tons of MG-Si are produced annually, and it is largely used in metallurgical industries. MG-Si is useful in many industries for semiconducting devices but not in the solar cell industry [44]. For advanced solar cells, the purity of Si must be ~99.9999% which is also referred as 6N and this purity of Si is called solar grade Si (SoG-Si). MG-Si is further purified to produce SoG-Si using the Siemen process and other purification processes [45].

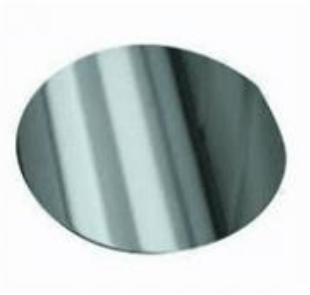

Figure 2.5 Mono c-Si wafer used in laboratory to fabricate solar cells.

Pure solar grade (SoG) Si chunks are further used to make mono or single-crystalline and poly or multicrystalline forms of Si. Single-crystalline Si or monocrystalline Si (mono c-Si) has all atoms arranged in the same crystal orientation throughout the material. Figure 2.5 shows the c-Si wafer that is usually used in labs for research and development activities. For solar cells, (100) orientation is preferred as it can be easily textured to reduce the surface reflection [46]. Multicrystalline Si (multi c-Si) has several grain boundaries in between the crystals of Si material with different orientations, unlike the monocrystalline substrate. Mono c-Si materials have a higher minority carrier lifetime compared to multi c-Si and hence higher solar cell efficiencies for a given solar cell technology [47].

2.3.2 Operation of Silicon Solar Cell

A solar cell is an electronic device that converts sunlight to electricity. Sunlight that shines on the solar cell produces current (I) and voltage (V) and hence power (P) from the cell. When the light enters the solar cell as shown in Figure 2.6, the operation of solar cell begins. The operation of silicon solar cells basically has 4 main steps, which starts with the creation of light-generated carriers (in the form of electron-hole pairs).

Next is the collection of light generated carriers to generate current (I). Third is the generation of large voltage (V) across solar cells. Finally, the dissipation of power (P) in external load [48]. The emitter is drawn thinner compared to the base (c-Si) to keep depletion region near to the surface of the device where the incident light is strongly absorbed [49]. The base is usually thicker to enable complete light absorption [50].

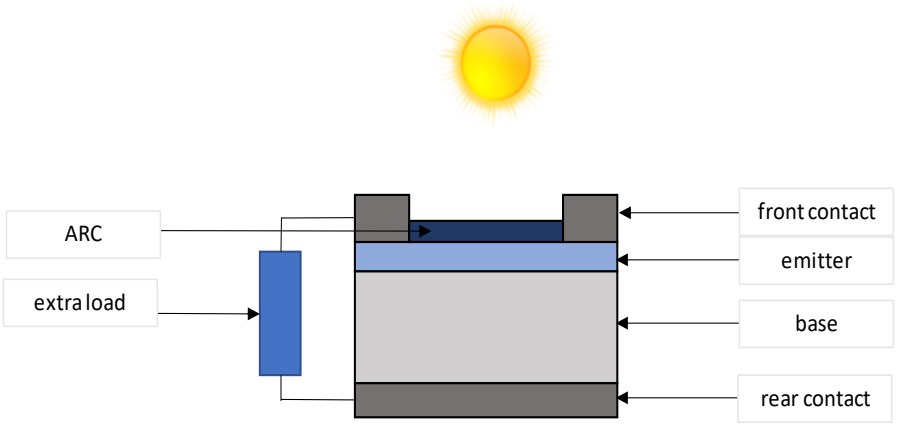

Figure 2.6 Schematic diagram of a solar cell.

P-n junction is compulsory to a solar cell operation. It is because the p-n junction plays an important role in generating electricity from the sunlight. P-n junction is located between emitter and base as illustrated in Figure 2.6. N-type silicon is doped with negatively charged dopants which contribute free electrons [51]. The free electrons are distributed equally throughout the volume of the n-type silicon crystal. P-type silicon is doped with positively charged dopants which contribute holes [51]. Therefore, the holes are distributed equally throughout the p-type silicon crystal. The charges in both n-type and p-type silicon are depicted in Figure 2.7. Once both the n-type and p-type silicon are combined, a p-n junction is formed, as can be seen in Figure 2.8.

Figure 2.7 The n-type silicon and p-type silicon.

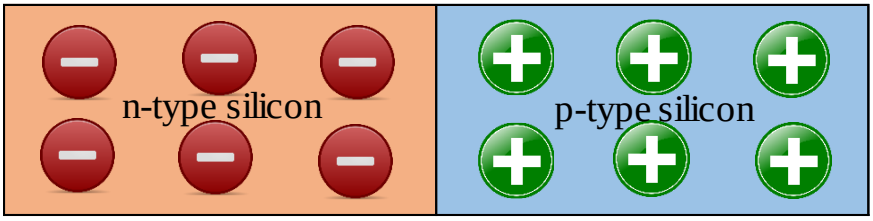

Figure 2.8 The combination of p-type and n-type silicon as a p-n junction.

When the p-n junction is formed, the electrons from n-type silicon start to diffuse into p-type side due to the presence of concentration gradient at the junction. The same process happens to the holes in the p-type silicon, but in the opposite direction. The diffusion of the electrons and holes into the opposite directions leads to formation of built-in electric field at the p-n junction which blocks further diffusion of both carriers into the opposite regions. A space charge region or depletion region is formed near the junction region, which contains fixed charges with opposite polarities to the electrons and holes in the original n-type and p-type silicon. At this point, thermal equilibrium condition is reached, as illustrated in Figure 2.9.

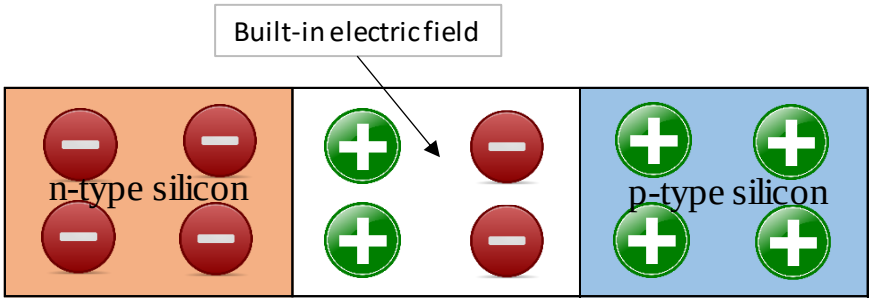

Figure 2.9 The p-n junction at thermal equilibrium.

2.4 Light Trapping in Solar Cell

According to Green, who studied the optical properties of intrinsic silicon and had tabulated the absorption coefficient as a function of wavelength, indicated that silicon is a poor light absorber especially at longer wavelength (approaching near infrared) as shown in Figure 2.10 (a) [15]. Approximately 1 cm thick silicon wafer is needed to fully absorb light energy at wavelength near infrared (IR). The reflection of silicon is very high especially in visible region based on the value of real refractive index and extinction coefficient as shown in Figure 2.10 (b) [15].

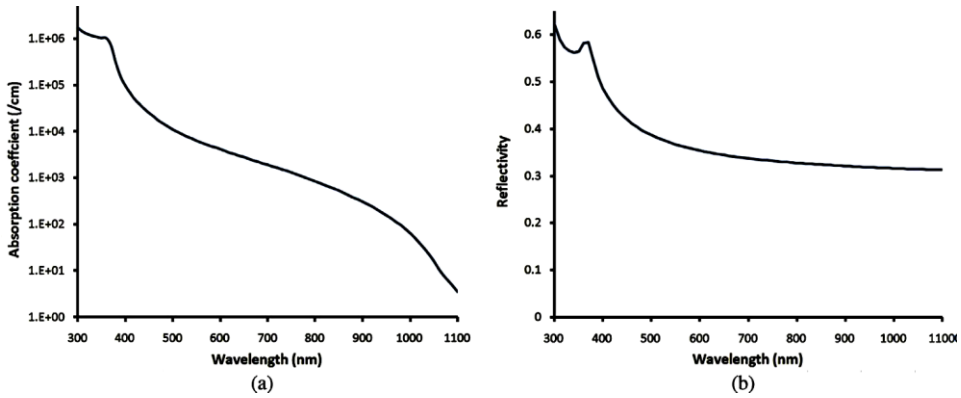

Figure 2.10 (a) Absorption coefficient of flat c-Si wafer at 300 K. (b) Reflectivity of flat c-Si wafer at 300 K [15].

About 30-40% of incident light is lost due to reflection. It is obvious in short wavelength range or to be precise in blue wavelength. Therefore, optical loss due to low absorption at long wavelength and high reflection at short wavelength causes minimum light to be converted to electricity. Thus, techniques that can prevent both limitations need to be incorporated. One of them is by front surface texturing.

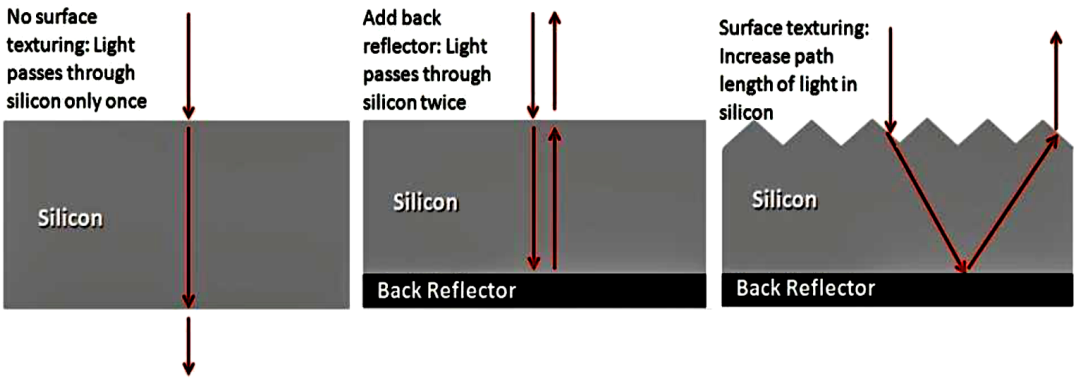

Figure 2.11 The textured silicon able to increase the optical path length [52].

Solar cell that has light trapping ability exhibits optical path length several times longer than its actual device thickness. Therefore, the efficiency to absorb light ray is still optimum although the thickness of silicon is reduced. Optical path length means the distance of unabsorbed photon travel within the device before it escapes [53]. Light trapping is achieved by altering the angle of incident light on the surface. Light trapping able to increase the optical path length can be produced by texturing the surface of silicon. It is shown in Figure 2.11. The textured surface not only able to trap light but it able to reduce the light reflection. The angle which light is refracted into silicon is obeys the Snell's Law [54];

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 \quad (2.1)$$

Where:

n_1 – refractive index of medium 1

n_2 – refractive index of medium 2

θ_1 – angle of incident ray

θ_2 – angle of refracted ray

2.5 Surface Texturing of Silicon with Wet Chemical Etching

Wet chemical etching is usually used in solar cell production for silicon texturization. The textured geometry depends on the isotropy or anisotropy of etch. The example of an anisotropic etchant for silicon is KOH and NaOH (alkaline etchants) [55]. Anisotropic etchants etch at particular crystallographic orientations with different rates. While isotropic etchant is usually from acidic etchants which is HF, HNO_3 and others [56]. Contrast from anisotropic, isotropic etchant etches all orientations with similar rates/characteristics. Thus, the textured silicon surface alters the effectiveness of reflection reduction and light trapping in c-Si wafer.

Wet chemical etching is used in c-Si cell processing for two reasons. The first one is to remove the sawing damage from the wafers cut from the ingot. Next is the texturization of c-Si surface for light-trapping. The formation of pyramidal textures on silicon wafer due to alkali hydroxides such as KOH and NaOH [57]. Alcohol like ethyl glycol or IPA are routinely used in texturing process [58]. The reasons of the alcohol usage are to improve the smoothness of the surface plane as well as to ensure the etch

uniformity [59]. There are also several organic and inorganic alkaline solution which able for anisotropic pyramidal texturing such as, EDP (ethylenediamine ($NH_2(CH_2)_2NH_2$), pyrocatechol ($C_6H_4(OH)_2$) and ammonium hydroxide NH_4OH [60].

The usage of alkaline etching to form pyramidal texturization of <100> oriented mono c-Si cells has been established for a long time [61]. The pyramids on <100> are formed due to the usage of anisotropy of the alkaline etchants. One of the properties of this etchant is able to etch in particular crystallographic direction in the silicon so that the other direction will have slow etching rate. In this case (<100> silicon wafer) the etching of <100> silicon wafer is produced either vertical (<100>) walls or sloping (<110> or <111>) walls which are 45^o or 54^o respectively. <100> or <110> walls are achieved by aligning the pattern edges to 100 direction, 45^o from the prime wafer flat. To achieve <111> walls the pattern edges must be in 110 direction [62]. The selection of wall depends on their relative etch rates R_{100} and R_{110}, with the plane forming a sidewall always being the one with the slowest etch rate aligned to the mask edge [63]. It has been reported that in pure aqueous KOH and TMAH solutions, vertical walls form ($R_{100} < R_{110}$), whereas in solutions with isopropyl alcohol (IPA) added, the {110} walls form ($R_{110} < R_{100}$) [64]. The anisotropy of TMAH solutions changes in the same way with addition of IPA.

The addition of IPA plays no active part in the chemical reaction, but at most KOH or NaOH concentrations it has the effect of reducing the etch rates of the high-order crystal planes (and so reversing the order of R_{110} and R_{100}). However, in a detailed study of etch rates [65], a different behaviour was observed at high concentrations, R_{100} remaining the slowest plane, even with IPA added. Vertical walls with KOH +

IPA have only been reported and were considered to be not useful due to slow etch rates and unreliability [66].

The surface of silicon is etched by these following ways. The silicon surface is hydrogen terminated during alkaline etching [56]. It has been observed after treatment in HF solution. However, there are some disagreements about the active etching species. OH^- is claimed to be active etching species as shown in Equation 2.2 – 2.5. It has been studied by Raman spectroscopy where the intensity of OH^- line gradually decreases during etching. However, there are some opinions that make water an active species as shown in Equation 2.2. OH^- acting to catalyse the etching reaction. It is agreed that the active species hydrolyses the (hydrogen terminated) surface silicon atom to become a hydroxyl-terminated silicon atom or (ionized) complex. This is generally assumed to be the rate-determining step. Therefore, the water or OH^- attacks the back-bonds of the silicon atom to form a silicate which can leave the surface, whereby it is generally accepted that the reaction products include a silicon hydroxide complex, e.g. $Si(OH)_4$ or $Si(OH)_2O_2^-$, with hydrogen gas released during the etch process. Investigations in using nuclear magnetic resonance showed that the lower the concentration of alkaline solution (NaOH), the higher the level of polymerisation of this complex. In summary, the proposed overall reaction where water is assumed to be the active species.

$$Si + 4H_20 \rightarrow Si(OH)_4 \text{ (or other complex)} + 2H_2 \quad (2.2)$$

A suggested (electrochemical) reaction with OH^- as the active species [15] is:

$$Si + 4OH^- \rightarrow Si(OH)_4 \quad (2.3)$$

$$Si(OH)_4 + 2OH^- \rightarrow SiO_2(OH)_2^- + 2H_20 \quad (2.4)$$

$$4H_20 + 4e^- \rightarrow 4OH^- + 2H_2 \quad (2.5)$$

In order to absorb more incident light, texturing is must to any c-Si solar cell. By adding textured on the surface of c-Si, the roughness is presence. This roughness is necessary to reduce reflection. Thus, increase the absorption of incident light. It happened due to the incident light is not reflected back to the air once it strikes the surface however it bounces among the textured c-Si surface. Therefore, it increases the optical pathlength. The reason is that surface texturing induced scattering effect toward the incident light. The theoretical size of a pyramid is 5-8 μm with the angle of 50-55^o [67].

2.6 PEDOT:PSS as Conductive Polymer

Organic semiconductors are unique class of materials because they offer several key advantages over inorganic semiconductors. They offer a wide range of materials from small molecules to polymers, easy processing via solution-based processing techniques like spin-coating, dip-coating, doctor blading, spray coating, ink jet printing and tuneable work functions to adapt to the heterojunction structure [68]. There are many examples of organic semiconductors such as copper phthalocyanine (CuPc), polyethylene (PE) polyacetylene (PA), poly(3,4-ethylenedioxythiophene) :poly(styrenesulfonate) (PEDOT:PSS) and so on [69]–[71].

In most applications, PEDOT:PSS can be possess metal-like properties although they are intrinsically conducting polymers. Amongst organic semiconductors, PEDOT:PSS is a very well-studied and popular choice with varied applications in the capacitors,

antistatic coatings, electroluminescent lamps, organic light emitting diodes, organic solar cells, and transistors to name a few. The wide range of applications originate due to superior properties of PEDOT:PSS like [72]:

1. Conductivities of up to 1000 S/cm
2. Water-based non-toxic dispersion and vast variety of solution-based deposition methods, such as spin-coating, spray-coating, dip-coating, slot-die-coating, screen-printing, and ink-jetting
3. Thermal stability of up to 200°C
4. Transparency over 80% in the visible wavelength spectrum
5. Adjustable work function

Fundamentally, PEDOT:PSS is a macromolecular salt where oxidized PEDOT is the cation and the PSS is deprotonated as the anion [73]. In this form, the PSS acts as a p-type doping counter ion which allows hole mobility along the PEDOT conjugated backbone and promotes the dispersion of the complex in polar solvents such as water due to the micelle-like morphology that the complex develops. In solution the PSS forms the outer shell and PEDOT is in the middle of the micelle like structure as can be seen in the Figure 2.12.

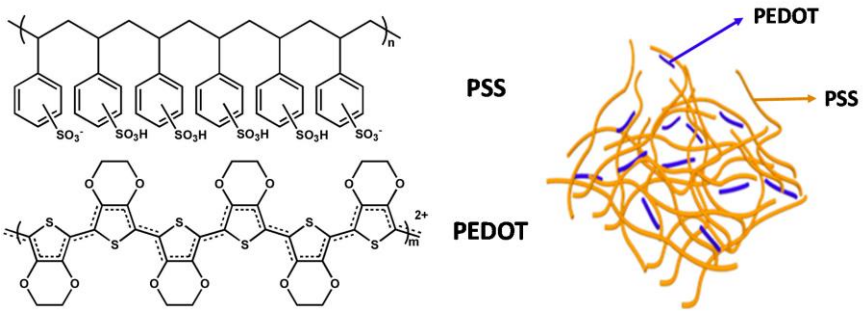

Figure 2.12 The chemical structure and schematic core-shell structure of poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate (PEDOT:PSS) [73].

PEDOT:PSS is usually available as an aqueous solution and obtained from the Baytron P process which involves polymerizing EDOT monomers using PSS as the electrolyte and $Na_2S_2O_8$ the oxidizing agent [74] From an energy level perspective, delocalized bonding of π-symmetry orbitals is important and responsible for the various levels [75]. Hence, for such materials there are series of energy levels rather than valence or conduction bands in semiconductors.

The highest occupied molecular orbital is referred as HOMO and lowest unoccupied molecular orbital as LUMO [72]. The HOMO level in organic semiconductors is essentially the valence band maximum while LUMO is equivalent to the conduction band minimum. Unlike a metallic conductor where the work function can be considered an intrinsic property of the material, the work function of PEDOT:PSS is altered based on the position of the fermi level with respect to the valence band which in turn depends on the carrier, doping, concentration and is similar to the fermi level in inorganic semiconductors [76].

PEDOT:PSS can also be treated as a degenerately doped p-type semiconductor due to the abundance of holes and the doping concentration can be as high as $3x10^{20}$ cm^{-3}