MULTISTAGE POWER AMPLIFIER IN 180nm CMOS TECHNOLOGY WITH INTEGRATED PASSIVE LINEARIZER FOR IEEE 802.15 APPLICATION

by

PREMMILAAH GUNASEGARAN

Thesis submitted in fulfilment of the requirements
for the degree of
Master of Science

October 2018

ACKNOWLEDGEMENT

First and above all, I thank the Almighty God for his infinite blessings.

Next, I would like to express my gratitude to my academic supervisor, Dr. Jagadheswaran Rajendran from Collaborative Microelectronic design Excellence Centre (CEDEC), Universiti Sains Malaysia (USM) who has provided the guidance and assisted me to obtain knowledge in this field, at the same time, helping me to promptly complete my master research studies.

I am very grateful to my co-supervisor, Assoc. Prof. Dr. Ir. Harikrishnan Ramiah for his great support and guidance throughout this study.

As part of my research project, I had the opportunity to spend time in Collaborative Microelectronic Design Excellence Center (CEDEC) Penang to conduct my research. I would like to thank Mr. Ruhaifi Abdullah Zawawi, Mr. Mohd Shukri and Mr. Hasnirol from CEDEC for their support and guidance throughout my project. They had provided me with numerous brilliant idea and guidance in completing my master research.

I would like to express my gratitude to Talent Corporation for their financial support.

Last but not least, I would also like to take this opportunity to thank all my family members especially to my mother, my father and my siblings whose unlimited love and support has made this effort possible.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ACLR	Adjacent channel leakage ratio
ACPR	Adjacent channel power ration
AM-AM	Amplitude Modulation to amplitude modulation
AM-PM	Amplitude modulation to phase modulation
APD	Analogue Pre-Distorter
BLE	Bluetooth Low Energy
CMOS	Complementary metal oxide semiconductor
DPD	Digital Pre-Distorter
DSP	Digital system processing
EVM	Error vector magnitude
GaAS	Gallium arsenide
HD	Harmonic distortion
IF	Intermediate frequency
IMD3	3rd order intermodulation distortion
IoT	Internet of things
LINC	Linear amplification with nonlinear components
OIP3	3rd order intercept point
PA	Power amplifier
PAE	Power added efficiency
PAR	Peak to average ratio
PHEMT	Pseudomorphic high electron mobility transistor
Pout	Output Power
RF	Radio frequency

VCO	Voltage controlled oscillator
Wi-Fi	Wireless Fidelity
WiMAX	Worldwide interoperability for microwave access
WLAN	Wireless local area network

PENGUAT KUASA PELBAGAI PERINGKAT DALAM TEKNOLOGI CMOS 180nm DENGAN MENGINTEGERASIKAN LINEARIZER PASIF UNTUK APLIKASI IEEE 802.15

ABSTRAK

Permintaan tinggi terhadap aplikasi standard komunikasi tanpa wayar telah meningkat dengan perkembangan yang pesat terhadap kadar data yang tinggi dan ini memberikan cabaran yang besar kepada rekabentuk penguat kuasa RF CMOS. Secara umumnya, sesebuah penguat kuasa haruslah berkemampuan beroperasi dengan cekap di samping mengekalkan lineariti yang ketat. Dalam projek ini, sebuah penguat kuasa linear pelbagai peringkat CMOS untuk aplikasi BLE telah direka dan dilaksanakan. Penguat kuasa CMOS bersaiz 1.5mm x 1.5mm telah difabrikasi menggunakan teknologi 180nm. Penguat kuasa ini terdiri daripada dua peringkat iaitu peringkat pemacu dan utama. Peringkat utama ini direka menggunakan konfigurasi "Class deep AB" untuk mengekalkan lineariti tanpa memberi kesan kepada kecekapan penguat kuasa tersebut. Linearizer pasif yang baru telah direka dan disatukan pada get utama peringkat penguat bagi meningkat lineariti. Ukuran puncak OIP3 sebanyak 19.67 dBm telah dicapai. Rekaan sepoadan puncak ini telah mencapai kecekapan (PAE) sebanyak 39.1% dengan keluaran maksimum linearnya 35%. Dengan masukan dan keluaran kehilangan kurang daripada -10dB, keuntungan kuasa penguat yang maksimum boleh diukur mencapai lebih daripada 20dB dengan mempamerkan ciri-ciri yang sangat stabil dari arus terus (DC) hingga 10GHz. Seni bina yang dicadangkan telah memberikan satu penyelesaian dalam meningkatkan keluaran kuasa linear bagi penguat kuasa CMOS kuasa rendah tanpa memberi kesan terhadap parameter-parameter yang penting.

MULTISTAGE POWER AMPLIFIER IN 180nm CMOS TECHNOLOGY WITH INTEGRATED PASSIVE LINEARIZER FOR IEEE 802.15 APPLICATION

ABSTRACT

As wireless communication standard continues to evolve accommodating the demand of high data rate operation, the design of RF CMOS power amplifier (PA) becomes ever challenging. PAs are required to operate more efficiently while maintaining stringent linearity requirement. In this work, the low power linear multistage CMOS power amplifier for BLE application is designed and implemented. The 1.5mm x 1.5mm CMOS power amplifier is fabricated in an 180nm technology. The power amplifier consists of two stages which is the driver and main stage. The main stage is designed in Class deep AB configuration in order to preserve the linearity without sacrificing the efficiency of the power amplifier. A novel passive lineariser is designed and integrated at the gate of the main amplifier stage to improve the linearity. The peak OIP3 of 19.67 dBm is achieved in measurement. The corresponding peak power added efficiency (PAE) of 39.1% achieved and at maximum linear output power 35% of PAE is achieved. With a respective input and output return loss of less than -10dB, the power amplifiers maximum power gain measured to be more than 20dB while exhibiting an unconditional stability characteristic from DC up to 10GHz. The proposed architecture serves to be a good solution to improve the linear output power of low power CMOS power amplifier without sacrificing other crucial parameters.

CHAPTER ONE

INTRODUCTION

1.1 Introduction

The wireless communication system has grown exponentially to realize higher data rate transmission scheme with low power consumption. Progress in the maturation of wireless communication improves the industrial turnover in late years. Improvement territories include Wi-Fi, Bluetooth, radar, communication and WLAN that possibilities a higher data rate exchange resourcefully. Establishment of communication demands the durability, integrated circuits and more serious performances of wireless communication system. As of late earlier, communication has been just with voice. Today the data, communication accomplished to break even significantly to interface with the world (Gopalrao & Yadav, 2016).

Bluetooth contraptions for Industrial, Scientific and Medical (ISM) band operate in the 2.4-2.483 GHz. There are basically 3 power classes of Bluetooth based on transmission distance. They are Class 1, Class 2 and Class 3 correspondingly as shown in Table 1.1. Normally, the Bluetooth power amplifier is running on a low power model, thus the production power of Class 1 power amplifier must controllable down to 4 dB or less to deliver the power (Vathulya, Sowlati, & Leenaerts, 2001).

Table 1.1: Power classes of Bluetooth

Class	*Power (dBm)*	*Power (mW)*	*Distance (m)*
1	20	100	100
2	4	2.5	10
3	0	1	1

On that point are various communication contraptions in which the radio frequency signals exchange information between its input and output levels. To realize this, an ideal approach to transmit and receive the RF signals is required. Frequently, the bottleneck to accomplish this objective is the power amplifier which consumes more energy and subject to non-linear operation. Figure 1 exemplifies the location of the PA in the BLE transmitter (Gunasegaran, Rajendran, & Ramiah, 2017).

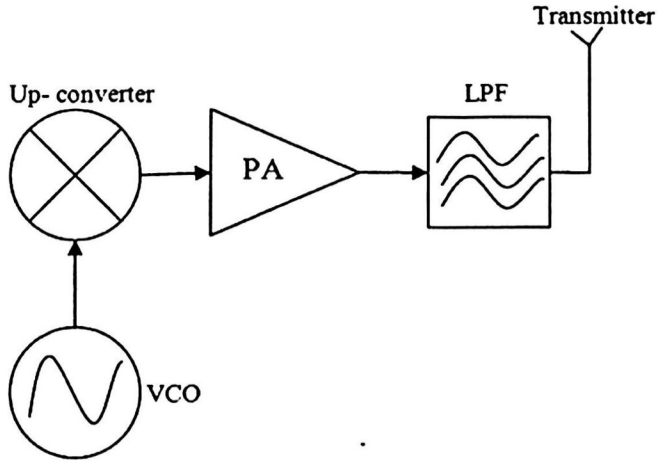


Figure 1.1: Block diagram of BLE transmitter(Gunasegaran et al., 2017)

To meet desires for the low price cost transceivers, CMOS Power Amplifier (PAs) have been widely tested. Nevertheless, the high peak to average power ratio signals in modern wireless communication system poses great challenge for CMOS PA implementation, due to the high trade-off between linearity and efficiency as contrasted to GaAs PAs (Koo, Na, & Hong, 2012) (S. Jin et al., 2013) (Kaymaksut & Reynaert, 2015) and (Oishi et al., 2014).

Maximum power transfer can be achieved by matching impedances between input and driver stage, between power stage and output and the inter-stage between driver and power stage. The PA must have high reverse isolation and they must be linear. As power amplifier are extensively utilized as a part of transceiver it's perfect to hold a

less power consuming device and having less active chip size at the applicable frequency, accomplishing desired gain, power added efficiency (PAE) and return losses (Indumathi & Keerthana, 2014).

However, the commercialization of CMOS PAs has not been effectively achieved because of the intrinsic drawbacks of typical CMOS processes. There are low-quality factor (Q), lossy substrate of passive structures, low breakdown voltage, and low trans-conductance of active devices. Hence, numerous endeavours, including the linearity enhancement techniques, and efficiency enhancement techniques, have focused on conquering the drawbacks of CMOS technology for PA designs (Jeong, Koo, Joo, & Hong, 2015).

To recognise high-efficiency RF power amplifier in standard CMOS, technology constraint must be understood (Gupta & Allstot, 1999). Therefore, much effort is as yet continuous to enhance efficiency, output power and operating frequency before a conclusive objective of full CMOS, single-chip radio, can be essentially accomplished (Gupta, Ballweber, & Allstot, 2001).

1.2 Problem Statement

As we know, Bluetooth power amplifier is heavily dependent on battery energy. Therefore, to achieve low power consumption operating point, it is biased at very low current. However, biasing at low current degrades the linearity of the PA severely. For BLE application, the linearity is crucial parameter, in order to preserve the quality of transmitted data. Hence, in this project, a linearization scheme is introduced to mitigate this effect. Active linearizer expends more power and subject

to process variation that bears on the non-linear signal cancellation (Gunasegaran et al., 2017). Hence to overcome this, passive linearizer is intended as a solution.

1.3 Research Objectives

The aim of this work is to design a linear low power CMOS PA proposed for BLE application.

The main objectives of this project are to design power amplifier

1. To design a power amplifier achieving more than 20dB gain from 2.4-2.5 GHz.
2. To achieve maximum linear output power of 10 dBm at centre frequency 2.45 GHz with drain voltage less than 2V.
3. To achieve minimum OIP3 of 15 dBm across the linear output power to preserve the quality of transmitted data.

1.4 Contributions of the Research

The challenges of CMOS RF PAs have just been portrayed in the previous section. From an absolutely performance-oriented viewpoint, CMOS technologies still lacking as compared to other technologies. Nevertheless, the integrability and adaptability of CMOS to achieve a single chip solution for wireless communications as the motivation for continuous improvement through circuit innovation. Moreover, CMOS advances would be the least expensive among different applicants, for example, III-V HBT, III-V PHEMT, SiGe HBT, and Si-MOSFET technologies. Consequently, it appears to be unavoidable that the both customers and manufacturers will pick CMOS technologies over all others as represented in Figure 1.2 (Bennett et al., 2005).

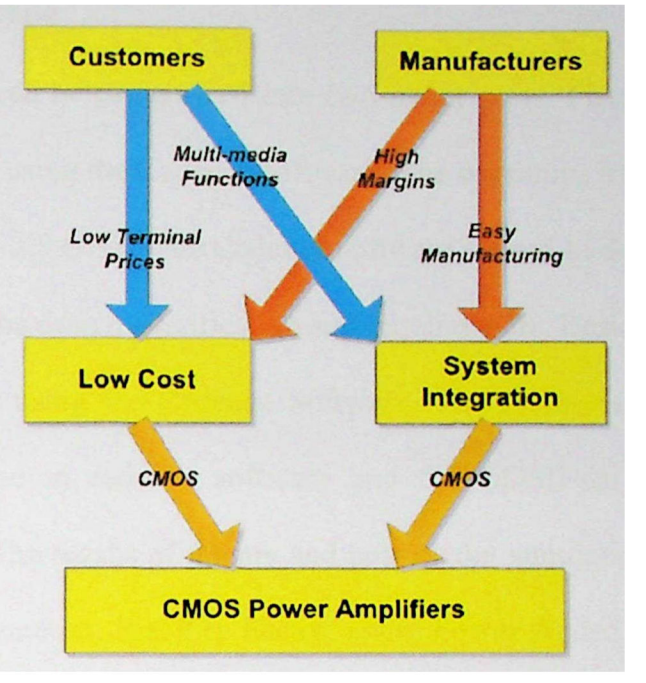


Figure 1.2: Benefits of CMOS PAs in wireless market

Now, the atmosphere is perfect for a RF CMOS PA in the wireless market. One warning, yet, CMOS is the way to accomplish similar performances utilizing CMOS in realizing a PA. Hence, in serious reflection of the implementation of CMOS RF PAs, this research will present and converse about different endeavours at determining good PA solutions for their commercial application in wireless market.

Efficiency and linearity are two important figures of merits to protect the battery life and to preserve the transmitted data. The first contribution for this work is to reduce the trade-off between the linearity and efficiency of the CMOS PA that is suitable for BLE Application. The second contribution is to design low power multistage CMOS PA with high power gain. The BLE operates at low power where the maximum desired current is 15mA. The third contribution is to achieve low power consumption at maximum linear output power of 12dBm, 8dB more than BLE specification.

1.5 Research Scope

This project can be categorized into two major parts. First part is designing linear low power PA using the Cadence software. The operating frequency of the PA is limited from 2.4 to 2.5 GHz. The Cadence software is used to design and simulate the PA according to the design specification and requirements. Besides that, the layout design also done by using the Cadence Software. The pre-layout and post-layout simulation were done in cadence software and the GDSII is streamed out for fabrication process. The results of the pre and post layout simulation will be verified in terms of its S-parameters, Stability Factor, Gain, Power Added Efficiency (PAE) and 3rd order Intercept Point (OIP3). Second part is on the measurement on the fabricated chip. The best given results from simulation will be fabricated. The fabricated chip will be measured to verify the post-layout simulation result.

1.6 Thesis Outline

The thesis is organized into five chapters. The first chapter discusses the background of the PA development particularly in the wireless system with the problem statement, project objective, thesis contribution and the scope of the project is highlighted.

Chapter 2 reviews the research and studies conducted previously on the high efficiency and linear power amplifier including the design parameters. Meanwhile the crucial parameters of PA are explained. Furthermore, the Linearization techniques were explained in details and recent work comparison were discussed.

Chapter 3 describes the work flow of the design by the flowchart. Furthermore, the design methodology is explained with theoretical analysis. On top of this, the measurement methodology is explained in detailed.

Chapter 4 encloses the analysis of the design which contains simulation and the measurement results. The corner and temperature analysis are also conducted. The layout is also shown. Meanwhile the comparison between simulation and measurement results is also been discussed.

Finally, the chapter 5 draws the conclusion of the project and the proposal for future work.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

In this chapter, the theory of non-linearity of power amplifiers are presented. A review of various RF CMOS PA linearization techniques and summary of recently published research works by other are discussed as well.

2.2 Power Amplifier parameters

The most crucial parameters in designing power amplifiers are discussed and explained further in this section.

2.2.1 Output Power

Output power is the most vital design aspect of a PA. In one sense, if the PA generates low output power, it loses its individuality, making it hard to specify. When a supply voltage is passed as a fixed value, only the amount of current that provides a required output power can be a design parameter. Assuming a normal output load with resistance, R, the PA in Figure 2.1 has an output power of the following expression:

$$P_{out} = \frac{\left(\frac{V_{pp}}{2}\right)^2}{2R} \tag{2.1}$$

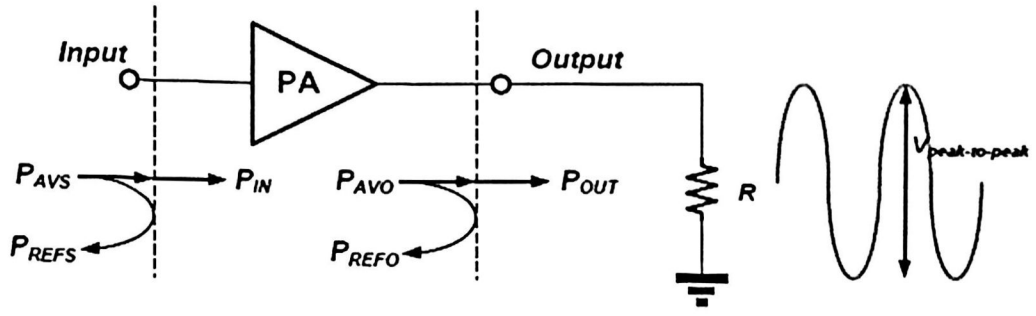


Figure 2.1: Defination of output power

2.2.2 Efficiency

In PA design, several similar, however slightly different metrics are employed to characterize the efficiency performance of a PA. Basically, efficiency represents the part of DC power converted to RF power. The most common efficiency definition used are drain efficiency and power added efficiency.

Drain efficiency is the ratio of RF output power to DC input power;

$$\eta = \frac{P_{out}}{P_{dc}} \times 100\% \tag{2.2}$$

where the Pout is the fundamental output power expressed by ½ VdcIout and Pdc is the dc power consumption expressed as VdcIdc.

The power added efficiency (PAE) is a more realistic indicator of the efficiency, performance, as it brings into account the fact that a PA has to be pushed in order to get the output power. The PAE is defined as

$$PAE = \frac{P_{out}-P_{in}}{P_{dc}} \times 100\% \tag{2.3}$$

where *Pin* is the input power, and *Pout* and *Pdc* are the output power and DC supply power, respectively.

PAE generally used to analyse power amplifier when the gain is low.

2.2.3 Gain

In Radio Frequency Integrated Circuit (RFIC) design, the power gain is represented by different definition. The operating gain design method is used to design for maximum linear output power. The approach starts form the desired load impedance and then matches the resultant input impedance. The operating power gain can be represented as;

$$G_P = \frac{Power\ delivered\ to\ the\ load}{Power\ applied\ to\ the\ input\ of\ two\ port}$$

$$= \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{\left(1-\left|\frac{S_{11}-(\Delta)\Gamma_L}{1-S_{22}\Gamma_L}\right|^2\right)|1-S_{22}\Gamma_L|^2} \quad (2.4)$$

where the symbol Δ is the determinant of two port matrix S-matrix

$$|\Delta| = S_{11}.S_{22} - S_{21}.S_{12}$$

2.2.4 Stability

The most important measure that needs to be paid attention is the stability. This is often critical in designing a high gain amplifier. Instability is a concern throughout the whole range of frequencies in which the circuit has gain. In-band instability is avoided by designing an unconditionally stable amplifier (Suárez, Ramirez, & Sancho, 2014). This can be measured by computing the Rollett (K) which has to be more than unity.

The K-Factor can be expressed equally:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2.|S_{21}||S_{12}|} \quad (2.5)$$

where, $|\Delta| = |S_{11}.S_{22} - S_{21}.S_{12}|$

Unconditionally stable when $K>1$, conditionally stable is when the $0<K<1$ and the circuit is unstable is when the $K<1$.

2.2.5 Linearity

RF power amplifiers are inherently non-linear and the main contributor for distortion products in a transceiver chain. This effect the utilization of the spectrum. Typically, non-linearity is caused by the compression behaviours of the power amplifier. Usually, non-linearity is attributed to gain compression and harmonic distortion which results in imperfect reproduction of the amplified signal.

One of the methods used to quantify linear operating zone of a power amplifier is by measuring the 1dB compression point as shown in Figure 2.2.

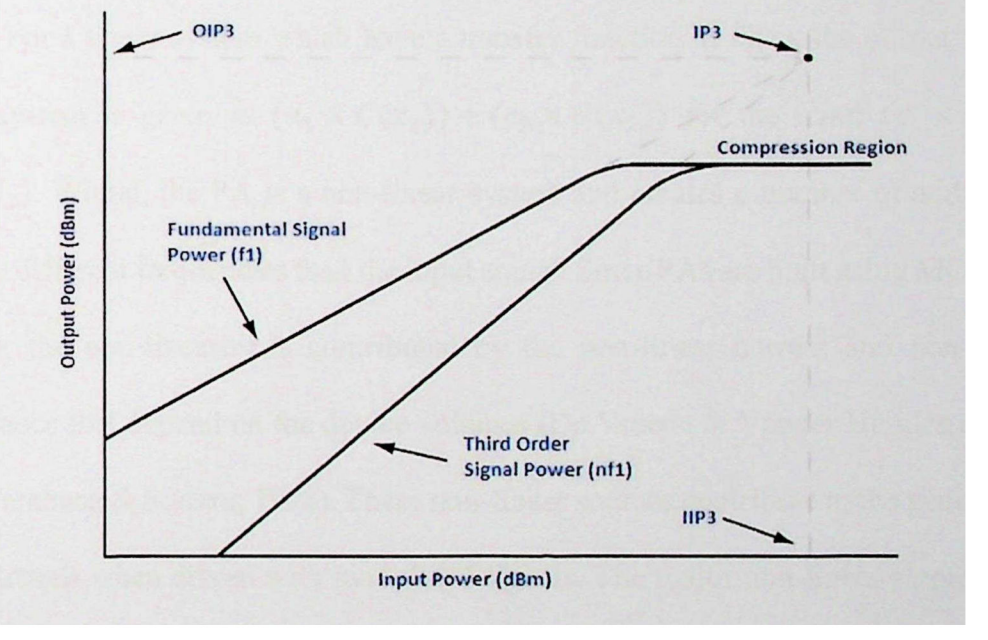


Figure 2.2: 1dB compression point

2.3 Non-Linearity in CMOS PA

As depicted in Figure 2.3, a PA can be modeled with one block in the system level considering x as the input signal and y as the output signal.

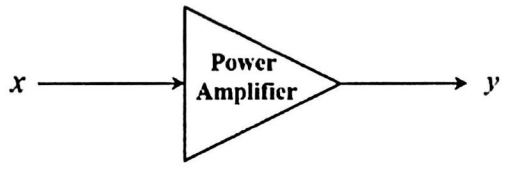


Figure 2.3 Input-output representation of a PA

For a linear system which have a transfer function of G(x), the output of this linear system is given as $(a_1 \times G(x_1)) + (c_2 \times G(x_2))$ for the input $(c_1 \times x_1) + (c_2 \times x_2)$. Withal, the PA is a non-linear system and creates a number of additional terms at different frequencies than the input signal. Since PAs are built using MOSFET devices, the non-linearity is contributed by the non-linear current and non-linear capacitance that depend on the device voltages (De Vreede & Vander Heijden, 2006) and (Wambacq & Sansen, 1998). These non-linear sources contribute to the generation of distortions when driven with modulated signals. The major non-linear elements of a MOSFET device are non-linear trans-conductance (gm), the drain-source capacitance (Cds), and the gate-source capacitance (Cgs) (Aitchison & Mbabele, 2001).

Taylor series expansion is used to approximate the polynomial of a non-linear transfer function. Basically, the terms that are considered are the first-order (gain), second-order (squaring), and third-order (cubing) (Minasian, n.d.). PA non-linearity can be modeled as:

$$V_0(t) = a_0 + a_1 V_i(t) + a_2 V^2{}_i(t) + a_3 V^3{}_i(t) \quad (2.6)$$

2.3.1 Intermodulation Distortion

PAs are usually tested with two tone method where two closely spaced fundamental signal tones are applied to its input. The amplitude is incremented until the third-order cross product generates a signal above the noise floor (Rogers & Plett, 2010), (Razavi, 2012) and (Thomas H.Lee, 2004). Intermodulation distortion (IMD) occurs when the PA is supplied with two tone signals. The third order product are most concern because it appears inside the band of fundamental signal and thus, difficult to be filtered out. Higher order products are usually small to cause any significant distortion and can be easily filtered out (Liu, Xiao, & Li, 2002). Applying a two-tone signal to the PA input yields:

$$V_i(t) = v\,Cos(\omega_1 t) + v\,Cos(\omega_2 t) \tag{2.7}$$

$$V_0(t) = a_0 + a_1 v[Cos(\omega_1 t) + Cos(\omega_2 t)] + a_2 v^2[Cos(\omega_1 t) + Cos(\omega_2 t)]^2 + a_3 v^3[Cos(\omega_1 t) + Cos(\omega_2 t)]^3 \tag{2.8}$$

The resulting harmonics and IMD products are listed in Table 2.1.

Table 2.1: Two tone IMD products up to third order

Order	Terms	a_1V	a_2V	a_3V
Zero	0		1	
First	ω_1	1		9/4
	ω_2	1		9/4
Second	$2\omega_1$		1/2	
	$2\omega_2$		1/2	
	ω_1+/-ω_2		1	
Third	$3\omega_1$			1/4
	$3\omega_2$			1/4
	$2\omega_1$+/-ω_2			3/4
	$2\omega_2$+/-ω_1			3/4

Figure 2.4 shows the output spectrum of a PA that includes the fundamental signals and the spurious products produced by IMD distortion. As can be seen in Figure 2.4, the third order IMD products which appearing at frequencies $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ are the main contributor to the signal distortion since they are located very near to the fundamental tones and its quite difficult to be filtered out. The 3rd order intermodulation distortion (IMD3) for Bluetooth requirement is -20 dBc at 1 MHz and -40 dBc at 3 MHz (Sowlati & Leenaerts, 2003).

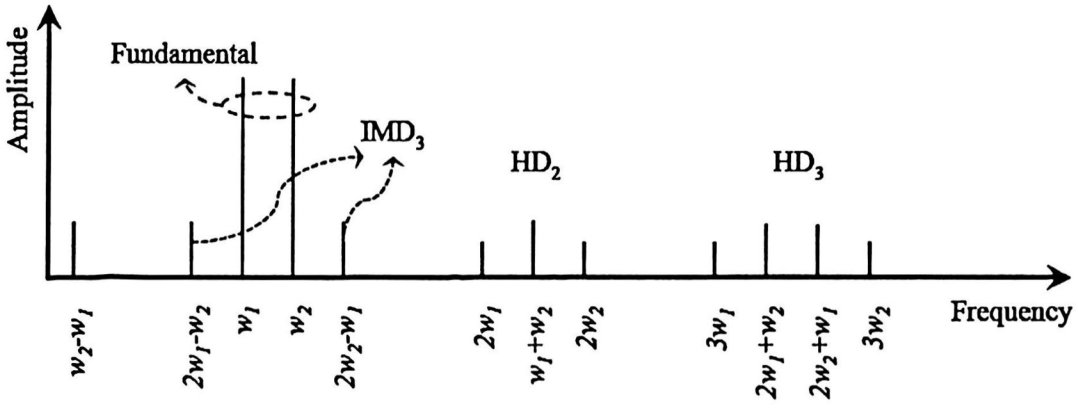


Figure 2.4: IMD products generated by a PA

2.3.2 Amplitude to Amplitude and Amplitude to Phase Modulation

AM-AM (Amplitude to Amplitude) and AM-PM (Amplitude to Phase) are the usual method to characterize the non-linearity of a PA. For ideally linear system response:

$$A_{out} = G_0 A_{in} \tag{2.9}$$

where A_{in} and A_{out} are the input and output amplitudes of the PA respectively, while G_0 is the constant PA linear gain. It is arduous to obtain linear response of G_0 in practical. It is due to the inherent non-linearity of the PA where the output amplitude is compressed for large input amplitude levels. This is briefed by the AM/AM conversion (Katz, 2001). Plus, the shift in phase is a measure of time delay. In ideal

case, this time delay is constant for all amplitude levels. However, because of signal dependent or device dependent non-linear effects, the AM/PM is not constant. Figure 2.5 and 2.6 delineates the AM/AM and AM/PM characteristics of a PA.

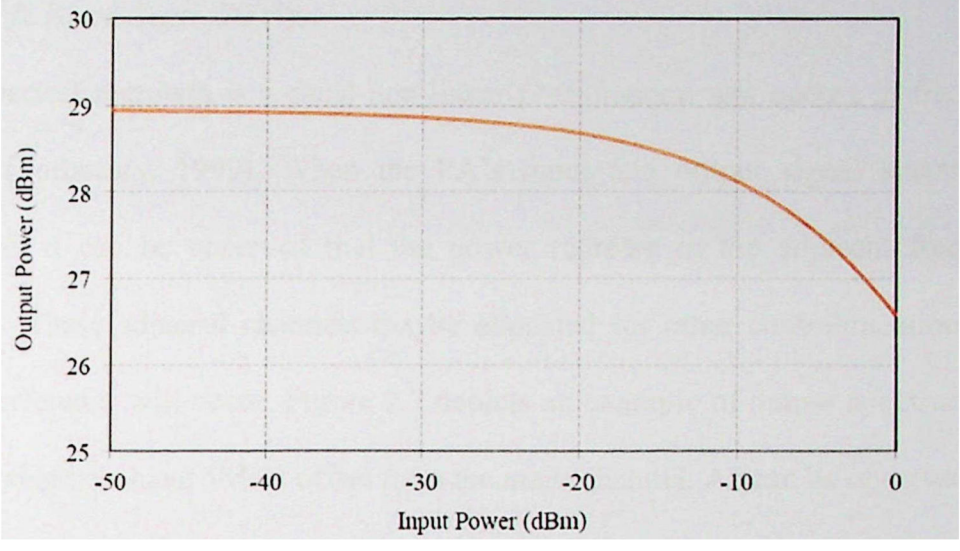


Figure 2.5: AM-AM characteristics

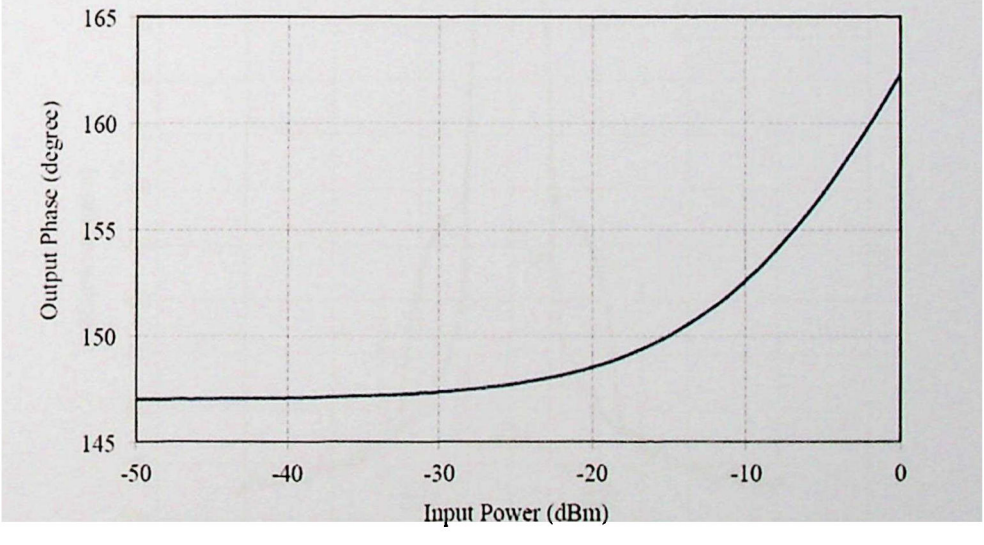


Figure 2.6 AM-PM characteristics

2.3.3 Modulated Signal

Non-linearity causes undesirable distortions such as spectral regrowth and dispersion or rotation of the constellation when operated with modulated input signals (Valkama & Springer, 2010). The typical parameters employed for evaluating this

non-linearity are ACPR (Adjacent Channel Power Ratio) in frequency domain and EVM (Error Vector Magnitude) in time domain (Boulejfen, Harguem, Hammi, Ghannouchi, & Gharsallah, 2010), (Anritsu, 2006) and (Mckinley, Remley, Myslinski, Kenney, & Nauwelaers, 2004).

Spectral regrowth is a usual non-linear phenomenon that occurs in frequency domain (Pothecary, 1999). When the PA's input and output signal spectrum is compared, it can be observed that the power regrows in the adjacent frequency channels. These adjacent channels maybe allocated for other communications, and thus, interference will occur. Figure 2.7 depicts an example of output spectrum. The adjacent channels have 5MHz offset from the main channel. As can be observed from the figure, the output signal spectrum has spectral regrowth which interferes with adjacent channels.

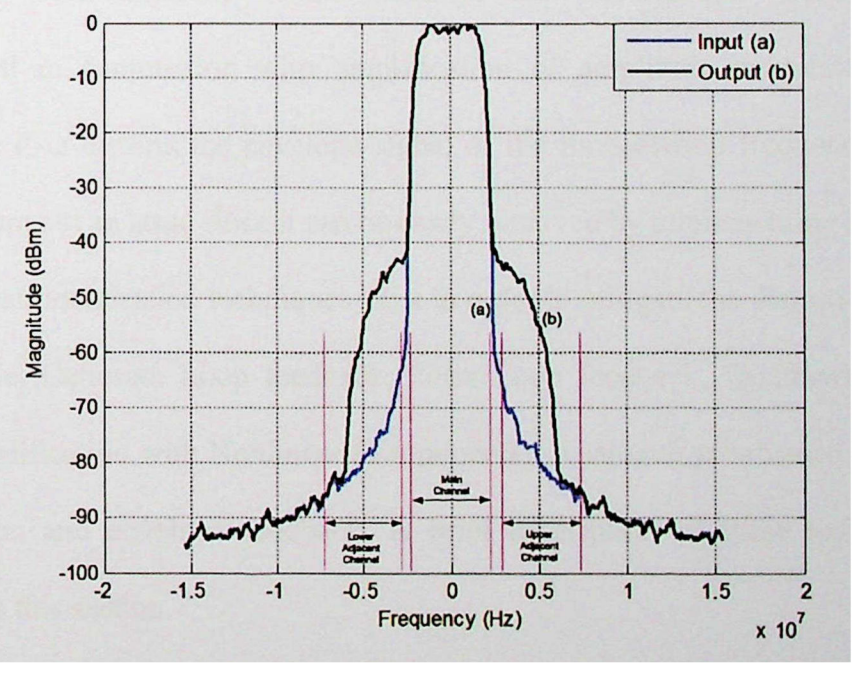


Figure 2.7: Spectral regrowth

The ACPR is used to describe the power ratio between the unwanted distortion in the adjacent channel and the signal in the main channel. The spectral regrowth

appears mainly on the adjacent channels. The ACPR for adjacent channel is described as:

$$ACPR_{adj} = 10\ log \frac{\int S(f)df\ (adj)}{\int S(f)df(main)} \tag{2.10}$$

where *S(f)* represents the power spectral density of the output signal and the term *adj* represents either the first lower or upper channel.

2.4 Linearization Techniques

Modern communication system, which prioritize spectral efficiency and high data rates make the linearity requirements stringent. Highly linear PAs are required in order to fulfill the needs of latest communication standards. Linearization techniques are employed to enhance the linearity of a PA in order to avoid in-band distortions and interference from adjacent bands. Usually, the linearization techniques are implemented in conjunction with amplification of amplitude modulated signals because the PAs distorts the envelope signal of the fundamental frequency. Higher harmonics are not an issue since it can be easily removed by implementing a low-pass filter. Several linearization techniques exist in order to mitigate the distortions in PA. For example, Cartesian Loop feedback, Polar Loop feedback, feedforward, LINC (Linear amplification with Nonlinear Components), Analogue pre-distortion, Digital pre-distortion and envelope feedback. A brief description of these techniques is presented in this section.

2.4.1 Cartesian Loop Feedback

Feedback mechanism is realized by feeding back a small part of the output signal to the input level in order to enhance the system performance. This method can be utilized to linearize the PA in narrowband. The feedback principle is depicted in Figure 2.8.

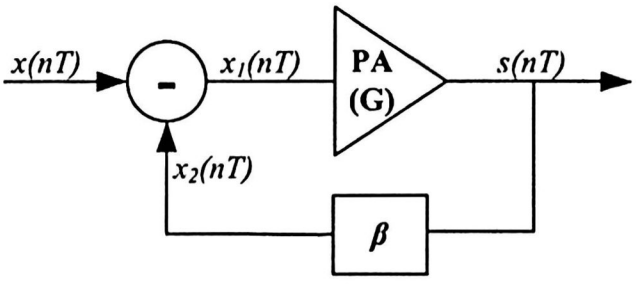


Figure 2.8: Principle of feedback technique

Cartesian loop is a type of feedback that involves linearization of the complete transmitter. In this technique, the baseband I and Q signals are up converted to the carrier frequency and then amplified to required power levels. This signal is then sampled and down converted back into quadrature component to be fed back to the transmitter input. At the input, the signal is compared to the original baseband inputs with error amplifiers(Dawson & Lee, 2004) and(Delaunay, Deltimple, Belot, & Kerherve, 2009). The drawback of this technique is the limited bandwidth due to delay across the loop. Figure 2.9 shows the simplified schematic of PA linearization scheme using Cartesian loop (Monticelli, 2000).

The separate I and Q- signal input are filtered binary symbol sequence, which are run through a differential correcting amplifier into vector modulators generates the actual RF signal. The amplified RF signal from the PA output is coupled and down converted, and the retrieved I and Q signal is compared with the original signals. The

accuracy of the system greatly depends on the gain and bandwidth of the error amplifiers and the linearity of he down converter modulator.

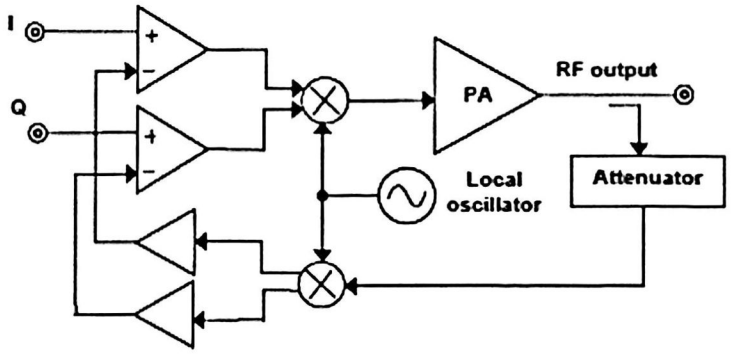


Figure 2.9 Linearization of PA using Cartesian feedback

2.4.2 Polar Loop Feedback

Polar loop is another form of feedback which is used for linearization. This technique is alike Cartesian loop except that the amplitude and phase are fed back to the input instead of I and Q (Sowlati et al., 2004). The constraint with this technique is that the required feedback bandwidths for the amplitude and phase components are different from each other. This restricts the available loop gain to either the amplitude or phase path because one path requires a feedback bandwidth that minimizes available loop gain, while the other path may need a larger loop gain. This impacts the overall linearity enhancement. Usually, the phase feedback operation relies on a phase-locked loop. This loop can encounter locking problems at low amplitudes and also encounter tracking issues for abrupt variation in phase.

Figure 2.10 shows block diagram of a basic polar loop system (Sowlati et al., 2004), which addresses both phase and amplitude distortion with two separate feedback loops. The output of the PA is attenuated and down converted using local oscillator and mixer. The envelope of the incoming intermediate frequency (IF) signal and down converted output are compared and subsequently the bias condition of the

PA is adjusted via one of the errors amplifies in a negative feedback loop. Likewise, the form of the output is compared with the incoming IF with necessary phase correction and subsequently up conversion is performed using voltage controlled oscillators (VCO). Apparently, the linearization scheme considers the system level implementation rather than just the amplifier. The key issue arises from the bandwidth requirement of both amplitude and phase amplifier.

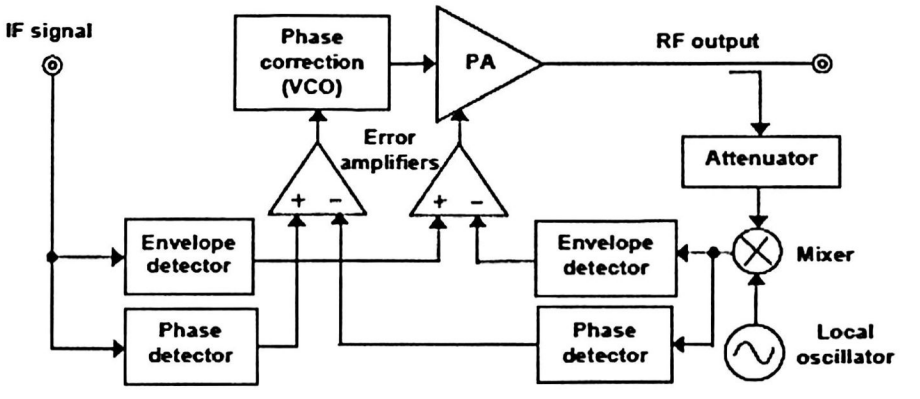


Figure 2.10: Polar loop feedback block diagram

The main advantage of feedback technique is its low complexity, while its main disadvantage is that it's input and output signal are needed to be operated at the same time. This cannot be achieved in practice due to the delays in the circuits. Another constraint of this technique is the stability considerations which limit the bandwidth to a few hundred KHz. This prevents its application in wideband systems (Yang et al., 2010). Common feedback techniques utilized are Cartesian feedback loop and Polar feedback loop.

2.4.3 Feedforward Linearization Technique

The feedforward technique is used to remove the distortions at the PA's output. The feedforward's principle is on the subtraction of the harmonics and intermodulation products from the PA's output spectrum(Liao, Chen, Chiou, & Chen, 2008). Feedforward technique consist of two cancellation loops which are based on two PAs. The two PAs are the main amplifier and an error amplifier.

Figure 2.11 illustrates the basic schematic of RF PA using feedforward linearization scheme. The radio frequency signal is divided in two parts, one portion of the input signal is amplified through main PA and the other part of the signal is processed through a delay element.

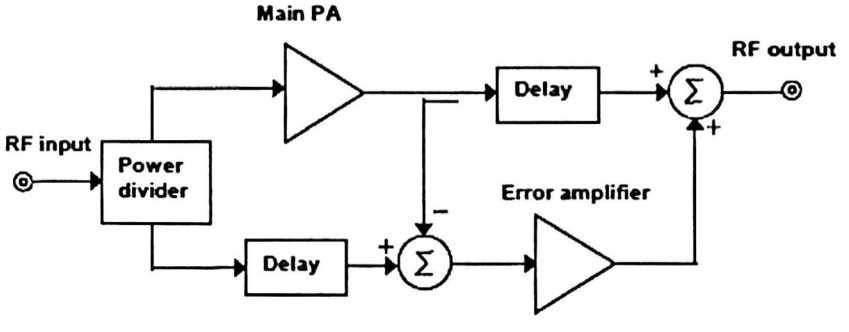


Figure 2.11: Simplified schematic of feedforward PA scheme.

The operation principle of feedforward technique is shown in Figure 2.12 (Tabatabai & Al-Raweshidy, 2007). As shown in Figure 2.12, circuit 1 is the carrier cancellation loop that extracts the distortion products. Circuit 2 is the error cancellation loop which amplifies the distortion products and cancels them by combining main amplifier's distorted output. Therefore, the distortion products are subtracted at the output end. The block τ is the time delay that should be applied to the signal in order to match with the PA paths.

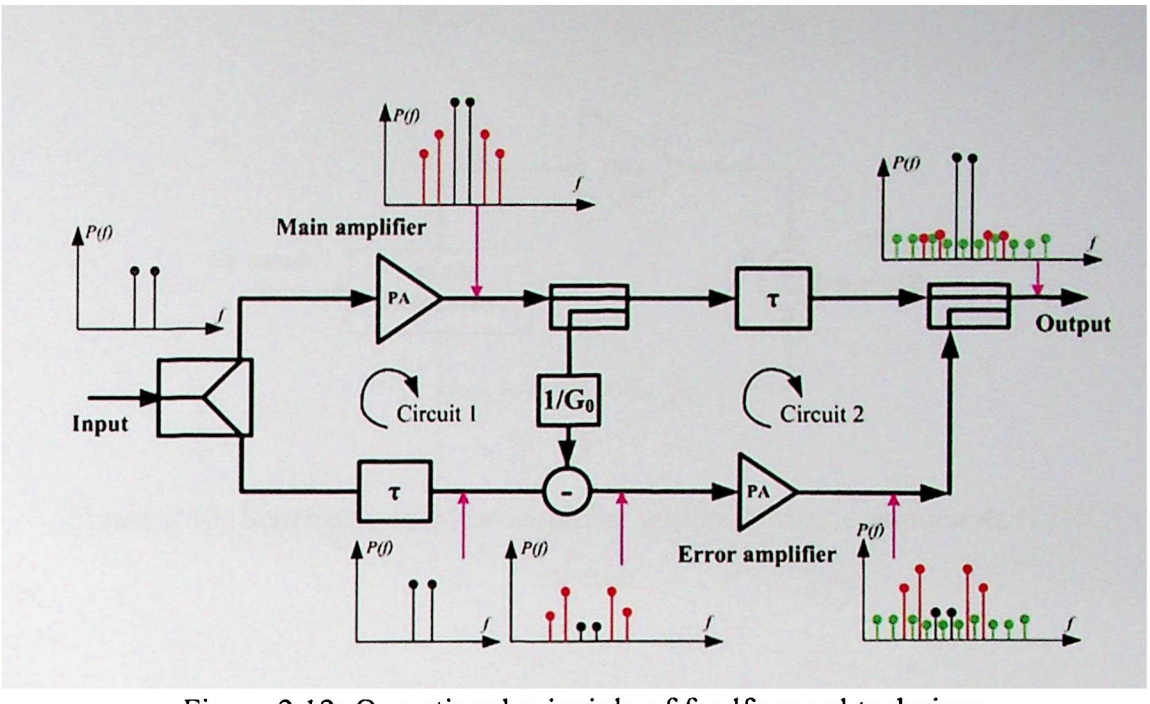


Figure 2.12: Operational principle of feedforward technique

The advantage of utilizing this technique is high stability and does not degrades gain of the amplifier. However, a precise matching of all the amplifying blocks is necessary. The feedforward technique shows good ability in wide band linearization but increases the cost and circuit complexity(Yang et al., 2010).

2.4.4 Linear Amplification Using Non-Linear Component (LINC)

Linear amplification using Nonlinear Components (LINC) is utilized for highly efficient PAs in Class C, D, E or F. The modulated RF input signal is divided into two constant envelope and phase modulated RF signals. The signals are then amplified separately by two PAs with same characteristics. Finally, the two amplified signals are combined at the output with mitigated distortions(García, de Mingo, Valdovinos, & Ortega, 2005). This technique is also regarded as out phasing technique(Raab, 1985), (Hung, Member, Choi, Larson, & Asbeck, 2007),(Xu et al., 2009), (Ding, Hur, Banerjee, Hezar, & Haroun, 2015) and (Beltran, Raab, & Velazquez, 2009).

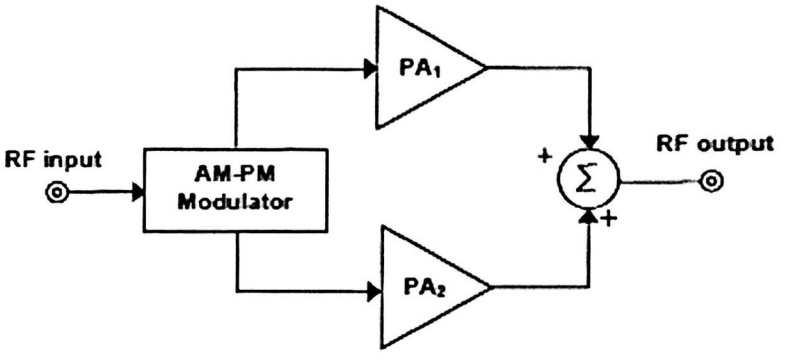
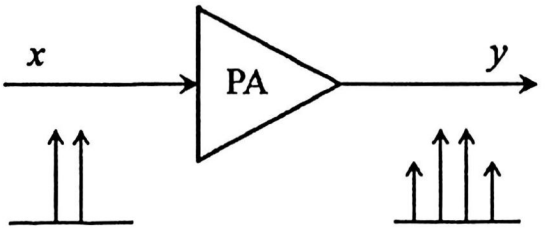


Figure 2.13: Schematic of linear amplifier with nonlinear components (LINC) scheme.

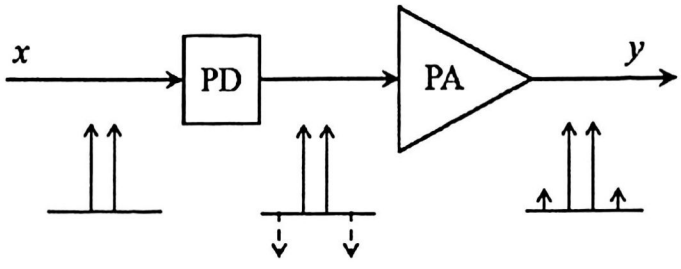
Since the separated signals are constant envelope, it is non-sensitive to the non-linearity of the PAs. Therefore, it is advantageous to utilize a highly non-linear but power efficient PAs. However, the signal separation is very challenging at RF frequencies(Shi & Sundstrom, 2000).

2.4.5 Pre-distortion

Pre-distortion is the technique of canceling out nonlinearities of PA by introducing a distortion characteristic exactly opposite to that of PAs (Vuolevi, Rahkonen, & Manninen, 2001). The pre-distortion block is placed before the PA as depicted in Figure 2.14. If the intermodulation products produced by the pre-distorter is equal in magnitude and out-of-phase to that of the PA, then the ideal cancellation of IMD products is possible.



(a)



(b)

Figure 2.14: Fundamental operation of predistortion.
(a) PA without predistortion. (b) PA with predistortion

Pre-distortion technique is a low-cost solution that gives a moderate performance improvement with additional advantages of low-power consumption and simple circuit configuration compared to feedforward technique. Pre-distortion technique also provides wider bandwidth operation compared to feedback techniques. Pre-distortion can be processed either analogically or digitally. An analog pre-distortion utilizes a non-linear device to pre-distortion the input signal before PA. Meanwhile, digital pre-distortion (DPD) uses DSP (Digital Signal Processor) technology to pre-distortion the input signal (Hammi, Boumaiza, Ghannouchi, & Vassilakis, 2007), (Chung, Holloway, & Dawson, 2008) and (Landin, Fritzin, Van Moer, Isaksson, & Alvandpour, 2012).

2.4.5(a) Analog Pre-distorter (APD)

RF pre-distortion is usually realized by utilizing analog pre-distortion (APD), because the required sampling frequency is too high to process the RF signal digitally. Several APD designs is constructed by using a variable phase shifter (VPS)(Huang, Jeon, et al., 2012)(Cho & Kenney, 2013) and a variable gain amplifier (VGA)(Huang, Woo, Jeon, Lee, & Kenney, 2012). Figure 2.15 shows the APD configuration, where APD offers a complete solution of integrating extra active devices, typically within the