HIGH LINEARITY AND HIGH EFFICIENCY CMOS POWER AMPLIFIER AND UP-CONVERSION MIXER FOR 5G NEW RADIO SUB-6 GHz

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by

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4G	Forth Generation
5G	Fifth Generation
AC	Alternate Current
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
AM-AM	Amplitude Modulation – Amplitude Modulation
AM-PM	Amplitude Modulation – Phase Modulation
APT	Average Power Tracking
BO	Backed-off
Cds	Drain to source Capacitance
Cgs	Gate to source Capacitance
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
DE	Drain Efficiency
ET	Envelope Tracking
GaN	Gallium Nitride
gm	Transconductance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IIP3	3rd Order Intercept Point
IMD3	3rd Order Intermodulation Distortion
LO	Local Oscillator
LTE	Long-Term Evolution
NR	New Radio
OFDM	Orthogonal Frequency Division Multiplexing
OIP3	3rd Order Intercept Point
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Ratio
RF	Radio Frequency
SoC	System-on-Chip

VCO	Voltage Controlled Oscillator

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PENGUAT KUASA DAN PENGADUN CMOS LINEARITI TINGGI DAN KECEKAPAN TINGGI UNTUK 5G RADIO BARU SUB-6 GHZ

ABSTRAK

Generasi Kelima (5G) Radio Baru (NR) adalah teknologi tanpa wayar terkini yang direka untuk memenuhi permintaan yang semakin meningkat dalam rangkaian moden dan peranti yang bersambung, namun ia mengenakan syarat ketat ke atas pemancar, yang boleh menyebabkan penurunan kecekapan disebabkan penggunaan kuasa yang tinggi. Dalam kajian ini, penguat kuasa (PA) CMOS dan pengadun naik penukaran yang cekap dan linear telah dibangunkan untuk aplikasi 5G NR Sub-6GHz. Sebuah *linearizer* berasaskan pengadun telah diintegrasikan pada input PA untuk meningkatkan prestasi merentasi julat frekuensi yang luas, memastikan sistem mengekalkan kecekapan dan lineariti yang tinggi walaupun dengan pengurangan kuasa keluaran sebanyak 3 dB. PA CMOS dan pengadun yang bersepadu ini, yang difabrikasi menggunakan teknologi CMOS 130 nm, meliputi jalur lebar 1 GHz dari 4 GHz hingga 5 GHz. Keputusan pengukuran menunjukkan keuntungan melebihi 30 dB, dengan kuasa keluaran maksimum berkisar antara 23.85 hingga 23.39 dBm, kecekapan kuasa tambahan puncak (PAE) antara 41.3% hingga 41.04%, dan titik temu ketiga keluaran (OIP3) antara 31.38 hingga 32.53 dBm. Keupayaan sistem untuk mengekalkan lineariti telah disahkan melalui ujian dengan isyarat 16 QAM, menonjolkan inovasi *linearizer* berasaskan pengadun yang diintegrasikan dengan pengadun sebelum dimasukkan ke dalam PA.

HIGH LINEARITY AND HIGH EFFICIENCY CMOS POWER AMPLIFIER AND UP-CONVERSION MIXER FOR 5G NEW RADIO SUB-6 GHZ

ABSTRACT

Fifth Generation (5G) New Radio (NR) is the latest wireless technology designed to meet the growing demands of modern networks and connected devices, but it imposes stringent requirements on transmitters, leading to potential reductions in efficiency due to high power usage. In this study, a highly efficient and linear CMOS power amplifier (PA) and up-conversion mixer were developed for 5G NR Sub-6GHz applications. A mixer-based linearizer was integrated at the PA's input to enhance performance across a wide frequency range, ensuring the system maintained high efficiency and linearity even with a 3 dB reduction in output power. The integrated CMOS PA and mixer, fabricated using 130 nm CMOS technology, cover a 1 GHz bandwidth from 4 GHz to 5 GHz. Measurement results demonstrated a gain of over 30 dB, with maximum output power ranging from 23.85 to 23.39 dBm, peak power-added efficiency (PAE) from 41.3% to 41.04%, and an output third-order intercept point (OIP3) between 31.38 and 32.53 dBm. The system's ability to maintain linearity was confirmed through testing with a 16 QAM signal, highlighting the innovation of the mixer-based linearizer integrated with the mixer before feeding into the PA.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Radio frequency (RF) wireless communication systems are widely utilized in many electronic devices, particularly in mobile applications. Since the introduction of the first modern mobile systems, the wireless market has experienced an exceptional boom, with an ongoing increase in the number of subscribers. Figure 1.1 illustrates the progression of mobile subscriptions through technology up until now, displaying the increasing number of mobile subscriptions [1].

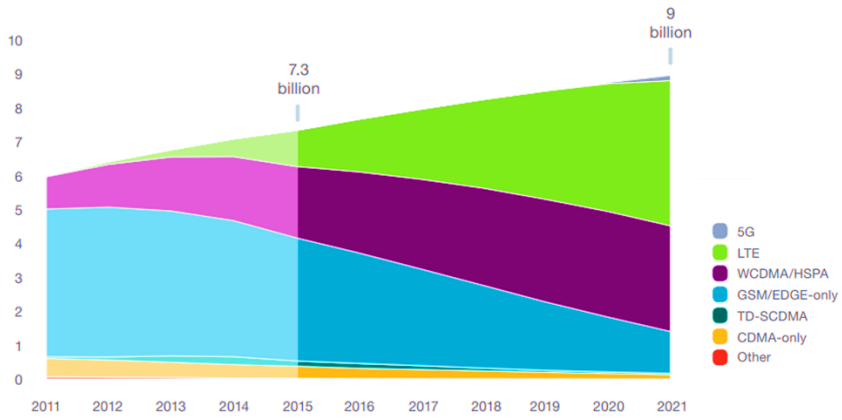

Figure 1.1 Mobile subscription trend up to recent times [1].

Faster speeds, lower latencies, and extended connectivity will be available with 5G networks, which are the next generation of mobile systems. The new 5G system will give access to a broad range of new services, and extended connectivity is necessary for IoT, smart home applications, and areas that utilize smart devices frequently.

5G New Radio (5GNR) will incorporate electromagnetic waves with higher frequencies, at least until 30 GHz in the millimeter-wave zone. Natural obstacles such

as obstructions and extreme weather conditions are more likely to affect these new frequencies, leading to shorter distances. The utilization of such high frequencies is anticipated to increase the quantity of mobile antenna stations required to cover the same geographical regions.

The consumer world has heavily promoted 5G as a leap forward for mobile devices, deeming it the next generation of wireless smartphone communications. Seven different global standards organizations are part of the 3rd Generation Partnership Project (3GPP), which is developing standards for 5G. In December of 2017, the 5G standards were started and are being enhanced in subsequent releases with the addition of new features, functionality, and requirements.

Technical Specification Groups (TSGs) are responsible for delineating 5G NR systems at increasingly abstract levels within 3GPP. Examples include, but are not limited to:

- Radio Performance Specifications at the lower level [1]-[3] are determined by Radio Access Network (RAN)
    - The physical layer
    - Modulation
    - Frequency-division duplexing (FDD)
    - Time-division duplexing (TDD)
    - Beamforming
    - Error detection
    - Correction
- Overseeing the overall architecture and service capabilities, which includes charging, accounting, network management, and security, is the responsibility of Services and Systems Aspect (SA).

- Specifications for user equipment, handoff between networks, and quality of service mapping are defined by the Core Network & Terminal (CT).

The growth of frequencies and bandwidth has been steady as wireless telecommunications technologies have progressed. In Figure 1.2, it is depicted that the latest generations retain some compatibility with older networks, but expand their coverage to more frequency bands.

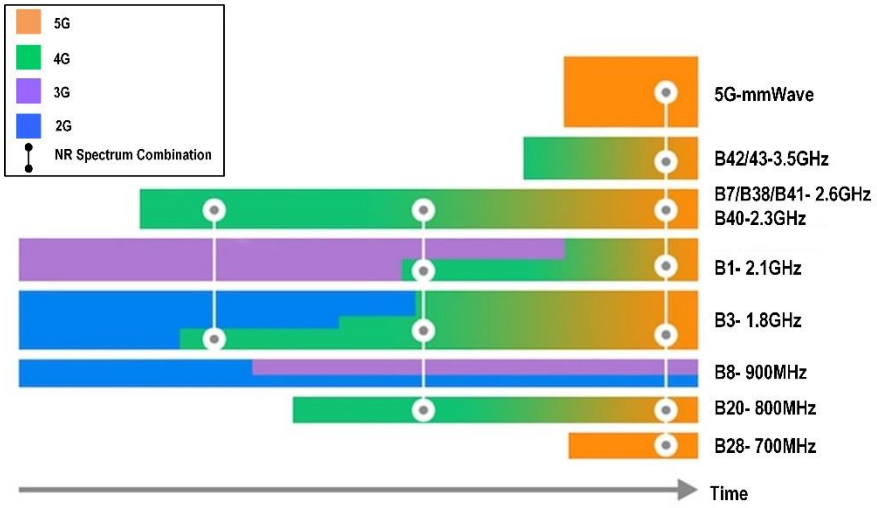

Figure 1.2 Evolution of frequency spectrum allocations for 2G, 3G, 4G and 5G networks [2].

As 5G progresses into millimeter-wave (mmWave) frequencies above 30 GHz, this trend takes a significant leap. 5G NR is capable of supporting ultra-wide bandwidths up to 100 MHz for frequencies under 6 GHz and up to 400 MHz for higher frequencies [3].

- FR1
  - Lower frequencies: 700 MHz – 1 GHz
  - Mid frequencies: 1-7 GHz
- FR2
  - Higher frequencies: 24-48 GHz

Transmitters and receivers are part of RF communication systems, which are used to transmit and receive data. Designing the transmitter, particularly the power amplifier (PA) block, is the most challenging task in developing a transceiver due to its unmoderate DC power consumption. The PAs are commonly fabricated using semiconductors with III-V compound such as GaN HEMT [2], GaAs HBT [3]-[4], Si Bipolar [5]-[6], and SiGe HBT [7]-[9] because of its advantages in delivering favourable linear output power and efficiency in contrast to silicon CMOS process. This hinders the progress of integrating towards a genuine single-chip radio or a system-on-chip (SoC). The size, implementation cost, and integration constraints with CMOS baseband chips are among the numerous drawbacks that PAs designed with the III-V compound have [10].

There has been a significant increase in research efforts on CMOS-based RFICs for wireless mobile applications [11]-[18]. CMOS based PAs have several disadvantages due to the lower breakdown voltage, higher substrate loss, and unavailability of back via-hole for the ground which limit the achievable output power and efficiency as compared to its III-V counterparts [19]-[21]. The efficiency and linearity of CMOS PAs [22]-[25] can be improved through the application of several performance enhancement techniques to overcome these drawbacks.

CMOS Power Amplifiers (PAs) have undergone extensive testing to meet the needs of low-priced transceivers. Nevertheless, the high peak to average power ratio signals in modern wireless communication system poses great challenge for CMOS PA implementation, due to the high trade-off between linearity and efficiency as contrasted to GaAs PAs [4] [5] and [6].

The maximum power transfer can be achieved by ensuring that impedances between the input stage and driver stage, between the power stage and the output stage,

and between the driver and power stage interstage match. The PA must possess a high reverse isolation and be linear. As power amplifier are extensively utilized as a part of transceiver it is perfect to hold a less power consuming device and having less active chip size at the applicable frequency, accomplishing desired gain, power added efficiency (PAE) and return losses [7].

The intrinsic drawbacks of typical CMOS processes have made it difficult to effectively commercialize CMOS PAs. There exists Q factors of low quality, lossy substrates in passive structures, low breakdown voltage, and low transconductance of active devices. To overcome the limitations of CMOS technology in PA designs, various efforts have been made, such as enhancing linearity and efficiency[8].

Standard CMOS requires understanding of technology constraints in order to recognize high-efficiency RF power amplifiers [9]. The goal of full CMOS, single-chip radio can only be achieved if there is significant effort to improve efficiency, output power, and operating frequency [10].

Highly linear PAs that consume higher DC power are often the target of efficiency enhancement techniques. Switching-based PAs with low conduction angles commonly use linearity enhancement techniques, but these methods also contribute to non-linearity. Efficiency and linearity performance in CMOS PAs are inevitably inversely proportional to each other. Recently, there has been a significant increase in research into the bandwidth enhancement of CMOS PAs, in addition to efficiency and linearity [10].

1.2 Problem Statement

Mobile wireless RF front ends typically incorporate multiple antennas to accommodate various communication standards operating at different frequencies, as

shown in Figure 1.3 [11]. To streamline the system and reduce costs, it is crucial for a single power amplifier (PA) to support wide bandwidth operation and multiple frequency bands, thereby eliminating the need for multiple PAs and reducing the chip footprint. However, achieving consistent linearity and efficiency across a broad frequency range is challenging due to the fluctuating frequency response of devices.

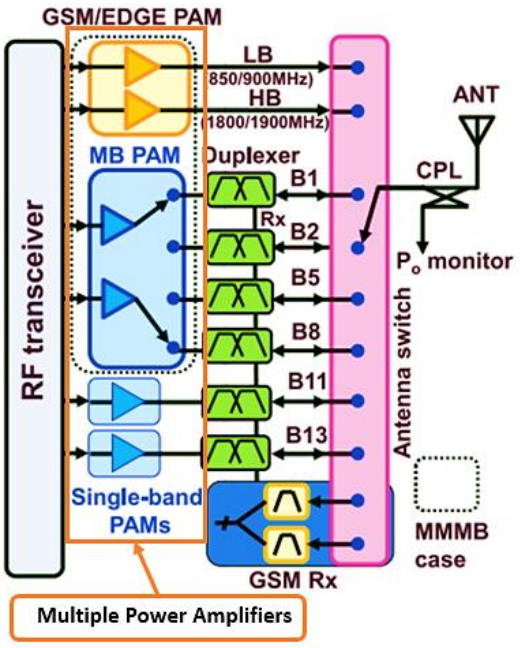

Figure 1.3 Block diagram of a mobile RF front end [11].

In addition, wireless communication systems often use Orthogonal Frequency-Division Multiplexing (OFDM), which relies on the Fast Fourier Transform (FFT) to improve resilience to multipath signal fading [12]. Despite this, the transmitter's performance can be adversely affected by the high Peak-to-Average Power Ratio (PAPR) of the signal. To ensure linear transmission and efficient operation without clipping high PAPR signals, the PA must operate with back-off output power (P_{bo}). The P_{bo}, which is the PA's output power reduced from its maximum level, typically results in lower Power Added Efficiency (PAE). Higher PAPR demands lead to greater P_{bo} and decreased PAE, making linearity enhancement crucial to mitigate P_{bo} impacts, as illustrated in Figure 1.4 [13].

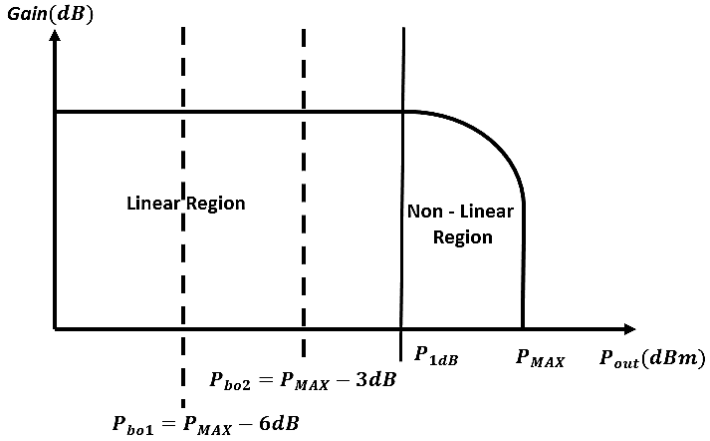

Figure 1.4 P_{BO} concept of a PA [13].

Figure 1.5 outlines the PAPR requirements for various mobile wireless communication standards [14]. Meeting both linearity and PAE performance goals is challenging since high linearity often occurs at lower power levels, which degrades PAE, while high PAE is achieved at peak power levels where linearity suffers. Figure 1.6 exemplifies this trade-off between linearity and PAE in RF power amplifiers [15].

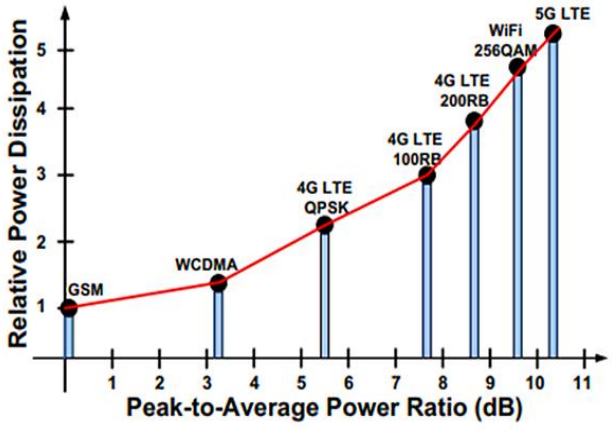

Figure 1.5 PAPR requirement of various wireless communication standards [14].

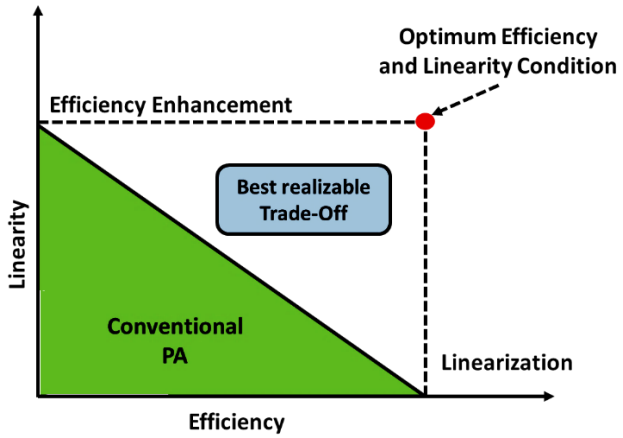

Figure 1.6 The trade-off between linearity and PAE of a RFPA [15].

Additional performance metrics such as Adjacent Channel Leakage Ratio (ACLR) are used to evaluate PA linearity. For instance, to meet an ACLR specification requiring 28 dBm output power with a PAPR requirement of 7 dB, the PA's maximum output power should be 35 dBm. Developing effective linearization methods to lower Pbo and prevent PAE degradation is essential, especially for wideband operation were maintaining linearity and PAE across a frequency range is critical.

Reducing power consumption remains a key objective in designing network entities and devices. Techniques like Average Power Tracking (APT), Envelope Tracking (ET), high voltage supply, power combination methods, Doherty amplifiers, reconfigurable techniques, and Digital Pre-Distortion (DPD) are employed to improve efficiency and manage power consumption. Each method has its limitations and benefits, influencing overall PA performance. Efficiency and power consumption have a relationship that can be described as:

$$PAE = \frac{(P_{OUT} - P_{IN})}{P_{dc}} \quad (1.1)$$

$$PAE = \frac{(P_{OUT} - P_{IN})}{(V_{dc} I_{dc})} \quad (1.2)$$

$$PAE_{BO} = \frac{P_{BO}}{P_{DC}} \quad (1.3)$$

This research aims to address the challenges of achieving high linearity and efficiency in CMOS PAs and up-conversion mixers for 5GNR Sub-6 GHz applications. By focusing on both the PA and mixer linearization, the goal is to minimize the trade-offs between linearity and efficiency, thereby reducing overall transmitter power consumption while enhancing performance. The development of a highly linear and efficient integrated CMOS transmitter is pursued by combining a high-efficiency CMOS PA with a mixer-based linearizer, achieving optimal performance across the 4.0 to 5.0 GHz frequency range.

1.3 Research Objectives

The main objectives of this research are to:

I. Design high efficiency CMOS power amplifier (PA) operates with a wide bandwidth from 4.0 to 5.0 GHz for 5G NR sub-6 GHz application, achieving minimum peak added efficiency (PAE) of 40%.

II. Design a CMOS mixer with a power consumption of less than 8mW and OIP3 of more than 7 dBm with minimum conversion gain of 8 dB from 4 GHz to 5 GHz for 200 MHz IF frequency.

III. Design a CMOS linearizer and integrate it to the mixer while achieving power consumption of less than 9 mW.

IV. Integrate the mixer-based linearizer to the CMOS PA to achieve maximum linear output power of more than 20 dBm from 4.0 GHz to 5.0 GHz with a linear PAE of more than 35%.

1.4 Scope and Limitation

This project can be categorized into two major parts. First part is designing high linearity and high efficiency CMOS PA and up-conversion mixer using the Cadence software. The operating frequency of the high linearity and high efficiency CMOS PA and up-conversion mixer is limited from 4.0 to 5.0 GHz. The Cadence software is used to design and simulate the high linearity and high efficiency CMOS PA and up-conversion mixer according to the design specification and requirements. Besides that, the layout design also done by using the Cadence Software. The pre-layout and post-layout simulation were done in cadence software and the GDSII is streamed out for fabrication process. The results of the schematic simulation and post layout simulation will be verified in terms of its S-parameters, Gain, Power Added Efficiency (PAE) and 3rd order Intercept Point (OIP3). Second part is on the measurement on the fabricated chip. The best given results from simulation will be fabricated. The fabricated chip will be measured to verify the post-layout simulation result.

There is limitation in CMOS to design high linearity and high efficiency CMOS PA and up-conversion mixer. From an absolutely performance-oriented viewpoint, CMOS technologies still lacking as compared to other technologies. Nevertheless, the integrability and adaptability of CMOS to achieve a single chip solution for wireless communications as the motivation for continuous improvement through circuit innovation. Moreover, CMOS advances would be the least expensive among different applicants, for example, III-V HBT, III-V PHEMT, SiGe HBT, and Si-MOSFET technologies. Consequently, it appears to be unavoidable that both customers and manufacturers will pick CMOS technologies over all others.

1.5 Thesis Outline

Chapter 2 presents the profound literature study on CMOS PA performance metrics, PA architectures, PA topologies, non-linearity in CMOS PA, linearity enhancement techniques, efficiency enhancement techniques and recent work comparisons which has been conducted by multiple research organizations on linearization and efficiency enhancement technique. Besides that, CMOS Up-conversion mixer, mixers figure of merits, mixer topologies, mixer design architectures, non-linearity in CMOS mixer and recent work comparisons of linearization technique in CMOS up-conversion mixer which has been conducted by multiple research organizations is presented as well. Furthermore, recent research has addressed non- linearity in CMOS PA and CMOS mixer. Lastly, the CMOS Transmitter, the integrated CMOS PA and up-conversion mixer, and recent work have been discussed.

The detailed methodology for a high linearity and high efficiency integrated mixer-based linearizer to CMOS PA for 5GNR Sub-6 GHz is presented in Chapter 3. An extensive theoretical analysis has been provided for integrated CMOS PA and mixer-based linearizers with high linearity and high efficiency. This section also explains the measurement setups.

Chapter 4 presented of high-efficiency CMOS PA and mixer-based linearizer simulations results. Besides that, presented complete post layout simulation and measurement results achieved by the high linearity and high efficiency integrated CMOS Power amplifier and up-conversion mixer are presented and elaborated in this chapter. The proposed design comes with the fabricated chip micrograph as well.

In Chapter 5, the conclusion and proposed future works for this research are presented.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter offers a comprehensive review of the existing literature on key components in radio frequency (RF) integrated circuits, specifically focusing on CMOS power amplifiers (PAs), CMOS up-conversion mixers, and integrated CMOS transmitters. It delves into the fundamental principles, design techniques, and performance metrics that define these components, examining the evolution of CMOS technology in the context of RF circuit design. The review also highlights the latest advancements and challenges in developing high-efficiency and high-linearity CMOS PAs, the role of CMOS up-conversion mixers in frequency translation within RF systems, and the integration of these components into complete CMOS transmitter systems. By synthesizing insights from various studies, this chapter provides a solid foundation for understanding the state-of-the-art in CMOS RF design, setting the stage for the subsequent analysis and development presented in this thesis.

2.2 CMOS Power Amplifier

The design of a transmitter relies heavily on a power amplifier (PA). Choosing the right architecture and class to meet system requirements is crucial due to their characterization as the most power-consuming part of the transmitter. As the final stage in radio transmitter, the power amplifier (PA) performs the important functions of amplifying the up-converted signal and delivering the desired power to a load, such

as a 50Ω. Due to its requirement to drive large output power, it often becomes the primary block in the entire transceiver chain when it comes to power consumption.

Table 2.1 shows the impact of the PA on some state-of-the-art CMOS Transceivers for a variety of communication protocols, allowing a measurable understanding of the importance of this decision.

Table 2.1 PA power consumption impact in state-of-art CMOS Transceivers in a variety of communication protocols. Adapted from [12]

Standard	Total Power Consumption, PDC,T (mW)	PA Power Consumption, PDC (mW)	Impact (%)	CMOS
Bluetooth [17]	19.5	7.5	38.5	0.25um
IEEE 802.11 [18]	1212	690	56.9	0.18um
WCDMA [19]	2114	1700	80.4	0.13um

2.2.1 PA Figure of Merits

This section outlines and clarifies the most crucial aspects of PA design. PAs' typical parameters are discussed, which include output power, efficiency, gain, stability, and linearity.

2.2.1(a) Output Power

Output power is essential in the design of a PA. Low output power can cause the PA to lose its individuality, making it difficult to specify. A power amplifier, as its name implies, is designed to enhance the power level of the input power applied, without altering the signal content. The power output of a PA is measured in its actual real power delivered to the antenna load at the operation frequency. A radiated electromagnetic wave is generated by the electrical power being dissipated in the

antenna. A generic amplifier's input and output power paths are illustrated in Figure 2.1. This figure depicts E_S as an RF source that transmits a signal at a frequency of f_0. Table 2.2 shows the design parameters of a PA.

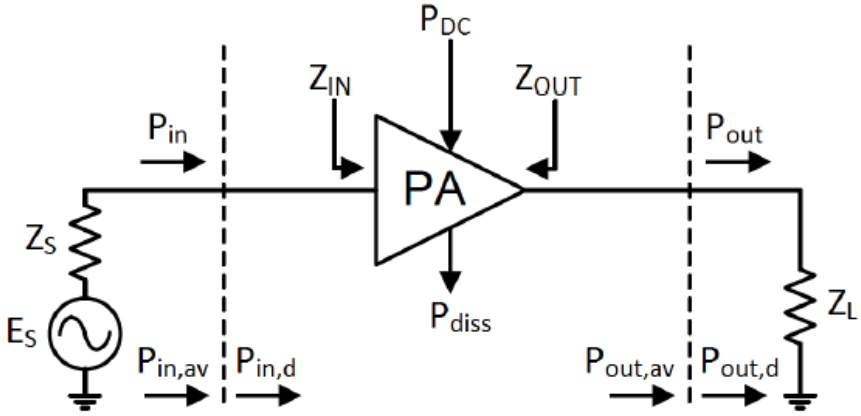

Figure 2.1 Characteristic parameter of a PA [12]

Table 2.2 Design parameters

P_{in}	Input power of the PA
P_{out}	Output power of the PA
$P_{in,av}$	Power available from the source
$P_{in,d}$	Power delivered to the amplifier
$P_{out,av}$	Power available from the amplifier
$P_{out,d}$	Power delivered to the load
P_{DC}	DC power supplied to the amplifier
P_{diss}	Power dissipated by the amplifier
Z_S	Source impedance of the generator
Z_L	Load impedance of the PA
Z_{in}	Input impedance of the PA
Z_{out}	Output impedance of the PA

Design parameters can be only determined by the amount of current that provides the required output power when a supply voltage is passed as a fixed value. The instantaneous output power can be calculated as:

$$P_{out}(t) = V_{out}(t).I_{out}(t) \quad (2.1)$$

Where the $V_{out}(t)$ and $I_{out}(t)$ are instantaneous output voltage and current respectively. The average output power can be written as

$$P_{out} = \overline{P_{out}(t)} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} P_{out}\,(t)dt \qquad (2.2)$$

Where $\overline{P_{out}(t)}$ represents the average of the instantaneous output power. If the output signal is periodical with the period given

$$T_0 = \frac{2\pi}{\omega} \qquad (2.3)$$

Where the angular frequency ω is defined as $\omega = 2\pi fc$. The average power of a periodic signal can be calculated using

$$P_{out} = \overline{P_{out}(t)} = \frac{1}{T_0} \int_{-T/2}^{T/2} P_{out}\,(t)dt \qquad (2.4)$$

The average power delivered to a purely resistive load can also be calculated in form of current and voltage signal according to

$$P_{out} = \frac{V^2{}_{out,rms}}{R_L} = I^2{}_{out,rms} \cdot R_L \qquad (2.5)$$

Where $V^2{}_{out,rms}$ and $I^2{}_{out,rms}$ are the RMS values of the output voltage and the current respectively.

2.2.1(b) Gain and Bandwidth

The relationship between output power and input power determines the power gain of a two-port amplifier in our study. As the signal passes through the PA from the generator to the load, there are several reflections due to mismatching problems. Different gain definitions are caused by this phenomenon, which has penalties for power gain.

Transducer gain $GT = Pout,dPin,av$ (2.6)

Available gain $GA = Pout,avPin,av$ (2.7)

Operating gain $GP = Pout,dPin,d$ (2.8)

The delivered power differs from the available power because of matching imperfections. Assuming that the matching is perfectly realized:

$Pin,av = Pin,d$

$Pout,av = Pout,d$

RF power amplifiers often use the transducer gain as it is easily measurable and takes into account input and output mismatches. Hence, the shortened term 'gain' is used to mean 'transducer gain'. The stability and matching network losses are analyzed by using other gain definitions in the small signal domain.

The gain of a power amplifier is defined as:

$$G_B = 10 \log \left(\frac{P_{out}}{P_{in}} \right) \quad (2.9)$$

where $Pout$ is the output power and Pin is the input power.

PAs are required to use the entire bandwidth of the communication standard that is in use. Cascaded stages are the norm for 5G New Radio to accomplish both high gain and wide band. If high output powers is to be delivered the output stage transistors must have a large size that means a huge input capacitance; this can create problem to the driving circuit. By implementing one or more pre-driving stages, the output transistor can be optimally driven, but it comes with increased power consumption.

2.2.1(c) Efficiency

The PA efficiency is determined by the percentage of energy that is transformed into an RF signal from the Direct Current (DC) power supply. To save power, a PA needs to be as efficient as possible. As previously mentioned, efficiency has a significant impact on crucial aspects of communication systems, like battery cost,

electrical power expenses, power supply weight, operational time, and cooling system size.

Efficiency is defined by two main concepts:

The ratio of output power to consumed power is known as Drain Efficiency (η_d or DE).

$$\eta_d = DE = \frac{P_{out}}{P_{DC}} \tag{2.10}$$

and the Power Added Efficiency (PAE) is the ratio between the additional power provided by the PA (the difference between the output power and the input power) and the consumed power (P_{DC}):

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.11}$$

Using the expression of the transducer gain, it can be shown that:

$$PAE = \eta_d \left(1 - \frac{1}{G_T}\right) \tag{2.12}$$

Back-off PAE as follows:

$$PAE_{Back-off} = \frac{P_{out,Back-off} - P_{in}}{P_{DC}} \tag{2.13}$$

As the transducer gain rises, the PAE will increase towards its maximum, which is the drain efficiency. The PAE expression has a greater use than the η_d because it considers the input power. At low frequencies, where the input port dissipates little power and the high gain makes $Pout$ much bigger than Pin, the two measurements coincide. As the frequency increases, the gain decreases, and the input power absorbed is comparable to the stage's output power. In this situation, the PAE is an estimation of efficiency that is more accurate.

2.2.1(d) Linearity

As shown in Figure 2.2, a PA can be represented by a single block at the system level, while considering x as the input signal and y as the output signal.

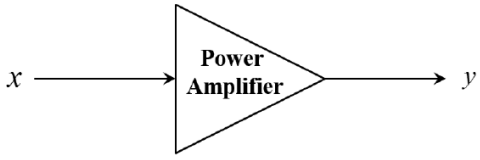

Figure 2.2 Input-output representation of a PA [20].

For a linear system which have a transfer function of G(x), the output of this linear system is given as $(a_1 \times G(x_1)) + (c_2 \times G(x_2))$ for the input $(c_1 \times x_1) + (c_2 \times x_2)$. Withal, the PA is a non-linear system and creates several additional terms at different frequencies than the input signal. MOSFET devices used in PAs result in non-linearity due to the non-linear current and capacitance dependent on device voltages [21][22]. Modulated signals generate distortions when driven by these non-linear sources. The major non-linear elements of a MOSFET device are non-linear transconductance (gm), the drain-source capacitance (Cds), and the gate-source capacitance (Cgs) [23].

The polynomial of a non-linear transfer function can be approximated using Taylor series expansion. First-order (gain), second-order (squaring), and third-order (cubing) are the terms that are essentially evaluated [20]. PA non-linearity can be represented by:

$$V_0(t) = a_0 + a_1 V_i(t) + a_2 {V^2}_i(t) + a_3 {V^3}_i(t) \quad (2.14)$$

2.2.1(d)(i) 1 dB Compression point

The main cause of distortion products in a transceiver chain is the inherent non-linearity of RF power amplifiers. The spectrum's utilization is influenced by this. The compression behaviour of the power amplifier often leads to non-linearity. Gain compression and harmonic distortion are usually responsible for non-linearity, which results in imperfect reproduction of the amplified signal.

Figure 2.3 illustrates a method for measuring the 1dB compression point, which is one of the methods used to quantify the linear operating range of a power amplifier.

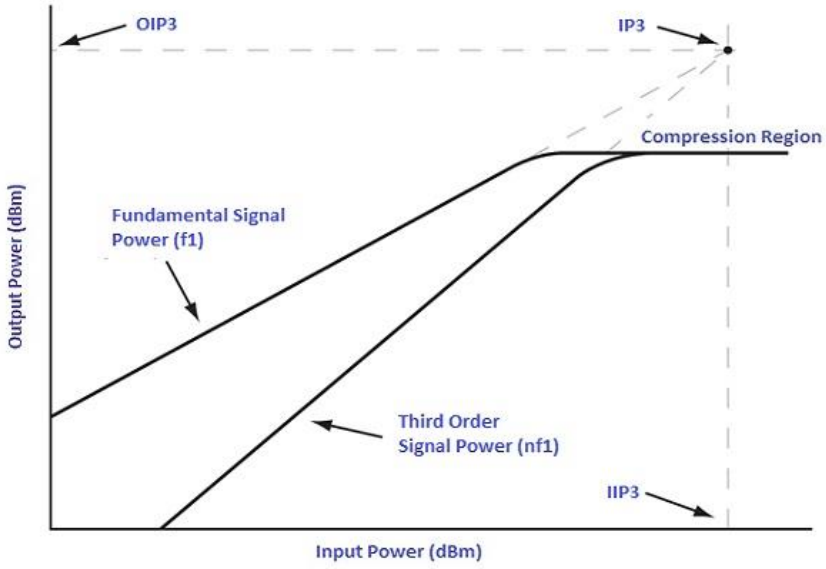

Figure 2.3 1 dB compression point [20].

2.2.1(d)(ii) Intermodulation Distortion

PAs are usually tested with a two-tone method, where two closely spaced fundamental signal tones are applied to their input. Increasing the amplitude leads to the third-order cross product generating a signal over the noise floor [24], [25] and [26]. When two tone signals are supplied to the PA, intermodulation distortion (IMD)

occurs. The third order product is of utmost concern due to its presence within the band of fundamental signals and its difficulty in filtering out. Higher order products are typically small and do not cause any significant distortion, which makes them easy to filter out [27]. A two-tone signal is applied to the PA input, and it produces:

$$V_i(t) = v\,Cos(\omega_1 t) + v\,Cos(\omega_2 t) \tag{2.15}$$

$$V_0(t) = a_0 + a_1 v[Cos(\omega_1 t) + Cos(\omega_2 t)] + a_2 v^2[Cos(\omega_1 t) + Cos(\omega_2 t)]^2 + a_3 v^3[Cos(\omega_1 t) + Cos(\omega_2 t)]^3 \tag{2.16}$$

Table 2.3 contains the list of resulting harmonics and IMD products.

Table 2.3 Two tone IMD products up to third order

Order	Terms	a1V	a2V	a3V
Zero	0		1	
First	ω1	1		9/4
	ω2	1		9/4
Second	2ω1		1/2	
	2ω2		1/2	
	ω1+/-ω2		1	
Third	3ω1			1/4
	3ω2			1/4
	2ω1+/-ω2			3/4
	2ω2+/-ω1			3/4

Figure 2.4 displays the output spectrum of a PA, which includes both the fundamental signals and the spurious products generated by IMD distortion. As can be seen in Figure 2.4, the third order IMD products which appearing at frequencies $2\omega_1$-ω_2 and $2\omega_2$-ω_1 are the main contributor to the signal distortion since they are located very near to the fundamental tones and its quite difficult to be filtered out [28].

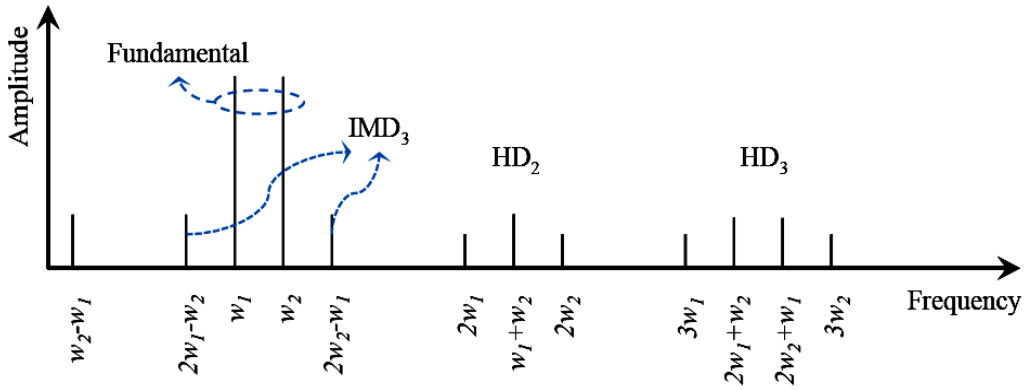

Figure 2.4 IMD products generated by a PA [28].

2.2.1(d)(iii) AM-AM and AM-PM

The most common ways to determine PA's non-linearity are AM-AM (Amplitude to Amplitude) and AM-PM (Amplitude to Phase) [29]. To achieve optimal response in a linear system:

$$A_{out} = G_0 A_{in} \tag{2.17}$$

Where A_{in} and A_{out} are the input and output amplitudes of the PA respectively, while G_0 is the constant linear gain of the PA. In practice, obtaining a linear response of G_0 is a challenging task. The output amplitude is compressed when there is a high input amplitude level, which is due to the inherent non-linearity of the PA [29]. Additionally, the phase change is a measure of time delay. For all amplitude levels, this time delay remains constant in the ideal scenario. The AM/PM fluctuates because of non-linear effects influenced by signals or devices. Figure 2.5 and 2.6 highlight the AM/AM and AM/PM characteristics of a PA.

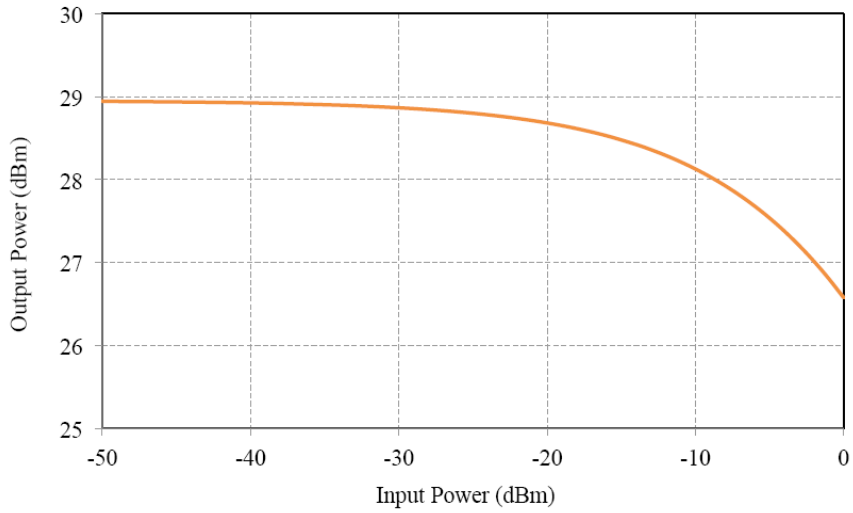

Figure 2.5 AM-AM characteristics [29].

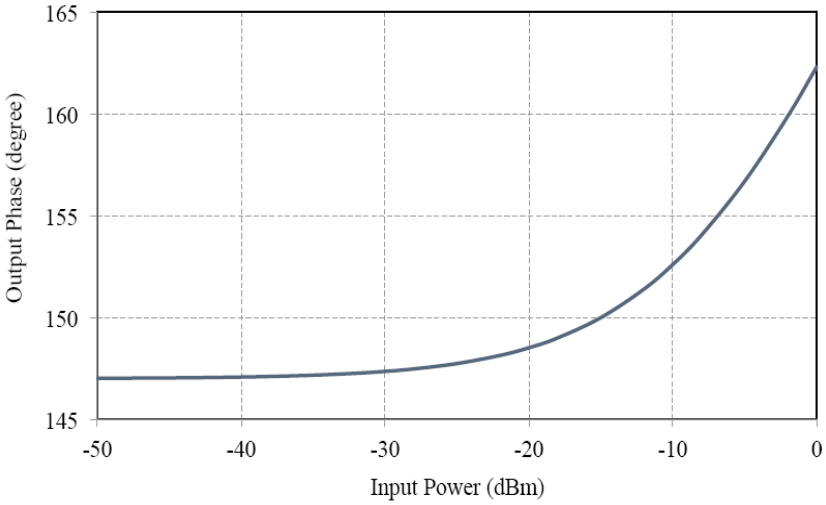

Figure 2.6 AM-PM characteristics [29].

2.2.1(d)(iv) Modulated Signal

When modulated input signals are used, non-linearity can result in undesirable distortions like spectral regrowth, dispersion, or rotation of the constellation [30]. The typical parameters employed for evaluating this non-linearity are ACPR (Adjacent Channel Power Ratio) in frequency domain and EVM (Error Vector Magnitude) in time domain [31], [32] and [33].

The frequency domain is where spectral regrowth is a common non-linear phenomenon that occurs. When the PA's input and output signal spectrum is compared, it can be observed that the power regrows in the adjacent frequency channels. Other communications may use these adjacent channels, resulting in interference. The output spectrum is depicted in Figure 2.7. The main channel and the adjacent channels are separated by 5 MHz. The spectral regrowth of the output signal spectrum is visible in the figure and interferes with adjacent channels.

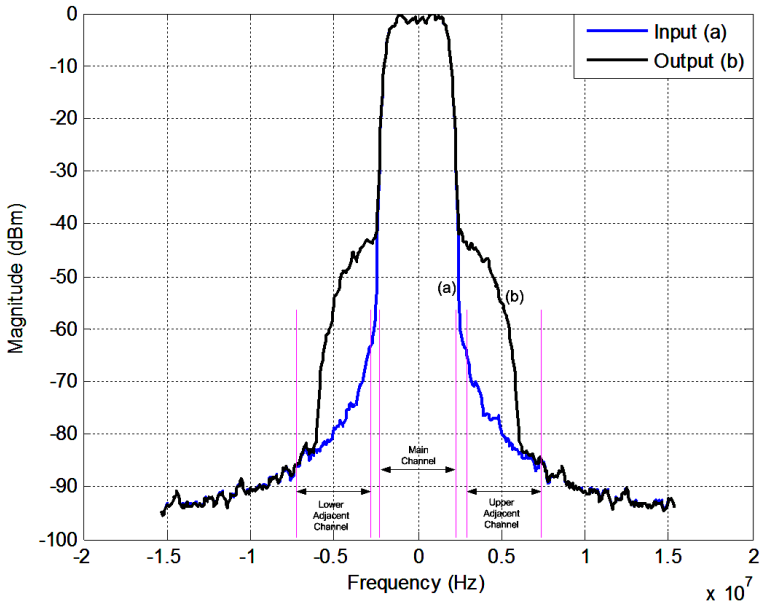

Figure 2.7 Spectral regrowth [30].

The ACPR represents the power ratio between undesirable distortion in the adjacent channel and the signal in the main channel. The spectral regrowth is mostly observed on the channels that are adjacent. The ACPR for adjacent channel is described as:

$$ACPR_{adj} = 10\ log \frac{\int S(f)df\ (adj)}{\int S(f)df(main)} \tag{2.18}$$

where S(f) represents the power spectral density of the output signal and the term adj represents either the first lower or upper channel.

2.2.1(e) Stability

Stability is the most crucial measure that must be taken. This can be a crucial aspect of designing a high gain amplifier. Instability is a concern for circuits that gain at all frequencies. To avoid in-band instability, an amplifier must be designed to be unconditionally stable [31]. The Rollett (K) value must exceed unity.

The K-Factor can be expressed equally:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2.|S_{21}||S_{12}|} \quad (2.19)$$

where, $|\Delta| = |S_{11}.S_{22} - S_{21}.S_{12}|$

Unconditionally stable when K>1, conditionally stable is when the 0<K<1 and the circuit is unstable is when the K<1.

2.2.2 PA Architectures

In this subtopic, various power amplifier (PA) architectures are discussed, including single-ended, differential, and balanced structures. Each architecture is analysed in terms of its design principles and operational characteristics.

2.2.2(a) PA Structures

The literature has reported a variety of PA architectures. Single-ended, differential, and balanced are the three categories that can be classified as shown in Figure 2.8.

Single-ended structure: Most PAs have been built in a cascade of single-ended stages. The reason for this choice is twofold: the antenna is generally single-ended, and single-ended RF circuits are simpler to test than their differential counterparts. The performance and stability of this structure are influenced by the ground return path, which needs to be perfectly mastered.