GREEN SYNTHESIZED CeO_2 NANOSTRUCTURES ON CeO_2 AND Eu DOPED CeO_2 AS PASSIVATION LAYER FOR SILICON BASED METAL-OXIDE-SEMICONDUCTOR DEVICES

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by

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LIST OF SYMBOLS

2θ	Dini-action Angles
Å	Angstrom
a	Lattice Parameter
A_G	Capacitor area (cm^2)
C	Capacitance
Cm	Centi meter
C_{ox}	Oxide capacitance (pF)
D	Crystallite size (nm)
d	lnterplanar Spacing
E^d_g	Direct Bandgap
E_g	Energy Bandgap
E^{id}_g	Indirect Bandgap
ε	Microstrain
ε_o	Permittivity or free space
hkl	Miller indices
hν	Energy of photon
I	Current (A)
J	Current density (A cm^{-2})
K	Dielectric constant
nm	Nanometer
q	Electronic Charge
T	Temperature
t	Time
T_{hkl}	Coefficient of texture
t_{TOT}	Total Oxide Thickness

V_g	Gate voltage
δ	Dislocation Density
λ	Wavelength
μm	Micrometre

LIST OF ABBREVIATIONS

a.u	Arbitrary unit
AFM	Atomic Force Microscopy
Al	Aluminium
Ar	Agon Gas
CH_3COOH	Acetic acid
CH_3OH	Methanol
C-V	Capacitance- Voltage
DFT	Density functional theory
EDX	Energy dispersive X-ray electron microscopy
eV	Electron volt
FESEM	Field Emission Scanning Electron Microscopy
FG	Forming Gas
ICCD	International conference for diffraction data
I-V	Current-Voltage
MEA	Monoethanolamine
MOD	Metal-Organic Decomposition
MOS	Metal-Oxide-Semiconductor
N_2	Nitrogen Gas
O_2	Oxygen Gas
PDA	Post-Deposition Annealing
PL	Photoluminescence Spectroscopy
RCA	Radio Corporation America
RMS	Root-Mean-Square
RT	Room temperature
Si	Silicon

SiO_2	Silicon oxide
UV-Vis	Ultraviolet-visible spectroscopy
XRD	X-Ray Diffraction Analysis
XRR	X-Ray Reflectivity

SINTESIS HIJAU NANOSTRUKTUR CeO_2 ATAS CeO_2 DAN CeO_2 DIDOPKAN Eu SEBAGAI LAPISAN PEMPASIFAN BAGI PERANTI LOGAM-OKSIDA-SEMIKONDUKTOR BERASASKAN SILIKON

ABSTRAK

Penyelidikan ini membentangkan sintesis hijau nanostruktur serium oksida (CeO_2) menggunakan ekstrak daun *P. amaryllifolius* yang dimendapkan pada CeO_2 dan CeO_2 didopkan Europium (Eu^{3+}) sebagai lapisan pempasifan untuk peranti logam-oksida-semikonduktor (MOS) berasaskan silikon. Kesan penambahan monoethanolamine (MEA) dan lapisan benih CeO_2 bagi pertumbuhan nanostruktur CeO_2 telah disiasat. Penemuan mendedahkan bahawa lapisan benih CeO_2 memainkan peranan penting dalam menghasilkan ketumpatan arus bocor (J) yang lebih rendah (~ 2.5 x 10^{-6}A cm^{-2} pada voltan get (V_g) = 2V) apabila dibandingkan dengan penambahan MEA disebabkan oleh peningkatan keadaan kaya oksigen dalam sampel-sampel CeO_2 oleh lapisan benih. Kesan suhu penyepuhlindapan pasca pemendapan (600, 700, 800, 900 ℃) dan ambien (nitrogen-oksigen-nitrogen, gas membentuk-oksigen-gas membentuk, dan argon-oksigen-argon) ke atas struktur, morfologi, optik, dan ciri elektrik lapisan benih CeO_2 dan Eu^{3+} didopkan CeO_2 telah dikaji. Pengoptimuman penemuan menunjukkan bahawa ciri J-V_g yang lebih baik telah dicapai pada 800℃ tanpa mengira ambien manakala penggunaan nitrogen-oksigen-nitrogen mengatasi ambien lain kerana pempasifan nitrogen untuk mengurangkan pembentukan silikon dioksida berpemalar dielektrik rendah (*k*) pada antara muka CeO_2/Si. Pertumbuhan nanostruktur CeO_2 pada 1 lapisan benih CeO_2 yang mengatasi sampel-sampel lain yang mempunyai 3, 5, dan 7 lapisan telah mencapai keputusan yang baik dari segi nilai *k* yang tinggi (16.19), jurang jalur langsung yang besar (3.98

eV), J yang rendah iaitu 5.07 x 10^{-11} A cm^{-2} pada V_g = 5V serta voltan medan kekuatan yang tinggi (12.82 V). Penggunaan lapisan benih CeO_2 yang didopkan Eu^{3+} untuk pertumbuhan nanostruktur CeO_2 walaupun telah menunjukkan pencapaian nilai *k* yang lebih tinggi (16.91) dan jurang jalur langsung yang lebih besar (4.20 eV), ciri J-V_g yang sepadan adalah tidak sebaik sampel nanostruktur CeO_2 yang ditumbuhkan pada lapisan benih CeO_2 disebabkan kewujudan kepekatan perangkap perlahan yang lebih tinggi dalam sampel yang akan mewujudkan laluan arus bocor dan membawa kepada kerosakan awal peranti. Penjelasan terperinci berkaitan prestasi sampel-sampel yang disiasat terhadap kebolehlaksanaan untuk berfungsi sebagai lapisan pempasifan bagi peranti MOS berasaskan Si telah dibentangkan dalam tesis ini.

GREEN SYNTHESIZED CeO_2 NANOSTRUCTURES ON CeO_2 AND Eu DOPED CeO_2 AS PASSIVATION LAYER FOR SILICON BASED METAL-OXIDE-SEMICONDUCTOR DEVICES

ABSTRACT

This research presented a green synthesis of cerium oxide (CeO_2) nanostructures using *P. amaryllifolius* leaves extract deposited on CeO_2 and Europium (Eu^{3+}) doped CeO_2 as passivation layer for silicon-based metal-oxide-semiconductor devices. The effects of adding monoethanolamine (MEA) and CeO_2 seed layers for the growth of CeO_2 nanostructures were investigated. Findings revealed that CeO_2 seed layers played an important role in yielding a lower leakage current density (J) (~ 2.5 x 10^{-6} A cm^{-2} at gate voltage (V_g) = 2V) when compared with MEA addition due to the improvement of oxygen-rich condition in the CeO_2 samples by the seed layers. The effects of post-deposition annealing temperature (600, 700, 800, 900˚C) and ambient (nitrogen-oxygen-nitrogen, forming gas-oxygen-forming, and argon-oxygen-argon) onto structural, morphological, optical, and electrical characteristics of CeO_2 and Eu^{3+}-doped CeO_2 seed layers were studied. Optimisation of the findings showed that a better J-V_g characteristic was achieved at 800˚C regardless of ambient while the use of nitrogen-oxygen-nitrogen outperformed other ambient because of the passivation of nitrogen to reduce the formation of low dielectric constant (*k*) silicon dioxide at the CeO_2/Si interface. The growth of CeO_2 nanostructures on 1 layer of CeO_2 seed layer surpassing other samples having 3, 5, and 7 layers has attained good results in terms of a high *k* value (16.19), a large direct bandgap (3.98 eV), a low J of 5.07 x 10^{-11} A cm^{-2} at V_g = 5V as well as large breakdown voltage (12.82 V). The employment of Eu^{3+}-doped CeO_2 seed layer for the growth of CeO_2 nanostructures though has

demonstrated the attainment of a higher *k* value (16.91) and a larger direct bandgap (4.20 eV), the corresponding J-V_g characteristic was not as good as the sample of CeO_2 nanostructures grown on CeO_2 seed layer due to the existence of higher concentration of slow traps in the sample, which would create leakage current path and led to an earlier breakdown of the device. Detailed explanation pertaining to the performance of investigated samples towards the feasibility to serve as passivation layer for Si-based MOS devices was presented in this thesis.

CHAPTER 1

INTRODUCTION

1.1 Overview

The semiconductor industry relies heavily on silicon (Si) as the main material for making electronic devices, such as Si-based metal-oxide semiconductor (MOS) devices. These devices have improved the semiconductor industry by using thermally grown silicon dioxide (SiO_2) as a passivation layer that could reduce leakage current of the devices (Robertson & Wallace, 2015). However, thermally grown SiO_2 has become a problem in recent years because its thickness has decreased (El Amrani et al., 2019), leading to a very high leakage current due to the direct tunnelling mechanism (Quah et al., 2010). To solve this problem and increase the reliability of Si-based MOS devices, high dielectric constant (*k*) materials were proposed in lieu of the thermally grown SiO_2. These materials could achieve higher capacitance with the same physical thickness as the SiO_2 passivation layer (Chiu & Chang, 2014). The downsizing of Si-based MOS devices and the limitations of using SiO_2 as the passivation layer have prompted the search for alternative high *k* materials (Devaray et al., 2022), such as hafnium oxide (HfO_2) (Fu et al., 2011), zirconium oxide (ZrO_2) (Kumar et al.,2016), aluminium oxide (Al_2O_3) (Koslowski et al.,2016), yttria oxide (Y_2O_3) (Alarcon-Flores et al., 2006) , lanthanum aluminate ($LaAlO_3$) (Li & Robertson, 2012), hafnium silicate ($HfSiO_4$) (Lok et al., 2017), zirconium silicate ($ZrSiO_4$) (Yoshiasa et al., 2021) and strontium titanate ($SrTiO_3$) (Jan et al., 2020) as the alternatives to SiO_2 in recent decades.

1.2 Problem Statement

Cerium oxide (CeO_2), a rare-earth oxide, attracted attention as a replacement for SiO_2 as a passivation layer for Si-based MOS devices due to its intriguing features such as high *k* values (~23–26), large bandgap (~3.0-3.6 eV), high dielectric breakdown strength (~2.6 MV cm1), high refractive index (~2.2–2.8), large conduction band offset with Si (~ 1.48 eV), and high thermal and chemical stability on Si substrate (Chen et al., 2013). Moreover, CeO_2 has a small mismatch (0.35%) with Si and a low interface-state density (~10^{11} cm^{-2} eV^{-1}) (Agrawal et al., 2017; Chiu & Chang, 2014; Chiu & Lai, 2010; Sapkota et al., 2020 ; Quah et al., 2010; Vangelista, 2017). Although CeO_2 in particular has garnered a great deal of interest because of the low reduction potential and co-presence of Ce^{3+}/Ce^{4+} on their surfaces, the interchangeability of the 4+ and 3+ valence states of the cerium ions result in oxygen vacancies within the CeO_2, which would be deemed to bring unfavorable results as a passivation layer for MOS devices (Bera & Anandan, 2014). The reduction of the cerium ions facilitates the hopping of electrons from a Ce^{3+} to an adjacent Ce^{4+} ion. This reduction would assist in enhancing the conductivity as well as contributing to the reduction of bandgap (Xiong et al., 2010 ; Pfau & Schierbaum, 1994). Moreover, the formation of oxygen vacancies coupled with the reduction process would encourage the diffusion of more oxygen into the interface to react with the underlying Si substrate to form low *k* SiO_2 interfacial layer. In addition to the oxygen vacancy induced diffusion, the high temperature annealing in an oxidizing ambient with prolonged annealing time would also be found to cause the formation of a low *k* interfacial layer. The formation of interfacial layer could be challenging as the low *k* SiO_2 interfacial layer could reduce the overall *k* value, thereby nullifying the objectives of using a high *k* CeO_2 passivation layer (Nishikawa et al., 2002). Therefore, it is

necessitated to find an alternative approach to improve the properties of CeO_2 on the perspective of the passivation layer for Si-based MOS devices.

Therefore, focus was shifted to doping CeO_2 with divalent and tetravalent cations to exploring trivalent doping as a potential passivation layer for Si-based MOS devices (Patil et al., 2016). Researchers have found that doping CeO_2 with divalent or tetravalent cations would increase reducibility of CeO_2, and bandgap while enhancing its conductivity. This made the divalent or tetravalent doped CeO_2 less suitable as passivation layers for MOS devices (Harish et al., 2018). Density functional theory (DFT) studies have revealed that divalent cations would generate oxygen vacancies and alter atomic structure, leading to bandgap reduction (Kehoe et al., 2011). Similarly, tetravalent cations doping resulted in structure distortion, Ce^{4+} reduction, oxygen vacancy generation, and increased conductivity. However, these results were not considered promising for passivation of MOS device (Maeng et al., 2014). Therefore, researchers have shifted their focus to trivalent CeO_2 doping as a potential passivation layer for MOS devices (Keating et al., 2013). The effects of incorporating trivalent metal cations (specifically gadolinium (Gd^{3+}), yttrium (Y^{3+}), lanthanum (La^{3+}), samarium (Sm^{3+}), neodymium (Nd^{3+}), and gallium (Ga^{3+})) as dopants into the lattice structure of CeO_2 whereby the reduction of the CeO_2 phase would be impeded since the energy needed to incorporate these trivalent metal cations into the lattice was lower than the energy required to form oxygen vacancies. (Zhang et al., 2011). The incorporation of Yb^{3+} and Gd^{3+} into the CeO_2 lattice was said to produce a better passivation layer, reducing leakage current density and enabling a higher k value compared to pure CeO_2 (Pan et al., 2017). This improvement in electrical properties was attributed to a decrease in leakage current and an enhancement in dielectric breakdown voltage (Andersson et al., 2007). This was caused by the trivalent metal

cations incorporated into the cubic fluorite structure of CeO_2 (Kumar et al., 2016). The trivalent cations and oxygen vacancies would create columbic forces that would render the sites inactive for oxygen diffusion (Yamamura et al., 2008). Due to increased interfacial polarization, the addition of trivalent cations increased the *k* value of CeO_2. For example, La^{3+} doping of CeO_2 has demonstrated a high *k* and reduced electrical conductivity, with low leakage current and improved insulation behaviour (Khairnar & Mahajan, 2013). Similarly, doping with Y^{3+} and Gd^{3+} cations were found to enhance insulating behaviour of CeO_2 and reduce electrical conductivity (Zhang et al., 2011). These results suggested that trivalent doping, such as Europium (Eu^{3+}) doping, could benefit CeO_2 films (Farrukh et al., 2019), of which Eu^{3+} doping has shown promise in optoelectronic devices in the aspects of reducing oxygen vacancies and leakage current in the ferroelectric bismuth titanium oxide ($Bi_4Ti_3O_{12}$) and zirconium oxide (ZrO_2) films (Khairnar & Mahajan, 2013) as well as increasing bandgap (Yamamura et al., 2007). Notwithstanding the above, there remains the challenge to synthesize high purity crystalline films via a facile and non-toxic approach (Kovacevic et al., 2016). Conventional wet chemistry techniques would require the use of precursor chemicals, pretreatment of the solution, and growth inhibitors, which can lead to surface defects and undesirable gate leakage current and interface trap density during deposition (Pandit et al., 2019). Various deposition methods were explored for CeO_2, including electron beam evaporation (Inoue & Shida, 2014), ion beam sputtering, spray pyrolysis, reactive sputtering, metal-organic decomposition (MOD), and pulse laser deposition (Balakrishnan et al., 2011).

In this research, the use of a green synthesis method using *Pandanus amaryllifolius* extract as environmentally friendly stabilizing agent to mediate CeO_2 nanostructures extract for potential incorporation as passivation layer for Si-based

MOS devices was implemented. The addition of monoethanolamine (MEA) as a stabilizer in the synthesis process was expected to improve the crystallinity and transparency of CeO_2 nanostructures. This has not been previously documented for MOS applications. Moreover, this research presented a facile approach to investigate the synthesis of multiple layers of CeO_2 films spin-coated onto Si substrates and subjected to post-deposition annealing at different temperatures (600, 700, 800, and 900°C) under mixed gases ambient. Additionally, this study attempted to take full advantage of the beneficial effects of nitrogen-oxygen-nitrogen, forming gas-oxygen-forming gas and argon-oxygen- argon by adopting novel ambiance during post-deposition annealing for Eu^{3+}-doped CeO_2 films for Si-based MOS devices, which has not previously been reported. Overall, this work represented an innovative investigation into the utilization of CeO_2 and Eu^{3+}-doped CeO_2 films as the seed layers to assist the overgrowth of CeO_2 nanostructures, aiming to improve passivation Si-based MOS devices.

1.3 Objectives

The principal objective of this research was to produce CeO_2 nanostructures using green synthesis method on Si substrates, and of which could be potentially used as a passivation layer for Si-based MOS devices. In order to achieve this principal objective, the following specific objectives are to be achieved:

i) To investigate the synergistic effects of monoethanolamine (MEA) and post-deposition calcination on green synthesized CeO_2 nanostructures spin-coated on Si substrates.

ii) To investigate the effects of post-deposition annealing temperature and ambient conditions on the structural, morphological, optical, and

electrical properties of CeO_2 and Eu^{3+}-doped CeO_2 films spin-coated on Si substrates.

iii) To investigate the incorporation of CeO_2 and Eu^{3+}-doped CeO_2 films as seed layers for the overgrowth of green synthesized CeO_2 nanostructures on Si substrates.

1.4 Scope of the Study

In this research, an investigation of the synergistic effects of monoethanolamine (MEA) and post-deposition calcination on green synthesized CeO_2 nanostructures spin-coated on Si substrates was conducted, as well as the incorporation of a CeO_2 seed layer for the overgrowth of CeO_2 nanostructures synthesized on Si substrates. This study also explored the effects of post-deposition annealing at different temperatures under mixed nitrogen and oxygen gas conditions onto CeO_2 films as well as the effects of varying the ambient gases onto Eu^{3+}-doped CeO_2 films on Si substrates to examine the corresponding effects on structural morphological, optical and electrical properties of the films. Additionally, the green synthesized CeO_2 nanostructures were deposited on the CeO_2 and Eu^{3+}-doped CeO_2 films to study and compare the characteristics amongst the CeO_2 nanostructures with and without the presence of seed layers.

1.5 Outline of Thesis

This thesis was divided into five chapters. The background, problem statement objectives, and scope of study were presented in Chapter 1. Chapter 2 presented an in-depth review of the background studies and theories. Chapter 3 described methodology, raw materials and design of experiment. Chapter 4 discussed the

findings and results of the research conducted using different characterization techniques. Chapter 5 summarized key outcomes from the research along with future recommendations.

CHAPTER 2

THEORETICAL BACKGROUND AND LITERATURE REVIEW

2.1 Introduction

Silicon (Si)-based metal-oxide-semiconductor (MOS) devices are one of the most important and commonly used components, which has fuelled the revolution in the semiconductor industry over the years. Consequently, MOS technology has played an unparallel role in the development of integrated circuits and has enabled the fabrication of faster, smaller, and more energy-efficient electronic devices. Furthermore, advancements in Si-based MOS technology helped the astonishing transformation of communicative systems through the development of compact, energy-efficient devices capable of handling advanced communication protocols. In addition, the Si-based MOS devices were found relevance in different fields such as sensors, memory devices, biomedical, alternating current (AC)/ direct current (DC) converters, amplifiers, and automobiles. The success of Si-based MOS devices was mainly due to the availability of thermally grown silicon dioxide (SiO_2) as a passivation layer, which possessed superior properties such as low defect density ($<10^{10}$ eV^{-1} cm^{-2}), a high bandgap (9 eV), and a large band offset (4.5 eV) with the Si substrate (Tuttle, 2004).

However, the SiO_2 passivation layer later encountered reliability issues as the thickness of the passivation layer was trimmed down immensely. Diverse high dielectric constant (k) materials, such as hafnium oxide (HfO_2), cerium oxide (CeO_2), zirconium oxide (ZrO_2), lanthanum oxide (La_2O_3), gallium oxide (Ga_2O_3), and samarium oxide (Sm_2O_3) have been considered as the probable contenders for reinstating SiO_2 as the passivation layer for MOS devices (Agrawal et al., 2017 ;

Bahari & Gholipur, 2013 ; El-Raheem et al., 2015 ; Kaya et al., 2017 ; Kitayama et al., 2011 ; Patil et al., 2016). Among the probable candidates, CeO_2 emerges as the front runner to be employed as the high *k* passivation layer for the Si-based MOS devices due to its admirable properties, which include *k* value of 26, wide bandgap (6 eV), high dielectric strength (25 MV cm^{-1}), low lattice mismatch with Si, as well as high refractive index (2.2-2.8) (Quah et al., 2010 ; Bera and Anandan 2014 ; Chiu et al., 2008; Kim et al., 2011; Park et al., 2019).

An introduction to nanostructured films as high *k* material, with a focus on CeO_2 nanostructure, and subsequently background work on low *k* materials as well as the transition from low *k* to high *k* materials was presented. Moreover, the properties and applications of CeO_2 and doped CeO_2 films, followed by synthesis methods for CeO_2 nanostructures with a focus on green synthesis, were reviewed and discussed. An introduction to monoethanolamine (MEA) and its effect on nanostructure was also presented. Towards the end of this chapter, employment of CeO_2 and doped CeO_2 films as seed layers and their applications for overgrowth of nanostructure were presented.

2.2 Nanostructured Films as High Dielectric Constant (*k*) Materials for Silicon-based Metal-Oxide-Semiconductor (MOS)

MOS devices are two terminal devices having a metal gate and substrate contact, as represented in the Figure 2.1. The oxide layer, in typical being shown as SiO_2 in the figure, has been used as the nanostructured films in two-dimensional (2D) to provide passivation for semiconductor substrates, which in turn would assist in control of voltage by metal gate. Moreover, excellent insulation between the metal gate and semiconductor substrate is also provided by the oxide layer to achieve low leakage current off the MOS devices. Previous studies have highlighted the significance of the

2D nanostructured films, which included SiO_2 as the low *k* passivation layer for Si-based MOS devices as well as other high *k* passivation layers that were emerging with regards to obtaining good electrical properties. Although the potential of the 2D nanostructured films is immense, the exploration in term of employing the nanostructured films for subsequent growth of nanostructures, and potentially used as the next generation high *k* passivation layer remains scarce. Hence the feasibility of such approach was explored systematically.

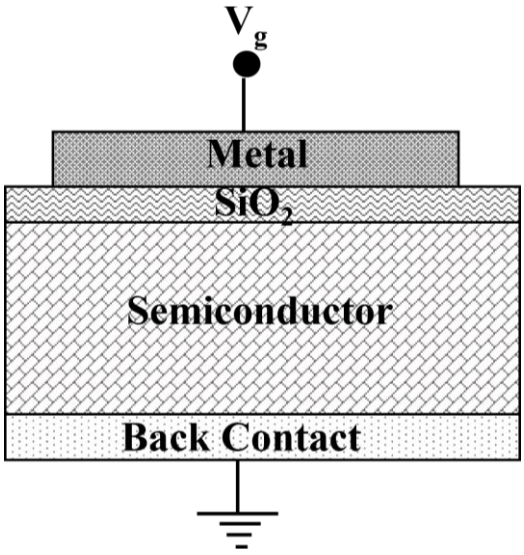

Figure 2.1 Typical MOS structure possessing metal electrode, oxide layer, and semiconductor substrate (Kahraman & Yilmaz, 2020).

2.2.1 Development of Gate Oxide as Passivation Layer for Silicon

The relentless scaling of Si-based MOS devices has been critical in achieving high performance electronics at a reasonable cost (Del Alamo, 2011). This scaling was governed by the renowned Moore's law (Lundstrom & Alam, 2022), which stated that the number of transistors on a single chip would double every two to three years. The incorporation of billions of transistors as a result of continued scaling over the years on a single Si chip has resulted in faster processing speed, high storage capacity, and low power consumption (Van, 2022). However, as the downscaling of Si-based MOS

continued to be implemented in order to meet stringent market requirements, the beneficial effect of using SiO_2 as the passivation layer for the Si-based MOS devices could be shattered. In fact, the passivation layer should provide excellent electrical solation between metal gate as well as semiconductor substrate. However, the continuous downscaling would push the SiO_2 to its thickness limitation whereby the electrons could tunnel through the thin (< 1 nm) SiO_2 passivation layer (Figure 2.2) and increased the leakage current as well as reliability issues (Kumar & Rao, 2011). Moreover, the control over the channel region (Figure 2.2) by the gate material was no longer stable due to the barrier potential lowering effect induced by the scaling of the SiO_2 passivation layer, which would induce drain current to modulate the channel region (Demarteau, & Roelofs 2014). Figure 2.2 presents a schematic diagram of typical p channel metal-oxide-semiconductor field effect transistor (MOSFET) using n-type Si substrate and SiO_2 passivation layer (Mendiratta & Suman, 2020).

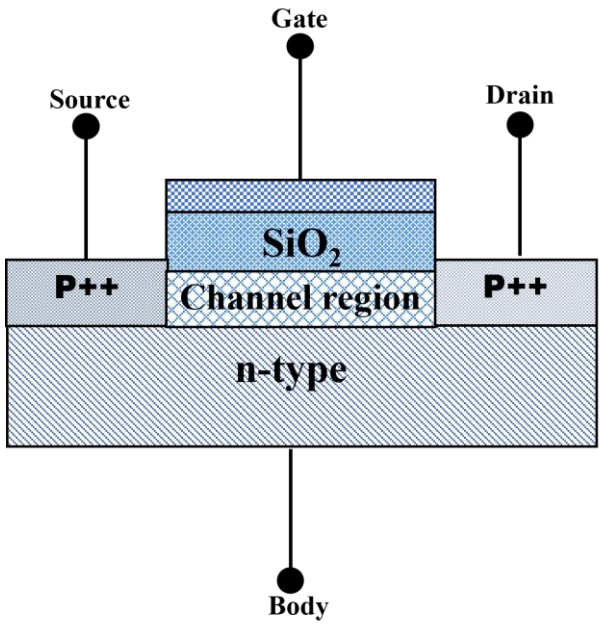

Figure 2.2 A schematic diagram of typical p channel MOSFET using n-type Si (Wang & Tsui, 2013).

2.2.1(a) The State-Of-The-Art Silicon Dioxide (SiO_2)

Silicon dioxide (SiO_2) has long been used as the native oxide for Si due to the excellent passivation provided by the thermally grown SiO_2.The thermally grown SiO_2 has shown high degree of growth control in passivating the Si surface. Consequently, the interface traps and fixed charges were considerably low to provide excellent device performance. The initial achievement of Si-based MOS devices was a result of the presence of thermally generated native SiO_2 as a passivation layer. In order to ensure optimal performance of produced devices, it is crucial to have a passivation layer of superior quality that has a low density of interface traps. From 1957 until recently, Si-based MOS capacitors have effectively utilised thermally generated SiO_2 as the main passivation layer, with the thickness of SiO_2 decreasing in each subsequent iteration. In addition to its passivation qualities, this layer also offers exceptional electrical isolation between the metal gate and the semiconductor substrate, hence reducing leakage current to a minimum. SiO_2 has a band gap of around 9 eV and forms a very favourable contact with the Si substrate, which is characterised by a very small number of interface traps. Due to the beneficial combination of SiO_2/Si, Si-based semiconductor technology has achieved significant achievements. Furthermore, SiO_2 is commonly used as a passivation layer to protect different electronic devices from the surrounding environment and packaging processes.

Prior research on SiO_2 passivated Si MOS capacitors demonstrated encouraging findings about a reduced leakage current of around 10^{-12} A cm^{-2} (Jiang, 2004), which was lower than that of the Si substrate (~10^{-8} A cm^{-2}) at 6 MV/cm (Yen & Lee, 2014). Nevertheless, as the continuous reduction in size of the SiO_2 passivation layer continues in line with Moore's law, there have been documented instances of degradation in the MOS properties. Prior results suggested that when exposed to a gate

voltage of around 1 V, the leakage current would undergo a shift from 1 x 10^{-12} A cm^{-2} at a thickness of 3.5 nm to 1 x 10^{-12} A cm^{-2} at 1.5 nm (Banerjee et al., 2011 ; Maestre et al., 2010). This observed phenomena indicated a significant twelve-fold increase in the amount of leakage current when the thickness falls by a factor of two. The rapid growth in leakage current raised serious concerns about the amount of power consumed during standby, the dependability of MOS devices, and their lifespan. This ultimately limited the effectiveness of the SiO_2 passivation layer when its thickness was less than 1.5 nm. However, as the device dimension has decreased, SiO_2 has been confronted with a high leakage current issue (Suñé et al., 2000), originating from the relatively thin SiO_2 thickness that would favour direct tunnelling of the electrons over a potential barrier height (Register & Yang, 1999), as represented in Figure 2.3, wherein E_{FM}, V_g, E_C, E_v, and E_F stands for metal fermi level, gate voltage, conduction band, valance band, and semiconductor fermi level, respectively. Moreover, the increment in the leakage current would induce additional heat and higher power consumption challenging the feasibility of the fabricated devices.

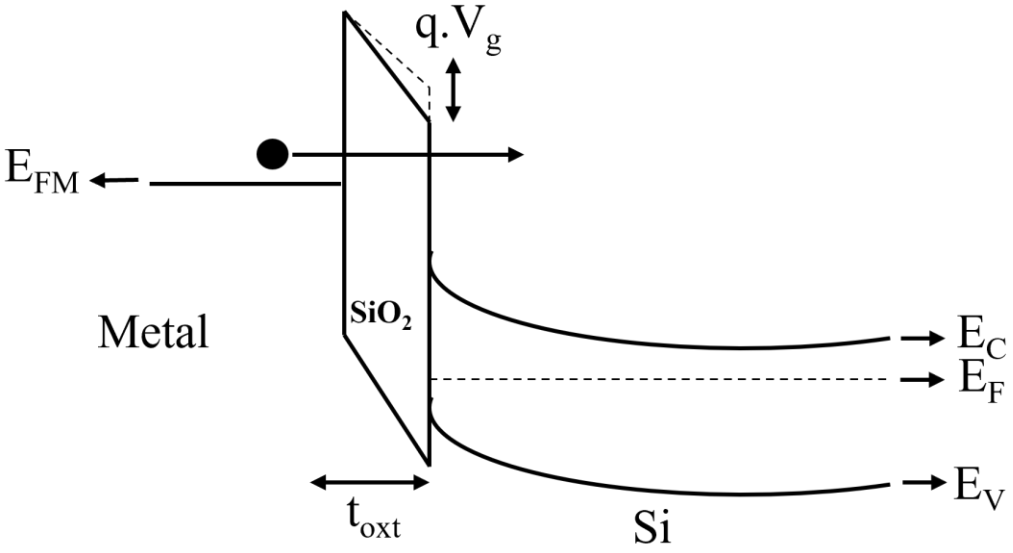

Figure 2.3 A schematic diagram showing the occurrence of direct tunneling of electrons through the triangular potential barrier (Thriveni & Ghosh, 2019).

The direct tunnelling through a potential barrier would cause significant leakage current, which could cause circuit instability and excessive power dissipation, leading to a high likelihood of dielectric breakdown. Subsequent studies introduced the addition of nitrogen to SiO_2 to form oxynitrides and nitride/oxide stacks, which were proposed to address these problems (Hegde et al., 1995). These materials were able to provide better passivating characteristics in terms of a higher *k* value (>3.9) than that of SiO_2 (*k*= 3.9) (Tanner et al., 2007), reduced leakage current, and improved reliability. Previous investigations showed that silicon oxynitride thermally grown at 1100°C under nitrous oxide (N_2O) ambience for 60 s and subsequent rapid thermal processing at 1100°C in nitrogen ambience have contributed to the accumulation of nitrogen at the interface. Consequently, the accumulated nitrogen was able to improve interface quality by passivating Si dangling bonds and reducing interface traps (Hwang et al., 1990). Another study reported the suppression of radiation-induced neutral and positive charge buildup in the thermally grown oxynitride passivation layer after annealing at 1000℃ in nitric oxide (NO) ambience for 100 s, which was subsequently subjected to rapid thermal processing (RTP) at 1000℃ under NO ambience for 80 s (Bhat et al., 1995). Moreover, a significant increment in the breakdown field strength by reducing the leakage current was also consistently reported (Ueng et al., 1995).

There was a comparison of the dielectric characteristics of several materials deposited via RF magnetron sputtering. The compound SiO_2 exhibited a *k* value of 3.9, a bandgap of 9 eV, and a band offset of 3.2 eV. According to Robertson 2004, the SiO_2 layer had a measured thickness of 1.4 nm, while the leakage current density was around $1x10^{-7}$ A cm^{-2} at an applied voltage of 1 V (Robertson, 2004). The compound SiON exhibited a comparatively higher *k* value of ~3.9-7.8 (Wong & Iwai, 2006), [a bandgap ranging from 7.8 - 9 eV, and a band offset ranging from 1.5 - 2 eV. The SiON layer

exhibited a range of thicknesses spanning from 25 - 200 nm, while the leakage current density at 1 V was found to be approximately $1x10^{-7}$ A cm^{-2}, similar to that observed in SiO_2. The SiON layer was formed at a temperature of 400°C under a nitrogen environment, as reported by Ma et al. (2018), King and Mays (2014).

2.2.2 High *k* Material as Alternative Passivation Layers for Silicon

Regardless of numerous efforts to improve potential of SiO_2 as the passivation layer for Si-based MOS devices, the relatively low *k* of SiO_2 nor SiON remained irrelevant to assist the achievement of breakthrough for Si-based MOS devices in the era of device miniaturization. Therefore, it is critical to replace SiO_2 as the passivation layer for MOS devices with a material having a *k* value greater than that of SiO_2. Since the *k* value of SiO_2 is 3.9, any material having a *k* value greater than 3.9 could be considered as a high *k* material. The employment of high *k* material as a passivation layer would circumvent the above-mentioned issues of leakage current and reliability while maintaining the continuous scaling of MOS devices. This scenario would be best understood based on the following equation:

$$C_{ox} = \frac{k\varepsilon_0 A_G}{d} \qquad (2.1)$$

where C_{ox}, k , A_G, ε_0 , d is the oxide capacitance, dielectric constant, area of metal contact, permittivity of free space (8.854 x 10^{-12} F/m) and the total oxide thickness. According to Equation 2.1, as SiO_2 was replaced by materials having a *k* value higher than SiO_2, the capacitance could be kept the same with a physically thicker high *k* passivation layer. This would minimise the leakage current issue occurring through the direct tunnelling mechanism as represented in the Figure 2.4.

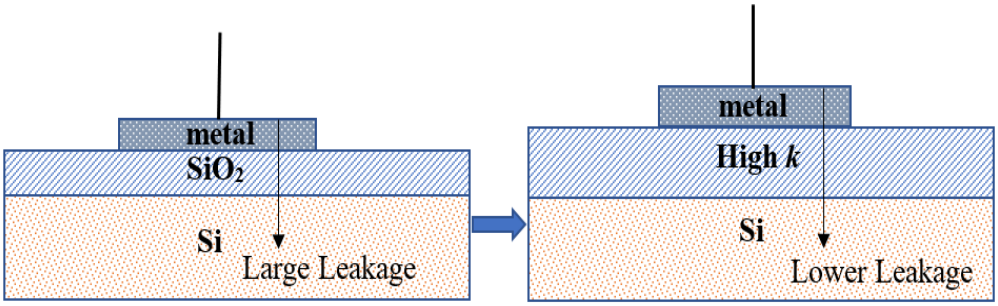

Figure 2.4 A schematic diagram of leakage current reduction with the replacement of SiO_2 passivation layer by high *k* materials (Sakshi & Singh, 2016).

One way to overcome the limitation of low *k* SiO_2 was to use thicker high *k* oxide materials as the alternative passivation layers. High *k* oxide materials could offer higher capacitance than SiO_2 passivation layer at the same physical thickness. There are different approaches to identify potential high *k* oxides. Robertson suggested several criteria for selecting new oxide candidates (Robertson, 2004; Robertson & Wallace, 2015) as follow.:

i) High *k* value (>3.9).

ii) Wide enough bandgap (>3 eV) and band offset (>1 eV) to minimise leakage current.

iii) Thermodynamically stable with Si substrate.

iv) Good interface quality with the Si substrate.

v) Minimum lattice mismatch with the Si substrate.

The high *k* oxide should have a *k* value greater than SiO_2 (k= 3.9). The high *k* candidate should also be thermally stable at high processing temperature up to 1000°C. This was a key issue to control the electrical properties of the MOS devices (Wilk et al., 2001). Schlom et al. (2008) also stated that the oxide should be thermodynamically stable with the underlying substrate material to avoid the formation of thick SiO_2

interfacial layer that would create electrical interface with Si. Moreover, the oxide should have good insulator properties to minimize carrier injection and probability of current direct tunneling into its layer. Many studies have been conducted on using high *k* oxide materials to replace SiO_2 for MOS based devices. Diverse high *k* materials, such as zirconium oxide (ZrO_2) (Singh et al., 2021; Kondaiah et al.,2020), hafnium oxide (HfO_2) (Seo et al., 2020; Kahraman &Yilmaz, 2020), yttrium oxide (Y_2O_3) (Kim et al., 2021; Lee et al., 2019), aluminium oxide (Al_2O_3) (Uenuma et al., 2018; Lee et al., 2019; Ren al., 2018), cerium oxide (CeO_2) (Abdul Shekkeer et al., 2022; Tan et al., 2022; Shin et al., 2019; Wang et al., 2022; Zhang et al., 2014), tantalum oxide (Ta_2O_5) (Thapliyal & Mohan, 2021; Kumar et al., 2019; Sahoo et al., 2023), lanthanum aluminium oxide ($LaAlO_3$) (Choi et al., 2022; Huang et al., 2022), and hafnium silicate ($HfSiO_4$) (Lok et al.,2017; Kahraman & Yilmaz, 2020; Kahraman et al., 2021; Bhanu et al., 2021; Carey et al., 2017) have been investigated as the probable contenders for reinstating SiO_2 as the passivation layer for MOS devices. A comparison of performance displayed by using the various high *k* materials was summarized in Table 2.1.

Table 2.1 High *k* Materials used as Passivation Layers for Si-based MOS Devices reported in the Literature and Their Performance.

Material	Deposition Technique	Post-Deposition Annealing (PDA)	*k* Value	Bandgap (eV)	Band Offset (eV)	Thickness (nm)	Leakage Current Density (A/cm^2)	References
ZrO_2	RF sputtering	PDA (500°C); 1 h	39.2	5.8	1.4	40-80	1.28×10^{-6} at 1 V	Kahraman et al., 2020
	RF sputtering	PDA (500-1000°C); 20 min; N_2	18.22	5.8-7.8	1.4	5	1×10^{-6} at 10.7 MV/cm	Wong & Cheong, 2013
HfO_2	RF sputtering	PDA (420°C) ; 20 min; 96% N_2-4% H_2	22.47	5.68	-	9.45	9.12×10^{-6} at 1 V	Tirmali et al., 2011
	RF sputtering	PDA (350-750°C); 20 min; N_2	8.06-9.44	5.8	-	35.38	3.39×10^{-9} at 1.5 V	Khairna and Mahajan, 2013
Y_2O_3	RF sputtering	PDA (500-700°C); 20 min; N_2	14-16	6	2.3	9	2.6×10^{-6} to 4.9×10^{-6} at 1V	Daso and Biswas 2011
	RF sputtering	PDA (200-1000°C); 30 min; Ar	6-11.5	5.5	1.97		1×10^{-8} at 10.7 MV/cm	Quah and Cheong 2012
Al_2O_3	Metallorganic Chemical Vapor Deposition (MOCVD)	PDA (750°C); 15 min	8-10	6-8.8	2.8	20-30	2×10^{-7} at -5 V	Zhang et al., 2016
	Atomic Layer Deposition (ALD)	PDA (150°C)	8.3	7.3	2.1	0.5-0.8	1×10^{-7} to 1×10^{-8} at 7.3 MV/cm	Wolborski et al., 2005

Table 2.1 (Continued)

Material	Deposition Technique	Post-Deposition Annealing (PDA)	*k* Value	Bandgap (eV)	Band Offset (eV)	Thickness (nm)	Leakage Current Density (A/cm^2)	References
CeO_2	Spin-Coated	PDA (300- 400°C); 20 min; 95% N_2-5% H_2	26-39	6	2.2-2.4	60-80	1×10^{-5} at 1 V	Agrawal et al., 2017
	RF sputtering	PDA (400-1000°C); 30 min; Ar	3.74-4.66	-	-	30-40	1×10^{-9} at 1.5 V	Chuah et al., 2011
Ta_2O_5	Spin-Coated	PDA (600-1000°C); 2 min; N_2	7.86-13.2	4.3	0.35	-	1×10^{-9} to 7×10^{-9} at 3 MV/cm	Salam et al., 2003
	RF sputtering	PDA (800°C); 30 min; N_2	16-29	4.5	-	30	1×10^{-2} to 1×10^{-8} at -10 V	Cheng et al., 2012
$HfSiO_4$	RF sputtering	PDA (800°C); 30 min; N_2	11	6.5	1.8	1.8-5	1.2×10^{-6} at 1 V	Wilk and Wallace, 1999
	RF sputtering	PDA (600°C); 10 min; O_2	11	5.5	-	5	2×10^{-6} at 1 V	Wilk et al., 2000
$LaAlO_3$	RF sputtering	PDA (400-700°C); 30 min; N_2	17.5	5.6	-	1.73	7.6×10^{-5} at -1 V	Chang et al., 2009
	RF sputtering	PDA (700-1000°C); 30 min; N_2	13-27	5	-	8.5-13.3	8.3×10^{-5} at -1 V	Chang and Lee, 2008

Initial experiments on RF-sputtered ZrO_2 on Si showed promising results in terms of a *k* value of 39.2 as well as a low leakage current density of 1.28 x 10^{-6} A cm^{-2} at 1 V after being subjected to post-deposition annealing at 500℃ in air for 1 hour. Nonetheless, as the annealing ambient was switched to N_2, a substantial reduction in leakage current was observed, with a low leakage current of 1 x 10^{-6} at 10.7 MV/cm (Kahraman et al., 2020 ; Wong & Cheong, 2013). Another study reported HfO_2 as a passivation layer in which post-deposition annealing in forming gas ambient has led to a high *k* value of 22.47 and a low leakage current density of 9.12 x 10^{-6} at 1V. A subsequent study reported a sudden reduction in leakage current to 3.39 x 10^{-9} A cm^{-2} at 1 V when the annealing ambient was switched to N_2 (Tirmali et al., 2011 ; Khairna and Mahajan, 2013). These results suggested the crucial role of annealing ambient in enhancing the passivating properties, wherein N_2 plays a dominant role. Nonetheless, the key properties of Al_2O_3 later attracted the attention of researchers, whereby promising results were achieved; however, the attainment of a low *k* value around 8 to 10 as compared to other high *k* materials was deemed challenging (Zhang et al., 2016 ; Wolborski et al., 2005).

Amongst the investigated high *k* materials, rare earth oxides are promising candidates for passivating layers based on the thermodynamic data and stability on Si (Hubbard & Schlom,1996). They also have good thermal stability, high *k* (20-30), and high conduction band offset with Si. In addition, rare earth oxide with close lattice match with Si when compared with ZrO_2 and HfO_2 shows thermodynamically stable phases (Leskela & Ritala, 2006). Among the rare earth oxides, CeO_2 has attracted a lot of attention for MOS-based devices and other suitable applications, such as photocatalysis, fuel cells (Chen et al., 2013), corrosion inhibitors (Carvalho et al., 2014), gas sensors (Michel & Martinez-Preciado, 2014), and high-temperature

superconductors (Sato et al., 1997) because of its remarkable properties of high k values (~23-52), large bandgap (3.4-3.8 eV), high refractive index (~2.2-2.8), large conduction band offset with respect to Si (~ 1.48 eV), as well as high thermal and chemical stability when in contact with Si substrate.

2.3 Materials Properties of CeO_2

CeO_2, often known as ceria, is a versatile chemical compound that has wide range of applications. One of the fundamental characteristics that distinguishes. CeO_2 is its ability to undergo oxidation and reduction processes owing to the alternate between the cerium (III), Ce^{3+} and cerium (IV), Ce^{4+} states, which, allow CeO_2 to function as both an oxidising and reducing agent (Varvoutis et al., 2023) Figure 2.5. This is made possible by the ground-state electron that exists in the 4f (Xe 4f15d16s2) orbital, which allows CeO_2 to display oxidation characteristics (Wu et al., 2010). Additionally, the full unit cell (Ce_4O_8) measures 5.1 Å on an edge and is made up of eight oxygen atoms bound to the cerium atom in a face-centered cubic (f.c.c) fluorite lattice (Liu et al., 2011). In addition, crystallite nature of CeO_2 could serves as the basis for nanostructures, and polycrystallinity is more prevalent in CeO_2 nanoparticles (Xu et al., 2015). Typically, the synthesis process of CeO_2 would determine the crystallite unit, and the X-ray diffraction technique could be used to study the crystallites. Furthermore, self-assembly of CeO_2 into sheets, rods or hollow variations, which are larger structures, could be used to perform hierarchical assembly of the unit's cells into crystallites and crystallites to particles (Sayle et al., 2013).

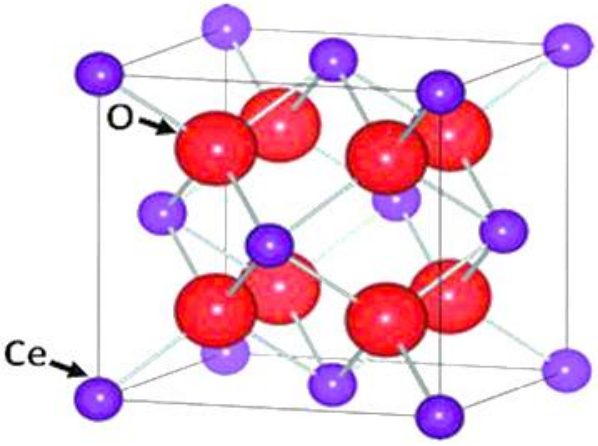

Figure 2.5 Schematic diagram showing cubic fluorite crystal structure of CeO_2 (Younis & Li, 2016).

2.3.1 Optical Properties

CeO_2 has intriguing optical characteristics, particularly in the ultraviolet (UV) portion of the electromagnetic spectrum. It is a powerful UV absorber, making it valuable in the creation of UV-blocking glass and optical filters as well as display technology (Bao et al., 2023). It could also be utilised as a dopant in semiconductor and optoelectronic manufacturing. As CeO_2 has a high refractive index, it can bend light at a larger angle than other materials, making it valuable in lens manufacturing (Oliveira et al., 2021). These optical properties of CeO_2, which depend on size, shape, surface, features, interaction with the outside environment, etc., are among the most fascinating and useful qualities of these materials (Singh et al., 2020). There are many applications based on optical properties of CeO_2 such as (Xie et al., 2015), sensors, imaging, display (Munirathnam et al., 2023), photocatalysis and photo-electrochemistry (Sharma & Pandey, 2021). Additionally, variations in bandgap, electrical conductivity, and saturation magnetization generate variations in the optical, magnetic, and electrical properties of nanomaterials. They are therefore useful for optoelectronic and opto-magnetic devices due to these variations. Optical properties

of CeO_2 could be examined using absorbance and fluorescence spectroscopy (Ali et al., 2018).

Numerous researchers have used ultraviolet-visible (UV-Vis) transmittance measurements to study optical properties of CeO_2 (Ilyas et al., 2022 ; Kumaran et al., 2022 ; Srinivasan et al., 2023). The interference effects and oscillations produced by the deposition of material on the substrate to form thin films would determine the UV-Vis spectra. As a result, the oscillations' amplitude would give the refractive index. CeO_2 films exhibit outstanding optical qualities, making them suitable for use in electro-optical and optoelectronic systems (Zinzuvadiya & Joshi, 2019). These films were transparent in the visible and infrared (IR) (near- and mid-) regions and have high direct current (dc) permittivity and refractive index. The refractive index readings in each study varied and fell between the ranges of 1.6 to 2.4. Also, the indirect bandgap was between 2.9 and 3.3 eV, while the direct bandgap was between 3.2 and 3.6 eV (Ullah et al., 2021). The hydroxide-mediated method produced cerium oxide nanoparticles with a 6.4 nm particle size. Additionally, research on optical properties was conducted using UV-visible absorption and fluorescence spectroscopy. Results showed that the produced CeO_2 nanostructures has a bandgap of 3.1 eV and an absorbance peak at 349 nm. The violet emission peak in the photoluminescence spectrum (PL) was owing to interface traps at grain boundaries, and the minor emission peak in the PL spectrum at 508 nm might be caused by surface defects or oxygen defects (Sharma & Pandey, 2021).

2.3.2 Electrochemical Properties

CeO_2 has remarkable electrochemical characteristics that make it advantageous in a range of applications, including energy storage and conversion, electrocatalysis,

lithium-ion batteries, electrochemical sensors, and supercapacitors, metal-oxide-semiconductor (MOS) applications (Karl Chinnu et al., 2015). One of the important electrochemical features of CeO_2 its capacity to store and release oxygen ions, which makes it useful in solid oxide fuel cells, oxygen sensors, and gas separation membranes (Li et al., 2018). CeO_2 is regarded as one of the most promising alternatives for electrode material among all these transitional metal oxides due to its special qualities, including greater thermal stability, and better oxygen storage capacity (Guo et al., 20). Galvanostatic methods were used to test the electrochemical properties of spherical crystalline CeO_2 nanostructures produced by the hydrothermal method. The results showed that the CeO_2 electrode's initial discharge capacity was 460 mA h g^{-1}, which was greater than the value of the pre-existing carbonaceous electrode. Only 7% decrease in discharge capacity was seen after 50 cycles, indicating higher cyclability (Liu et al., 2015).

The hydrothermal process was used to create hexagonal CeO_2 nanostructures, which were then investigated for their electrochemical characteristics using cyclic voltammetry, alternating current (ac) impedance spectroscopy, and charge-discharge in various neutral electrolytes (NaCl, KCl, Na_2SO_4, and K_2SO_4). The findings showed that the NaCl electrolyte had the highest capacitance, which was approximately 523 F g^{-1} at 2 mV s^{-1}. Only an 18% drop in capacitance was seen after 2000 cycles when testing for cyclability. It could be concluded that NaCl was the optimum neutral electrolyte for CeO_2 based supercapacitor electrodes, (Maheswari & Muralidharan, 2015). Moreover, CeO_2 was also being researched as a catalyst for electrochemical processes such as the oxygen reduction reaction in fuel cells and the water splitting reaction in electrolysis cells. Because of its capacity to store and release oxygen ions, as well as its redox activity, it is a potential material for these applications.