MULTIBAND CMOS POWER AMPLIFIER WITH INTEGRATED HIGH-Q COMPACT INDUCTOR FOR LORA APPLICATION

ARVIND SINGH RAWAT

UNIVERSITI SAINS MALAYSIA

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MULTIBAND CMOS POWER AMPLIFIER WITH INTEGRATED HIGH-Q COMPACT INDUCTOR FOR LORA APPLICATION

by

ARVIND SINGH RAWAT

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TABLE OF CONTENTS

ACKNOWLEDGEMENT ii

TABLE OF CONTENTS iii

LIST OF TABLES vii

LIST OF FIGURES viii

LIST OF ABBREVIATIONS xvi

LIST OF APPENDICES xix

ABSTRAK xx

ABSTRACT xxii

CHAPTER 1 INTRODUCTION 1

1.1 Introduction 1

1.1.1 Sub-GHz Frequency Band 2

1.1.2 Long Range (LoRa) Technology 3

1.2 Problem Statement 4

1.3 Research Objectives 11

1.4 Research Scope 12

1.5 Thesis Outline 12

CHAPTER 2 LITERATURE REVIEW 14

2.1 Introduction 14

2.2 CMOS Radio Frequency Power Amplifier (RFPA) 14

2.3 Types of RF Power Amplifiers 15

2.3.1 Linear Power Amplifier 16

2.3.1(a) Class-A Power Amplifier 16

2.3.1(b) Class-AB Power Amplifier 21

2.3.2 Non-Linear Power Amplifier 23

2.3.2(a) Class-B Power Amplifier 23

2.3.2(b) Class-C Power Amplifier 25

2.3.2(c) Class-D Power Amplifier 26

2.3.2(d) Class-E Power Amplifier 28

2.3.2(e) Class-F Power Amplifier 29

2.3.2(f) Class-G Power Amplifier 31

2.3.2(g) Class-J Power Amplifier 33

2.3.3 Efficiency and Linearity Trade-off in Power Amplifier 34

2.4 Efficiency Enhancement Techniques in Power Amplifier 36

2.4.1 Differential Power Amplifier 36

2.4.2 Doherty Power Amplifier 38

2.4.3 On-chip Transformer Power Amplifier 42

2.4.4 Envelope Tracking Power Amplifier 45

2.4.5 Envelope Elimination and Restoration Power Amplifier 48

2.4.6 Outphasing Power Amplifier 51

2.4.7 Hybrid Power Amplifier 55

2.5 Linearity Enhancement Techniques in Power Amplifier 56

2.5.1 Feedback Technique 57

2.5.1(a) Cartesian Feedback Technique 58

2.5.1(b) Polar Feedback Technique 60

2.5.2 Feed-forward Technique 62

2.5.3 Linear Amplification Using Non-Linear Components Technique (LINC) 64

2.5.4 Pre-Distortion Technique 66

2.5.4(a) Analog Pre-Distortion Technique 66

2.5.4(b) Digital Pre-Distortion Technique 69

2.5.5 Cascode Power Amplifier 71

2.6 Work Comparison of Recently Published CMOS PAs in Sub-GHz............. 74

2.7 CMOS Inductors 84

2.7.1 Concepts and Modelling of On-Chip Spiral Inductors 87
2.7.1(a) Series Inductance (Ls) 89
2.7.1(b) Quality Factor (Q- Factor).. 90
2.7.1(c) Series Resistance (Rs) 92
2.7.1(d) Capacitance (C) 93
2.7.2 Different Shapes and Types of On-Chip Spiral Inductors 93
2.8 Summary 97
CHAPTER 3 METHODOLOGY 98
3.1 Introduction 98
3.2 Research Flow-Chart 98
3.3 Design Specifications of Multiband CMOS Power Amplifier for LoRa Applications 102
3.4 Design of a Novel Geometry, High Q-Factor Compact Inductor (HQCI) .. 103
3.4.1 Mathematical Expressions for the Inductance and Q-Factor of HQCI 106
3.4.2 Comparison of Performance of HQCI with other Conventional Planar Inductors 114
3.5 Design of CMOS Power Amplifier 115
3.5.1 Schematic Design of Mode Switching PA 116
3.5.1(a) Bias Circuit 119
3.5.1(b) Matching Networks... 122
3.5.1(c) Principle of Operation for Back-off Efficiency Enhancement by Mode Switching Technique 124
3.5.2 CMOS Power Amplifier with Integrated High Q-factor Compact Inductor (HQCI-PA) 125
3.6 Measurement Setup 128
3.7 Summary 131
CHAPTER 4 RESULTS AND DISCUSSIONS 132
4.1 Introduction 132

4.2 Simulation Results 132

4.2.1 Simulated Results of Novel Geometry HQCI 132

4.2.2 Simulation Results of Mode Switching Multiband CMOS HQCI-PA 134

4.3 Measurement Results 142

4.3.1 Measurement Results of Novel Geometry HQCI 142

4.3.2 Measurement Results of Mode Switching Multiband CMOS HQCI-PA 146

4.4 Summary 160

CHAPTER 5 CONCLUSION AND FUTURE RECOMMENDATIONS 162

5.1 Conclusion 162

5.2 Recommendations for Future Research 163

REFERENCES 164

APPENDICES

LIST OF PUBLICATIONS

LIST OF TABLES

Page

Table 2.1 Summary of classes of PAs and their corresponding efficiencies..... 35

Table 2.2 Performnace comparison of recent works in sub-GHz CMOS PAs....83

Table 3.1 Design specifications of CMOS PA 102

Table 4.1 Performnace comparison of proposed custom shape HQCI with other conventional inductors.. 145

Table 4.2 Measured performance summary of multiband CMOS HQCI-PA..158

Table 4.3 Performnace comparison of proposed CMOS HQCI-PA with recent works in sub-GHz frequency.. 159

LIST OF FIGURES

		Page
Figure 1.1	Application of LPWAN technologies [1]	1
Figure 1.2	Benefits of a standardized sub-GHz system [20]	4
Figure 1.3	Multiple PAs for multiband wireless system [26]	6
Figure 1.4	The trade-off between linearity and PAE of a RFPA [31]	8
Figure 2.1	Basic block level architecture of a two-stage CMOS PA [38]	15
Figure 2.2	Classification of RFPAs	16
Figure 2.3	Basic single-stage CMOS PA [65]	17
Figure 2.4	Drain current and drain voltage waveforms for ideal Class-A PA [65]	17
Figure 2.5	ST 0.13 µm CMOS Class-A PA [68]	19
Figure 2.6	Measurement results of HiVP-PA [68]	20
Figure 2.7	Configuration of a class-AB PA [69]	21
Figure 2.8	Conduction angle of a class-AB PA [69]	21
Figure 2.9	Envelope tracking PA [72]	23
Figure 2.10	Drain voltage and current waveforms in an ideal Class-B [69]	24
Figure 2.11	Configuration of a class-C PA [69]	25
Figure 2.12	Conduction angle of a class-C PA [69]	26
Figure 2.13	Configuration of a current mode class-D PA [74]	26
Figure 2.14	Waveforms of a current mode class-D PA [74]	27
Figure 2.15	Configuration of a class-E PA [69]	28
Figure 2.16	(a)Voltage waveform of a class-E PA [69]	29
Figure 2.16	(b)Current waveform of a class-E PA [69]	29

Figure 2.17 Configuration of a class-F PA with 3rd-order harmonic termination [69]……………………………………………………………. 30

Figure 2.18 (a)Voltage waveform of a class-F PA [69]…………………………. 30

Figure 2.18 (b)Current waveform of a class-F PA [69]…………………………..38

Figure 2.19 Conceptual diagram of a two-supply voltage class-G PA [82]………32

Figure 2.20 Operation waveform of the two-supply voltage class-G PA [82]……32

Figure 2.21 Efficiency comparison between conventional single-supply PA and class-G PA [82]…………………………………………………...33

Figure 2.22 Configuration of a typical class-J PA [92]………………………….. 33

Figure 2.23 The modified waveform of the class-J PA [92]………………………34

Figure 2.24 Efficiency and fundamental output power versus conduction angle [95]……………………………………………………………. 35

Figure 2.25 Non-linearity versus conduction angle [99]…………………………36

Figure 2.26 Differential PA with capacitive cross-coupling neutralization [101]. 37

Figure 2.27 Block diagram of a classic DPA [105]………………………………39

Figure 2.28 The concept of Doherty PA [105]……………………………………39

Figure 2.29 The efficiency profile of DPA [107]…………………………………40

Figure 2.30 DPA with Wilkinson divider, dephasing circuit, and impedance inverter [110]…………………...……………………......................41

Figure 2.31 (a)Series transformer combination structure [113]…………………..42

Figure 2.31 (b)Parallel transformer combination structure [113]…………...……42

Figure 2.32 (a)Configuration of interleaved transformer and (b) top view of interleaved transformer [121]………………...………………..…… 45

Figure 2.33 Autotransformer integrated PA [122]………………………………. 45

Figure 2.34 Voltage difference between supply voltage and modulated RF output signal waveform [125]…………………………………………… 46

Figure 2.35 Block diagram of the ETPA [126]………………………………….. 46

Figure 2.36 Key waveforms in an ETPA [125]………………………………….. 47

Figure 2.37 ETPA with dual-mode supply modulator [129]…………………….. 48

Figure 2.38 Key waveforms in an EERPA [125]……………………………….…. 48

Figure 2.39 Block diagram of the supply modulator [134]……………………… 50

Figure 2.40 Circuitry of the proposed mode-switching PA [134]……………….. 51

Figure 2.41 Architecture block diagram of out-phasing [136]…………………... 51

Figure 2.42 Operation principle of out-phasing [136]…………………………… 53

Figure 2.43 Schematic of the out-phasing PA (same for PA1 and PA2) [144]……54

Figure 2.44 Schematic of the combiner [144]…………………………………… 54

Figure 2.45 Class-EF2 PA with negative capacitance compensation [146]……... 56

Figure 2.46 Principle of feedback technique [154]……………………………… 58

Figure 2.47 Cartesian feedback technique [156]………………………………… 58

Figure 2.48 (a)Cartesian feedback employed in the system [158]……………….. 59

Figure 2.48 (b)Class-E CMOS PA employed in the system [158]………………..60

Figure 2.49 Output spectrum of the Cartesian feedback [158]……………………60

Figure 2.50 Block diagram of a Polar feedback system [169]…………………….61

Figure 2.51 Schematic of the CMOS PA with AM replica linearization [161]….. 62

Figure 2.52 Block diagram of the feed-forward based PA [162]………………… 62

Figure 2.53 Configuration of the feed-forward CMOS PA [163]……………….. 63

Figure 2.54 The measured linearity of the feed-forward CMOS PA [163]……….64

Figure 2.55 Block diagram of LINC technique [164]…………………………….64

Figure 2.56 Schematic of the hybrid Polar-LINC [171]………………………… 65

Figure 2.57 The concept of pre-distortion [172]……………………………………66
Figure 2.58 (a) The schematic of the proposed CMOS DPA [179]……………….68
Figure 2.58 (b) The schematic of the 1st and 2nd stage PAs at both main and peaking paths [179]…..……………………………………………..68
Figure 2.58 (c) The schematic of the proposed APD [179]…………………….....68
Figure 2.59 (a) Block diagram of the DPD transmitter [185]……………........ 70
Figure 2.59 (b)Schematic of the digital PA [185]…………………………..…… 70
Figure 2.60 Cascode PA configuration [186]……………………………………. 71
Figure 2.61 (a) Schematic of the proposed CMOS cascode PA [191]…………….73
Figure 2.61 (b) Schematic of the proposed dynamic bias linearizers [191]….…..73
Figure 2.62 Operational diagram of ET and APT mode supply modulator [72]…..74
Figure 2.63 Schematic of dual mode supply modulator [72]……………………..75
Figure 2.64 (a)Equivalent load resistance of supply modulator for ET and APT mode. Switch configuration for switching amplifier (b) One-switch with one inductor (c) reconfigurable dual switch with one inductor (d) reconfigurable dual switch with two inductors [72]………………... 76
Figure 2.65 Operational diagram of the proposed dual-mode PA. (a) HPM. (b) LPM [103]………………………………………………………. 77
Figure 2.66 Schematic of two-stage dual-mode CMOS PA [103]………………..77
Figure 2.67 Non-isolated power combiner [194]…………………………………78
Figure 2.68 Schematic of the PAPR-aware CMOS PA [195]…………………….79
Figure 2.69 Dual mode CMOS PA [195]…………………………………………79
Figure 2.70 Schematic of two stage three stacked CMOS PA [196]……………..80

Figure 2.71 Cross-sectional view of the enhanced voltage MESFET device fabricated on the 45 nm technology with no changes to the CMOS process flow [197]…………………………………………………...80
Figure 2.72 (a) Schematic PA with single MESFET transistor and grounded inductor for gate biasing. (b) Board level design photograph for 900 MHz [197]……………………………………..……………82
Figure 2.73 Lumped π-model of the inductor proposed by (a) Nguyen and Meyer [229]; (b) Ashby et al. [211]; and (c) Yue and Wong [217]…………88
Figure 2.74 Equivalent circuit of single terminal grounded inductor for Q-factor modelling…………………………………………………………… 91
Figure 2.75 Different structures of planar spiral indictors on-chip (a) Square (b) Hexagonal (c) Octagonal (d) Circular (e) Meander (d) Solenoid coil…………………………………………………………………...95
Figure 2.76 Patterned ground shield (PGS) inductor……………………………. 96
Figure 2.77 (a) Single-ended (b) Symmetric Inductors (c) Centre tapped inductor [221]…………………………………………………………………97
Figure 3.1 The flow chart of the research methodology………………………. 101
Figure 3.2 Metal stacking of novel HQCI in Sonnet Suit………………………104
Figure 3.3 Structure of novel HQCI……………………………………………104
Figure 3.4 Induced eddy currents and displacement currents in the substrate on impressing current in the spiral inductor……………………………106
Figure 3.5 Geometry of HQCI and its projection on the square spiral sharing the same horizontal and vertical segments……………………………..108

Figure 3.6 (a)Negative mutual inductance contributed by segments on the opposite side(b) Positive mutual inductance contributed by segments on the same side of the inductor………………………………………...109

Figure 3.7 The breakup of the geometry of HQCI: V-shape notch and bent corners into a horizontal and vertical component…………………………..110

Figure 3.8 Impedance versus frequency for the inductance derived in (3.23)….113

Figure 3.9 (a)Size of 4-turn, 7 nH HQCI, octagonal and square planar inductor (b) Inductance and Q-factor response of HQCI, octagonal and square planar inductor……………………………………………………….. 115

Figure 3.10 Basic block diagram of a two-stage RFPA…………………...….... 115

Figure 3.11 Gain of the PA for single stage and double stage…………………. 117

Figure 3.12 Full schematic of proposed multiband dual mode CMOS PA……..118

Figure 3.13 The proposed bias circuit for the PA……………………………….119

Figure 3.14 The dynamic range of bias circuit………………………………… 120

Figure 3.15 High-frequency small signal model for the proposed bias circuit…. 121

Figure 3.16 Impedances and sweet spot for linearity on Smith chart for various matching networks shown in Figure 3.17 ………......................... 123

Figure 3.17 Various output matching networks ………………………………..123

Figure 3.18 Full schematic of the multiband dual mode CMOS PA with the integrated HQCI……………………………………………………126

Figure 3.19 Various output matching networks (a, b, c, d, e) based on the sweet spot of linearity and their impedances on the Smith chart (f)……………127

Figure 3.20 Layout of multiband CMOS HQCI-PA……………………...…..128

Figure 3.21 Probe station and equipment set up for measurement………………129

Figure 3.22 Setup for the small-signal measurement of the PA………..……..130

Figure 3.23 Setup for the large-signal measurement the PA……………….………131
Figure 4.1 Simulated Inductance of HQCI for different turns………………….133
Figure 4.2 Q-factor of HQCI for different turns……………………………….133
Figure 4.3 Series resistance of HQCI for different turns……………………….134
Figure 4.4 Simulated S-parameters and stability factor………………………..135
Figure 4.5 Simulated (a) OIP3 and (b) IMD3 for different output matching networks designed based on sweet spot of linearity for LP and HP modes………..…………………………………………………. 140
Figure 4.6 Simulated (a) OIP3 and (b) IMD3 in HP mode with HQCI integration at OMN at 868 MHz, 892 MHz and 915 MHz……………….…… 136
Figure 4.7 Simulated PAE of the CMOS PA for LP and HP modes before and after integration of HQCI…………………………………………….....139
Figure 4.8 DC power consumption by the CMOS PA for LP and HP modes before and after integration of HQCI……………………………………139
Figure 4.9 Simulated PAE of the multiband CMOS PA in HP mode at 868 MHz, 892 MHz and 915 MHz ……………………………………….....140
Figure 4.10 Simulated (a) AM-AM and (b) AM-PM for LP and HP modes at 868 MHz, 892 MHZ and 915 MHz…………………………………. 141
Figure 4.11 Chip micrograph of stand-alone HQCI with open and short de-embedding structure……………………………………………..142
Figure 4.12 Measured and simulated inductance and Q- factor of HQCI for the 4 turns……………………………………………………………...143
Figure 4.13 Chip microphotograph of multiband CMOS HQCI-PA for LoRa applications ………………………………………………….. 146
Figure 4.14 Measured S-parameters of multiband CMOS HQCI-PA…………..147

Figure 4.15 Measured (a) AM-AM and (b) AM-PM response of HQCI-PA in LP and HP modes at 868 MHz, 892 MHz and 915 MHz……………….149

Figure 4.16 Measured PAE performance for LP and HP modes at 892 MHz……150

Figure 4.17 DC power consumption by CMOS HQCI-PA in LP and HP modes..151

Figure 4.18 Measured PAE performance of multiband HQCI-PA in HP mode at 868 MHz, 892 MHz, and 915 MHz……………………………………. 151

Figure 4.19 Measured (a) ACLR in LP and HP modes at the center frequency of 892 MHz (b) ACLR in HP mode at 868 MHz, 892 MHz, and 915 MHz for 16- QAM/20-MHz modulated input signal.………..………….. 153

Figure 4.20 Measured (a) EVM in LP and HP modes at the center frequency of 892 MHz (b) EVM in HP mode at 868 MHz, 892 MHz, and 915 MHz for 16-QAM/20-MHz modulated input signal.……………………....... 154

Figure 4.21 Measured normalized power spectral density (PSD) across the output power of (a) 21.5 dBm in HP mode and (b) 18 dBm in LP mode at 892 MHz ………………………………………………………………..155

Figure 4.22 Measured output spectrum across the output power of (a) 21.5 dBm in HP mode and (b) 18 dBm in LP mode at 892 MHz…......................156

Figure 4.23 Measured EVM constellation diagram across the output power of (a) 21.5 dBm in HP mode and (b) 18 dBm in LP mode at 892 MHz……………………………………………………………..…. 157

LIST OF ABBREVIATIONS

4G	4th Generation
5G	5t^{h} Generation
AC	Alternating Current
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ration
AM-AM	Amplitude Modulation to Amplitude Modulation
AM-PM	Amplitude Modulation to Phase Modulation
APD	Analogue Pre-Distorter
APT	Average Power Tracking
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
CW	Continuous Wave
DPA	Doherty Power Amplifier
DC	Direct Current
DPD	Digital Pre-Distorter
DRC	Design Rule Check
DSP	Digital System Processing
DUT	Device Under Test
EDA	Electronic Design Automation
EER	Envelope Elimination and Restoration
EM	Electromagnetic
ENA	Electrical Network Analyzer

ESD	Electro Static Discharge
ET	Envelope Tracking
EVM	Error Vector Magnitude
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HBT	Heterojunction Bi-Polar Transistor
HEMT	High Electron Mobility Transistor
HP	High Power
HQCI	High Q-Factor Compact Inductor
IC	Integrated Circuit
IMD3	3rd Order Intermodulation Distortion
IMN	Input Matching Network
IoT	Internet of Things
IQ	In-Phase, Quadrature-Phase
LINC	Linear Amplification with Nonlinear Components
LoRa	Long Range
LPA	Linear Power Amplifier
LP	Low Power
LPWAN	Low Power Wide Area Network
LTE	Long Term Evaluation
LUT	Look-Up Table
LVS	Layout Vs Schematic
NLPA	Non-Linear Power Amplifier
NR	New Radio

OFDM	Orthogonal Frequency-Division Multiplexing
OIP3	3rd Order Intercept Point
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
P_{bo}	Backed off Output Power
P_{out}	Output Power
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RMS	Root Mean Square
SC	Switched Capacitor
SDPA	Stacked Distributed Power Amplifier
SiGe	Silicon Germanium
SoC	System-on-Chip
SOI	Silicon on Insulator
SOLT	Short-Open-Load-Through
SRF	Self -Resonance Frequency
VNA	Vector Network Analyzer
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless Local Area Network
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

LIST OF APPENDICES

APPENDIX PUBLICATIONS

PENGUAT KUASA CMOS BERBILANG JALUR DENGAN INDUKTOR PADAT Q TINGGI BERSEPADU UNTUK APLIKASI LORA

ABSTRAK

Dalam pembangunan meluas Internet Perkara (IoT), Mesin-ke-Mesin (M2M), dan aplikasi bioperubatan dalam penyelidikan dan penyeragaman, spektrum sub-GHz telah mendapat perhatian baharu. Peranti jarak jauh (LoRa) menggunakan jalur frekuensi sub-GHz untuk beroperasi. Saiz cip menjadi lebih besar apabila direka untuk menyasarkan frekuensi rendah dan ia disumbangkan terutamanya oleh induktor. Dalam penyelidikan ini, penguat kuasa (PA) CMOS berprestasi tinggi dengan bentuk tersuai baru, induktor padat faktor Q tinggi (HQCI) dihasilkan dalam proses CMOS 130 nm, 6 lapisan logam. HQCI direka bentuk dan direka dengan 4 lilitan, setiap satu dengan lebar logam berubah-ubah 20 µm, 28 µm, 30 µm, dan, 30 µm (dari dalam ke luar), dipisahkan oleh 2 µm. Kearuhan 7 nH dan faktor Q 11.2 HQCI diukur pada frekuensi 892 MHz. Kawasan sebenar yang diduduki oleh HQCI pada cip ialah 0.21 mm^2, manakala induktor oktagon dan segi empat sama konvensional menduduki 0.27 mm^2, dan kawasan 0.32 mm^2 pada cip untuk nilai kearuhan yang sama. HQCI yang direka bentuk disepadukan dalam mod dwi CMOS PA yang beroperasi pada jalur frekuensi 868-915 MHz. Teknik pensuisan digunakan untuk meningkatkan kecekapan tambah kuasa belakang (PAE). 1.96 mm^2 CMOS HQCI-PA ialah mod dwi 3.3 V yang mampu memberikan kuasa output linear maksimum 18 dBm pada mod kuasa rendah (LP) dan 21.5 dBm pada mod kuasa tinggi (HP). PAE linear yang sepadan ialah 22% dan 28% masing-masing. Ini menunjukkan bahawa pertukaran antara lineariti dan PAE juga dikurangkan dengan menggunakan HQCI kerana ia memberikan nilai faktor

Q yang lebih baik. Kuasa keluaran linear tinggi dengan kecekapan tinggi ini sesuai dengan PA untuk disepadukan dalam pemancar-penerima LoRa berbilang jalur.

MULTIBAND CMOS POWER AMPLIFIER WITH INTEGRATED HIGH-Q COMPACT INDUCTOR FOR LORA APPLICATION

ABSTRACT

In the wide development of the Internet of Things (IoT), Machine-to-Machine (M2M), and biomedical applications in research and standardization, the spectrum of sub-GHz has received fresh attention. Long-range (LoRa) devices use the sub-GHz frequency bands to operate. The size of the chip becomes bigger when designed to target low frequencies and it is mainly contributed by the inductors. In this research, a high-performance CMOS power amplifier (PA) with a novel custom shape, high Q-factor compact inductor (HQCI) is fabricated in 130 nm, 6-metal layers CMOS process. The HQCI is designed and fabricated with 4 turns, each with a variable metal width of 20 µm, 28 µm, 30 µm, and, 30 µm (from inner to outer), separated by 2 µm. An inductance of 7 nH and a Q-factor of 11.2 of HQCI is measured at the frequency of 892 MHz. The actual area occupied by the HQCI on the chip is 0.21 mm^2, whereas the conventional octagonal and square inductor occupies 0.27 mm^2, and 0.32 mm^2 area on-chip for the same inductance value. The designed HQCI is integrated in mode switching CMOS PA operating on the frequency band of 868-915 MHz. Switching technique is employed to improve the back-off power added efficiency (PAE). The 1.96 mm^2 CMOS HQCI-PA is a 3.3 V dual mode which is capable to deliver a maximum linear output power of 18 dBm at low power (LP) mode and 21.5 dBm at high power (HP) mode. The corresponding linear PAE are 22% and 28% respectively. This indicates that the trade-off between linearity and PAE is also reduced by using the HQCI since it provides a better Q- factor value. This high linear output power with high efficiency suits the PA to be integrated in the multiband LoRa transceiver.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Recent years have seen a significant advancement in wireless communications. The wireless industry, along with microchips and computers, is a major impetus behind semiconductor development. As a result, foundries are improving their technologies to incorporate expansion that facilitates the implementation of radio frequency (RF) circuits. Recent technological advancements and development in wireless communications and RF integrated circuits have enabled low-power solutions strategically placed to enhance machine-to-machine communication as well as human-to-machine communication to revolutionize the manufacturing industry which leads to the birth of Industry revolution 4.0. The development of low power wide area networks (LPWAN) is one of the innovations that underpins this revolution [1]. Figure 1.1 depicts the applications of the LPWAN technologies.

Figure 1.1 Application of LPWAN technologies [1]

In cognate to Moore's law for integrated circuits, a reduction in the size and cost is expected in the design of today's wireless communication products. In the era of the internet of things (IoT), communication between the physical and digital world has become easier and covers wider areas with long battery life [2]. There has been a drastic advancement in the IEEE 802.11 devices that highly clogged at 2.4 GHz band, as well as IEEE 802.15.4 sensor devices which uses UHF band. Lately the first frequency band (FR1) of 5G new radio (NR), 410 MHz - 7125 MHz (Sub-6 GHz) is rapidly growing and specifically sub-GHz hence becoming the centre of attraction for the researchers for the new wireless technology [3].

For the transmission and reception of data, RF system needs to have transmitters and receivers. The design of a power amplifier (PA) block is the most strenuous part in a transceiver, owing to its unrestrained power consumption. In handsets and cellular base stations, the PA is an essential integral component of the RF front-end architecture. The PAs are commonly fabricated in III-V compound semiconductors such as GaN HEMT [4], GaAs HBT [5]-[6], Si Bipolar [7]-[8], and SiGe HBT [9-11] because of its advantages in delivering favourable linear output power and efficiency in contrast to silicon CMOS process. To reach the goal of system-on-chip (SoC), however, the implementation of RFIC positively required to be fabricated with the CMOS process so that the cost and size can be minimized. Due to its distinct characteristics, complementary metal-oxide semiconductor (CMOS) radio frequency PA is preferred in the majority of SoC applications.

1.1.1 Sub-GHz Frequency Band

The sub-GHz frequency band refers to the frequency below 1-GHz. The RF devices working on frequencies below 1- GHz are known as sub-GHz devices. Although the higher frequency RF devices are faster in wireless communication, researchers are moving towards the sub-GHz frequency band due to its long-distance and wider scope communication capability. The IoT, M2M, and biomedical

applications that have grown significantly in recent years, both in terms of research and standards, have drawn new attention to the spectrum below 1 GHz. This is because it has a greater communication range and is license-exempt. Higher frequencies are attenuated more strongly inside solid structures and building materials. The ability of the sub-GHz frequency to penetrate huge buildings or structures gives it an edge over the 2.4 GHz transmission. Additionally, a sub-GHz signal can travel a long way and pass through obstructions in densely populated regions. This is the primary factor contributing to the superior performance of sub-GHz microchips for RF devices that operate in the license-free Industrial, Scientific, and Medical (ISM) frequency bands [12].

1.1.2 Long Range (LoRa) Technology

The term "LoRa" refers especially to devices that operate in sub-GHz frequency bands. Chirp-spread spectrum modulation, or LoRa, is a physical layer that is used to build long-distance communication lines. Chirp spread spectrum modulation, in contrast to frequency shifting keying (FSK) modulation, keeps the low power feature while vastly expanding the communication range [13]-[14]. The rapidly expanding LoRa technology is receiving more attention from the scientific research community as a result of applications that coincide with significant advancements in the industrial sector. LoRa modulation's sensitivity and communication coverage range are initially tested in numerous specialized field trials [15]-[17]. For IoT and M2M communication, LoRa technology delivers long-range wireless fidelity with minimal power and reasonably safe data transmission. In line of sight, RF devices using LoRa technology perform better on the battery life at distances of 5 km in urban areas and 10–15 km or more in rural areas [18]. The LoRa-based system's attractive feature is its extremely low power consumption, which allows it to run for up to 10 years or longer on a single battery. The benefits of LoRa over Wi-Fi, Bluetooth, and NB-IoT include a greater communication range, longer battery life, and lower costs.

Different frequency bands for LoRa technology are used in various geographical locations: It runs in the 915 MHz spectrum in the United States, the 868 MHz band in Europe, and the 865 to 867 MHz and 920 to 923 MHz bands in Asia [19]-[20]. The key advantage of the sub-GHz band is that a longer transmission distance can be achieved under the same power of transmission. For example, if 2.4 GHz Wi-Fi covers the 100 meters distance then the LoRa device operating in sub-GHz frequency may cover around 800 meters, approximately 64 times larger coverage area. Moreover, complex modulation schemes such as 16-QAM, 32-QAM, etc, or high transmission rates are not required in sub-GHz. It can be implemented with simple modulation schemes such as ASK, FSK, etc., and longer transmission distances up several kilometres can be achieved [21]-[22]. Figure 1.2 indicates the benefits of sub-GHz system in terms of setup, reliability, and battery operation.

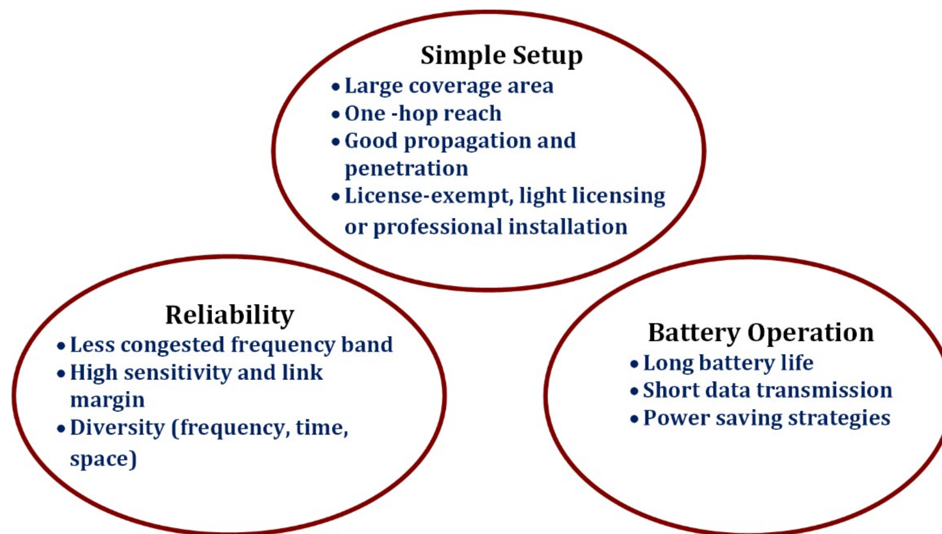

Figure 1.2 Benefits of a standardized sub-GHz system [20]

1.2 Problem Statement

Despite the advantages of the sub-GHz band, there are some challenges in this band. The first is the larger area occupying circuits. The frequency and wavelength are related as follows:

$$f = \frac{c}{\lambda}$$

(1)

In above relation, c denotes the speed of light which can be considered as v, the speed of radio wave, λ is the wavelength of the signal. Frequency and wavelength are reciprocal in relation which implies that: a lower frequency has a larger wavelength. To some extent, the size of an electrical/electronic circuit is determined by the wavelength of the circuit it operates on and the way it interacts with EM fields. For example, the size of a transmitter must be a significant fraction of the wavelength of the radio signal to receive and transmit the signal effectively. Similarly, another component also may produce or receive the noise signals if the size of the transmitter is large or small as compared to the wavelength. By comparing physical dimensions to wavelength, one can determine the electrical dimensions of a device or circuit as follows:

$$d_e = \frac{l}{\lambda} \tag{2}$$

If the circuits' biggest dimension is less than the wavelength of the signal it is working on, then they are said to be electrically small. Additionally, it must be noted that the size of the circuits depends on the substance through which radio waves travel. If a device is assembled on a printed circuit board (PCB), it may be larger than if it were surrounded by air. For instance, a capacitor with a high permittivity dielectric is electrically larger than one with air between the plates of a similar capacitor [23]-[25]. So, for the sub-GHz frequency band, the one drawback is the circuits will become larger and the overall chip size will be increased due to the larger wavelength.

Secondly, the un-unified frequency band for LoRa for different regions of the world. Different countries have different frequency bands allotted in sub-GHz bands for LoRa applications. Therefore, IC designers need to design a single chip that can support multiple frequency bands.

Typically, a mobile wireless RF front-end comprises multiple PAs in order to serve for the various communication standards that operate at multiple frequencies as shown in Figure 1.3 [26]. In this Figure, it can be observed that substantial amount of space is needed just for the PAs. Therefore, it is essential for a single PA to occupy lesser area on the chip for sub-GHz operations. Additionally, a single PA can operate at a higher bandwidth to cover the numerous frequency bands required by wireless communication standards. This will guarantee the removal of many PAs from a system and help to save costs because the chip footprint can be mitigated. Due to the devices' different frequency responses across the frequency, it is difficult to attain the same linearity and efficiency across the bandwidth.

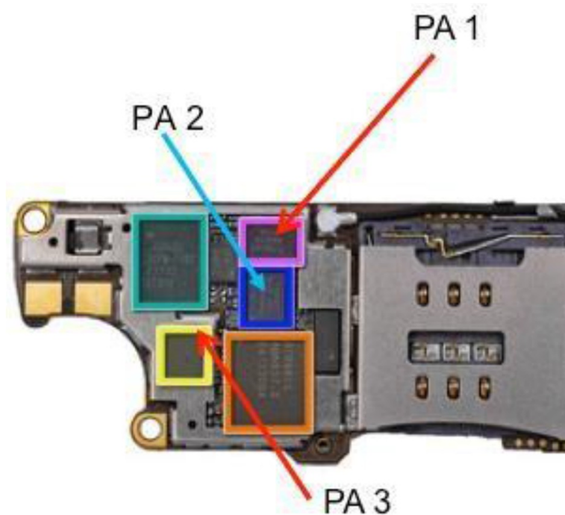

Figure 1.3 Multiple PAs for multiband wireless system [26]

One of the key challenges limiting the performance of PAs is the current exchange between linearity and efficiency. For RF transmitters to achieve very high bandwidth (around and even above 1-GHz for broadband modulation), high-efficiency PA is required. Linearity is one of the most crucial factors of merit (FoM) in PA design. Recently, it has been challenging to get the PA to work at high efficiency with acceptable linearity, especially in the CMOS process. This is due to the CMOS technology' drawbacks, which include low breakdown voltage, a lack of substrate

through holes, constrained current driving capabilities and a low-quality factor [27]-[28].

The signal envelope produced by the orthogonal spread spectrum has a non-constant shape and a high peak-to-average power ratio (PAPR) [29]. This imposes strict requirements on the linearity of the PA. In addition to linearity, PAE is a crucial characteristic for improving the battery life of the device. In spite of that, the transmit signal's high PAPR depreciates the performances of the PA in terms of PAE and linearity. This is because, in order to transmit linearly and efficiently without clipping the high PAPR signals, the PA is required to be operated at backed-off output power (P_{BO}). The P_{BO} is a reduced output power of the PA from its maximum output power and the PAE achieved at the P_{BO} is usually low. Therefore, PAs are compelled to work in a less effective back-off region in order to transmit in compliance with the rigorous linearity standards. Thus, to increase the P_{BO} , the linearity and efficiency of the PA needs to be enhanced [30].

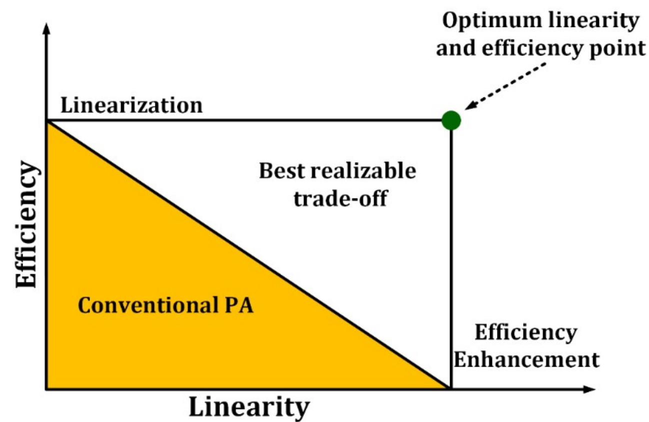

Figure 1.4 The trade-off between linearity and PAE of a RFPA [31].

The main hindrance for the design engineer to design a PA is to achieve high linearity as well as high PAE at the same time. Since, achieving high linearity at

maximum output power (P_{out}) with high PAE is a challenging task. Besides, high linearity is achieved at the low P_{out} where PAE is low. Figure 1.4 conceptually illustrates the trade-off between linearity and PAE in the RFPA [31]. A key linearity and PAE enhancement techniques are needed to reduce the trade-off between the linearity and PAE.

The of adjacent channel leakage ratio (ACLR) is another important measure for the linearity of the PA. For an example, a PA should deliver peak P_{out} of 37 dBm to meet the ACLR specification that needs 30 dBm P_{out}, if the specified PAPR of 7 dB is the requirement for the transmitted signal. By referring to equations (1.1) and (1.2) that relate the PAE and P_{bo}, it can be observed that PAE is degraded significantly.

For a class-A PA, the backed-off PAE is expressed as [31]:

$$\eta_{\text{pbo-classA}} = \frac{1}{2} \bullet \frac{P_{bo}}{P_{max}} \tag{1.1}$$

For a class-B PA, the backed-off PAE is expressed as [31]:

$$\eta_{\text{pbo-classB}} = \frac{\pi}{4} \bullet \sqrt{\frac{P_{bo}}{P_{max}}} \tag{1.2}$$

In above equations, the back-off power is denoted by P_{bo} and peak output power (mW) is indicated by P_{max}.

It can be understood by taking an example from equation (1.1), if a class-A PA with 37 dBm maximum output power is transmitting a WCDMA signal with a PAPR of 7 dB, then the PAE at P_{bo} of 30 dBm will be 9.98%. The PAE of 9.98 % is not enough for a battery of a wireless communication device to operate for long life since it will drain the battery power quickly and frequent charging will reduce its lifetime. Therefore, the need of innovation of linearization techniques is essential to reduce the P_{bo} and improve the PAE. Care should also be taken by the designer so that high linearity and PAE must be maintained across the target band of frequency to sustain for wideband applications.

On the other side, in the RFICs, most of the area is consumed by the planar spiral inductor. Being an essential component of the chip performance of analog RFICs such power amplifiers (PA), low noise amplifiers (LNA), and voltage-controlled oscillators (VCO) depends on the inductor's Q-factor. Due to larger size, on-chip spiral inductors are essential in determining the actual chip area specially for low frequencies. To reduce the size of the overall chip and meet with fully integrated system's requirement, the inductor size is the challenge for the low frequency applications [32]-[34].

Therefore, the focus of this research is on decreasing the overall circuit size for the sub-GHz application. Since the CMOS planar spiral inductor is the main component in RFIC which covers a larger area on the chip. Additionally, Q-factor of the inductor is an important parameter which affects the performance of the PA. This issue is addressed by inventing custom shape compact inductor having high Q-factor/Area (Q/A) ratio. The idea of proposing new inductor starts with the EM simulation of conventional shape ideal inductors. Octagonal, square shapes inductors are simulated in Sonnet EM simulation tool. The shape and structure of these inductor are varied in order to get high Q-factor. Further, variable width of metallic turns is employed to reduce the magnetic losses in the inner turns to improve the Q-factor. High Q- factor of the inductor helps to improve the PAE of the PA because of its lower series resistance. To decrease the overall chip area, a unique shape, high Q-factor compact size inductor (HQCI) is invented. The HQCI is implemented in the 2-stage CMOS RFPA at the input/output matching network and RF choke. The complexity of the matching networks is reduced by the use of HQCI in the input and output matching networks. Moreover, PAE of the PA is enhanced by using the HQCI. Furthermore, the linearity of the PA is improved by optimizing the HQCI based matching networks according to the sweet spot of the linearity without scarifying the PAE. The RFPA is designed and fabricated in the 130 nm CMOS process with the least trade-off between

the linearity and PAE. The sub-GHz frequency band of 868-915 MHz is targeted for the design of RFPA applicable for the LoRa technology.

1.3 Research Objectives

Based on the problems discussed in the previous section, this research work is focused to address the issues associated in the sub-GHz frequency band. To reduce the size of the biggest component in the analog RFIC, i.e. planar inductor, a compact size high Q-factor planar inductor need to be designed which will be used at the matching networks and RF chokes. The high Q-factor compact inductor reduces the overall DC power consumption of the PA resulting the enhancement in the PAE. Furthermore, a single PA is also needed to be designed which can work on the multiple LoRa frequencies.

The research objectives this research work are as follows:

I. To design and fabricate a compact size CMOS planar spiral inductor achieving Q-factor/Area (Q/A) ratio of more than 47 on-chip for sub-GHz frequency operation.

II. To integrate of high Q-factor compact inductor (HQCI) in CMOS PA that operates at lower backed-off output power while maintaining a linear PAE of more than 20%, hence reducing the trade-off between linearity and PAE for LoRa applications

III. To design, fabricate and validate a multiband CMOS PA which achieves maximum output power more than 25 dBm with reduced power dissipation to be integrated in LoRa SoC.

1.4 Research Scope

This research work is focused to address the issues associated in the sub-GHz frequency band. The size and area of the overall chip is reduced by inventing new small size custom inductor with high Q- Factor. The proposed Inductor is integrated in CMOS PA to enhance the overall efficiency and reducing overall chip area. The CMOS PA is designed to work at multiband sub-GHz frequency. The trade-off between PAE and linearity of the PA is targeted to be reduced. The PA is designed to meet the specifications of ACLR below -30 dBc and EVM of below 4%. Furthermore, a single PA is designed which can work on the multiple LoRa frequencies.

1.5 Thesis Outline

In order to execute the stipulated objectives and design envisioned for this research, this thesis is outlined as follows.

Chapter 2 presents the profound literature study on CMOS PA performance metrics, types of RFPAs, trade-off between efficiency and linearity, efficiency enhancement techniques, linearity enhancement techniques, and recent work comparisons which have been conducted by multiple research organizations in the frequency band of sub-GHz. The literature study on the on-chip CMOS planar inductors has also been carried out in this chapter.

The overall design methodology and its flow have been described extensively in chapter 3. The design of the novel shape, compact size, high Q-factor CMOS inductor is presented. A comprehensive mathematical and theoretical analysis for the inductance and Q-factor is presented. The new bias circuit and bias modulation technique for linearity enhancement in 2-stage CMOS PA is presented. Th analysis of 2-stage of CMOS PA and the integration of high Q-factor compact inductor (HQCI) with the 2-stage CMOS PA is described in this chapter.

Chapter 4 presents and elaborates the complete simulation and measurement results achieved by the layout design of HQCI-PA in 130 nm has been presented and fabricated chip photo micrograph of the chip are clearly shown.

Chapter 5 briefly provides the conclusion and proposed future works for this research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Wireless communication systems have been enormously evolving in current era, exclusively for the transition from 4th Generation (4G) to 5th Generation (5G) which is tremendously being deployed in recent years. The unprecedented increase in the number of wireless devices and mobile data usages are creating the demand for more enhancements and upgrades to be implemented on current wireless communication systems. CMOS transceivers are being progressively explored in order to fulfill the stipulations of the latest wireless communication protocols and applications as well as achieving the goal of System-on-Chip (SoC). In a CMOS transmitter, the RFPA plays a vital role in amplifying the RF signals and transmit it from the antenna. In this chapter, a concise discussion of the performance metrics that needed to be focused on while designing a PA is presented. This chapter is then continued with a brief explanation on the existing classes of CMOS RFPAs designed recently to operate on sub-GHz frequencies for LoRa applications. Lastly, recent published work comparison in terms of the performances of CMOS PA is presented.

2.2 CMOS Radio Frequency Power Amplifier (RFPA)

In both cellular base stations and handset RF front-end systems, the power amplifier (PA) is a crucial component. PAs are the component of the transceiver that are most important for reliable wireless communications. It is also the most power-hungry block because it is utilized to amplify the signal to obtain the necessary output power [35]-[36].

An emerging architecture of PA for 5G technology is required to improve the power efficiency of the transmitter as it directly depends on the performance of the RFPA. Currently, expensive III-V compound semiconductors are used to design PAs for mobile handset applications since they tend to produce higher linear output power than silicon because of their less inherent parasitic. [37].

Figure 2.1 indicates the basic block level architecture of the CMOS power amplifier (CMOS PA). It consists of 2 power stages (sometimes three, including the pre-driver stage) namely the main stage and driver stage. Both the stages are biased with different biasing voltages. The power supply is also given separately to both stages so that the PA can operate accurately and properly. Input and output impedances are matched to a 50 Ohm load impedance using input and output matching networks. Matching networks reduce the return losses (S_{11} and S_{22}), and improve the power gain and output power. Inter-stage matching is also required to match the impedance between the main stage and driver stage [38].

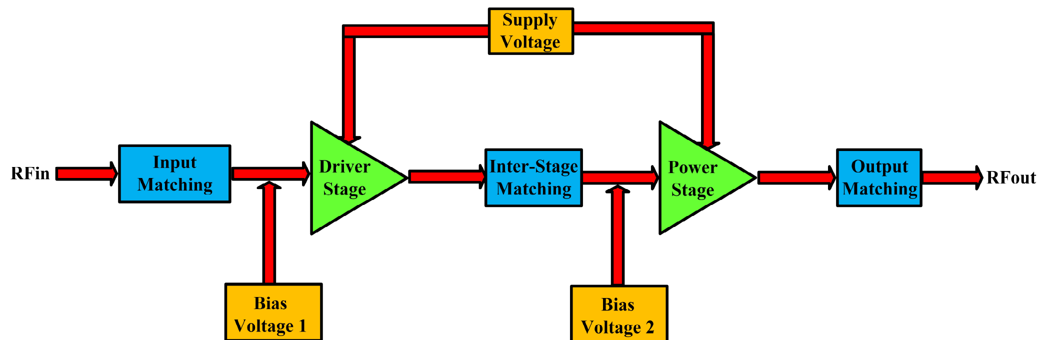

Figure 2.1 Basic block level architecture of a 2-stage CMOS PA [38]

2.3 Types of RF Power Amplifiers

The classes of RFPAs are determined by its operation mode, and it can be classified onto two major groups which are linear and non-linear modes. Figure 2.2

shows the classes of RFPAs which are commonly implemented in circuit designs. The topologies such as class A and AB are classified as linear modes. These classes are operated with a sinusoidal waveform in where the transistors acts as a voltage controlled current source [64]. The class of operation of these linear PAs can be identified from their drain current conduction angle. The percentage of the RF signal cycle in where the transistor is conducting reflects the operation class of the PA.

On the other hand, the non-linear PAs consist of classes such as B, C, D, E, F, G and J. Although class B, C, G and J are current source mode PAs, distortions are still present due to their reduced conduction angle. The class D, E and F PAs are also referred as switch-mode PAs since the transistor behaves like a switch by turning on and off during operation. In an ideal case, the switch dissipates zero power since there are no voltage across it or current flowing through it. Thus, since the transistor dissipates zero power and provided there are no other losses in the PA, its efficiency is theoretically 100%.

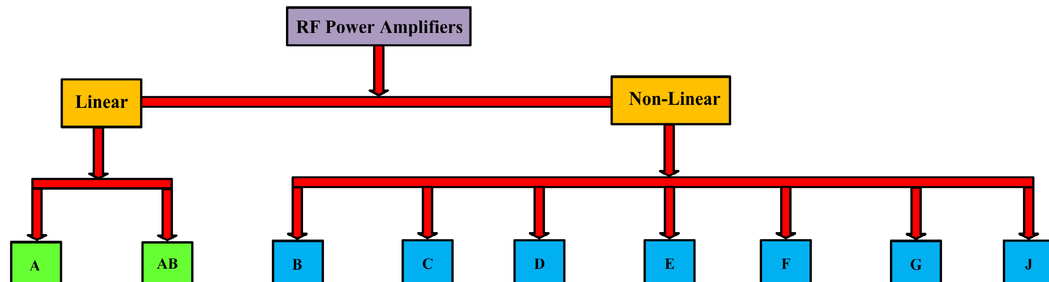

Figure 2.2 Classification of RFPAs.

2.3.1 Linear Power Amplifier

2.3.1(a) Class-A Power Amplifier

Class-A PA is known as the most “classical PA” for its full conduction angle of 360° which never lets the transistor turns off. The portion of a signal applied to the input of

the PA for which the transistor conducts is indicated by the conduction angle. The typical drain voltage and current waveforms are shown in Figure 2.4 for the generic single-stage PA shown in Figure 2.3. Due to the linear relation between the drain current and input voltage in equation (2.1) and non-abrupt drain current, the linearity of the class-A PA is certainly high but efficiency is low for the same reason. Since this relationship is not highly linear [65] for the practical PA from an analytical perspective, it is very tractable to use the ideal model. Figure 2.3 shows the basic circuit for consideration. The transistor is biased at a certain voltage with the bias current (I_{DC}) and the current (i_{rf}) as the signal component of the drain current. Several works reported the derivation for the efficiency [66]-[67].

$$i_D = k\left(v_{in} - V_{th}\right) \tag{2.1}$$

$$i_D = I_D + i_{rf} \sin \omega t \tag{2.2}$$

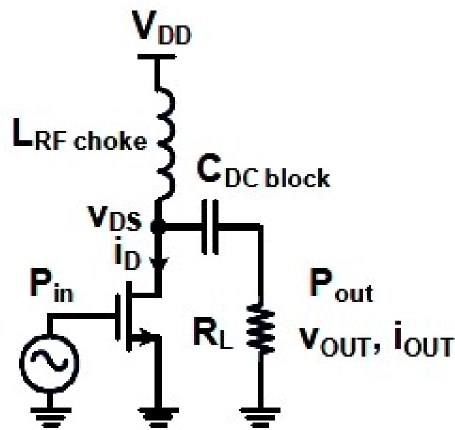

Figure 2.3 Basic single-stage CMOS PA [65]

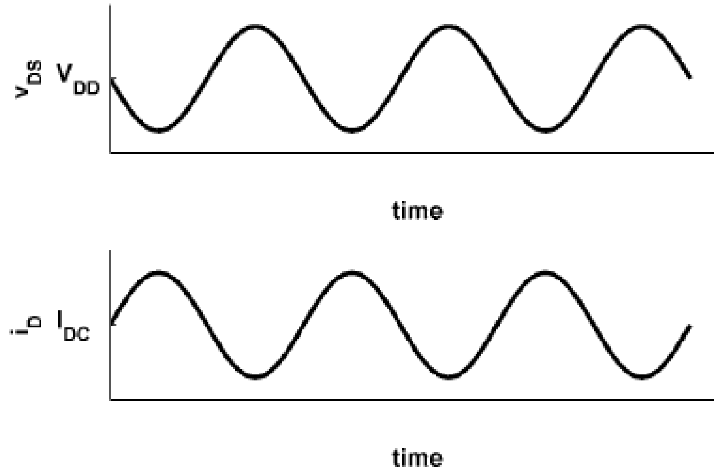

Figure 2.4 Drain current and drain voltage waveforms for ideal Class-A PA [65]

The output voltage is the simple multiplication of current and load resistance equation (2.3). RF choke is provided to pass the pure DC while blocking the AC component from the supply and consequently, the signal current is just the signal component of the drain current. Since the RF choke is short-circuited for the DC frequencies originating from the supply, drain voltage will be the sum of DC voltage and signal voltage. In a conclusion, the peak drain voltage would be $2V_{DD}$ for the peak drain current of $2V_{DD}/R$. From this assumption, output power and dissipated DC power can be stated as in equation (2.4) and (2.5). It is evident that these parameters are independent of the output RF signal. Consequently, 50% maximum efficiency can be calculated according to equation (2.6). The efficiency may drop significantly for the low output swing with amplitude A equation (2.7) owing to more power dissipation across the device. It is noted that the absolute maximum efficiency of class-A PA is 50 % assuming full output swing without any loss in matching network and presence of amplitude modulation.

$$v_{out} = i_{rf} R \sin \omega t \tag{2.3}$$

$$P_{\text{out}} = P_{rf} = \frac{i_{rf}^2 R_L}{2} = \frac{V_{DD}^2}{2R_L} \tag{2.4}$$

$$P_{dc} = V_{DD} I_{DC} = V_{DD} i_{rf} \tag{2.5}$$

$$DE = \frac{P_{rf}}{P_{DC}} = \frac{i_{rf}^2 \left(R_L / 2\right)}{i_{rf} V_{DD}} = \frac{i_{rf} R_L}{2V_{DD}} = \frac{V_{DD}}{2V_{DD}} = \frac{1}{2} \tag{2.6}$$

$$DE(A) = \frac{P_{\text{out}}(A)}{P_{DC,drain}(A)} = \frac{A^2 / 2R_L}{V_{DD} I_{DC}} = \frac{A^2 / 2R_L}{V_{DD}\left(V_{DD} / R_L\right)} = \frac{1}{2}\left(\frac{A}{V_{DD}}\right)^2 \tag{2.7}$$

High voltage/high power (HiVP) PA was proposed by Lei Wu et al. utilising ST 0.13 μm CMOS technology [68]. The claimed PA is operated at 900 MHz frequency and in class-A mode.

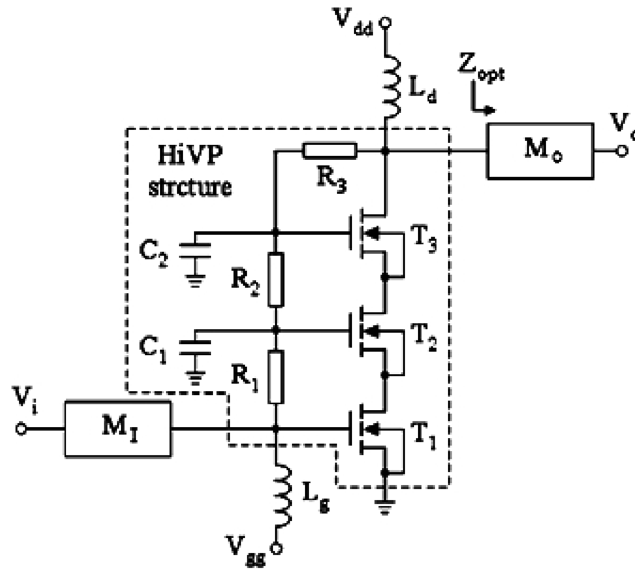

Figure 2.5 ST 0.13 μm CMOS Class-A PA [68]

The schematic of the reported PA is shown in Figure 2.5. The full supply voltage (3.5 V) used in cellular phones is applied in order to achieve high output power. For a

single transistor, however, the breakdown voltage is near 2.5 V, and the supply voltage itself is overstrained. The large drain voltage required for high output power is shared by series-connected transistors. The transistors are used in HiVP mode with identical operating points so that equal current flows through them. A voltage divider resistor combination (R_1-R_3) is formed to ensure equal drain voltage at all the transistors. All the gates are connected to a voltage source (V_{gg}) providing equal gate to source voltage at all transistors. R_3 is also serving as a feedback resistor to allow all the gate voltages to swing according to the RF output signal. Inductors L_d and L_g work as RF choke to feed pure DC to the drain and gate of the PA respectively. Output matching circuits, M_1 and M_2 are employed to match load impedance to 50 Ω RF load. The HiVP chip is mounted on a printed circuit board (PCB) with all the passive components for the measurement.

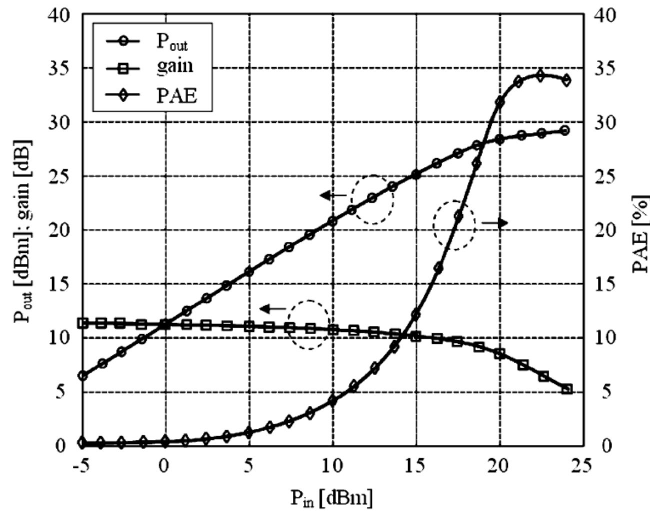

Figure 2.6 Measurement results of HiVP PA [68]

Figure 2.6 indicates that the measured saturated power is 29.5 dBm with 27 dBm 1-dB compression power. The maximum PAE of 34.5 % is achieved at saturated output power. The low small-signal gain of 11.5 dB is the drawback of the reported PA. Moreover, the authors have not reported linearity related measurements.

2.3.1(b) Class-AB Power Amplifier

Class-AB PA operates in the saturation region for a period of time that is longer than the half signal cycle and shorter than the full signal cycle. The drain current has a conduction angle of more than 180º but less than 360º. Both class-A and class-B PA traits can be found in class-AB PAs. In other words, a class-AB PA operates in class-A mode while the input signal is weak, switching to class-B mode when the input signal significantly increases. The typical structure of class-AB PA and its conduction angle are illustrated in Figures 2.7 and 2.8, respectively.

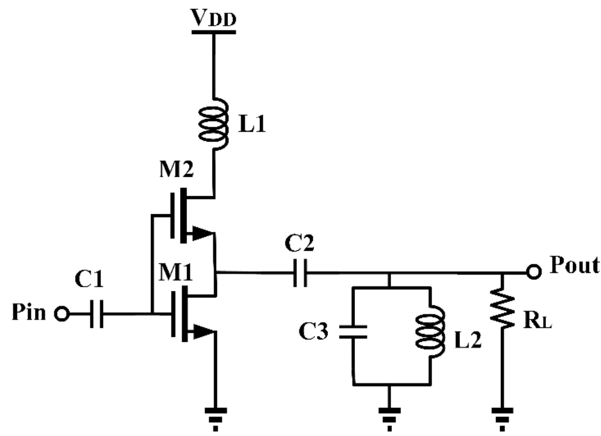

Figure 2.7 Configuration of a class-AB PA [69].

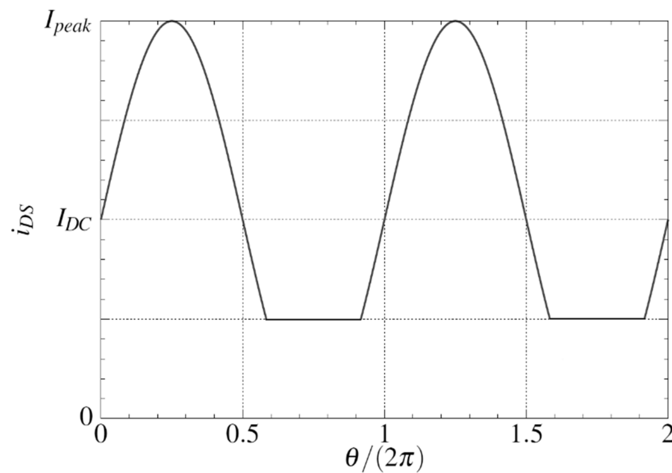

Figure 2.8 Conduction angle of a class-AB PA [69].

The output power for Class-AB PA may be expressed as [69]:

$$P_{out} = \frac{I_f^2 R_L}{2} = \frac{I_f R_L I_{out}}{4\pi}\left[2\theta - \sin(2\theta)\right] \quad (2.8)$$

where I_f is the fundamental current. The DC power for class-AB PA is defined as [69]:

$$P_{DC} = I_{DC} V_{DC} = \frac{V_{DC} I_{out}}{\pi}\left[\sin\theta - \theta.\cos\theta\right] \quad (2.9)$$

Consequently, the efficiency of this PA can be calculated as [69]:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{I_f R_L\left[2\theta - \sin(2\theta)\right]}{4V_{DC}\left(\sin\theta - \theta.\cos\theta\right)} \quad (2.10)$$

The ideal efficiency of a class-AB PA is halfway between that of a class-A PA (50%) and a class-B PA (78.5%). Practically, maximum efficiency of 55% can be achieved in class-AB CMOS PAs [70].

A GaAs HBT PA is designed in class-AB mode for the sub-GHz operation as reported in [71]. For the frequency range of 700 MHz–800 MHz, an analog pre-distortion (APD) circuit and phase linearizer are utilized to improve the linearity of the PA while retaining efficiency. Using a unique linearizer circuit for dual stage PA, the AM-AM distortion caused by parasitic capacitances at PN-junction under low bias current conditions is eliminated. The maximum linear P_{out} of 28.5 dBm with PAE of 57 % is achieved for the bandwidth of 100 MHz. The fully integrated multistage GaAs HBT PA is designed to deliver both efficiency and PAE for the 4G and 5G wireless communications applications.

An envelope tracking (ET) PA operating in class-AB mode is reported in 180 nm CMOS process to operate at the frequency of 0.78 GHz in [72].

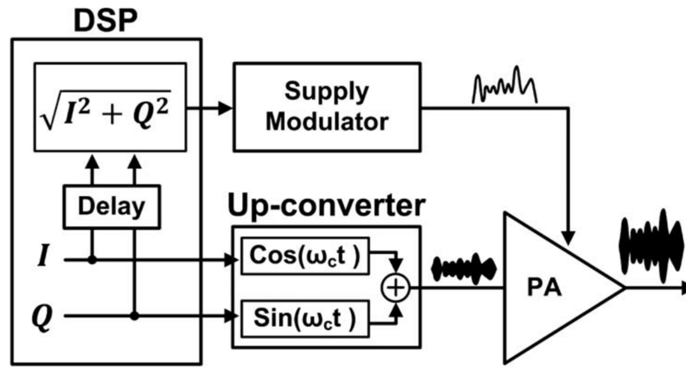

Figure 2.9 Envelope tracking PA [72]

The fundamental block diagram of the ET PA, which includes the supply modulator, is delineated in Figure 2.9. The supply modulator dynamically inputs the bias voltage to the PA in accordance with the digital block's envelope signal. The designed PA operates on two mode: ET mode (for high output power) and average power tracking (APT) mode for low output power by the switching technique. The buck converter based dual mode supply modulator is used. The maximum PAE of 45.4 % is achieved at the average P_{out} of 24 dBm while the PAE of 14.1 % was achieved in APT at the average P_{out} of 9 dBm.

2.3.2 Non-Linear Power Amplifier

2.3.2(a) Class-B Power Amplifier

Class-B is known as the 'sister' of Class-A PA as both have similar basic circuitry as shown in Figure 2.3. The only difference is the bias condition. The bias voltage in class B is adjusted so that the transistor can conduct in half RF cycle only i.e. the conduction angle will be 180° at the threshold voltage [69]. Consequently, more distortions occur in output voltage due to the intermittent operation of the transistor. To get fairly sinusoidal voltage at the output, a high-Q tank circuit is needed to be connected at the output. Just like class-A PA, drain current and voltage can be analyzed where it is sinusoidal for the conduction angle of the transistor as shown in Figure 2.10.

According to Fourier coefficient, a fundamental element of drain current can be stated as in equation (2.11). The maximum output voltage and hence the maximum signal component in drain current will be similar to that of class-A. The DC supply current can also be computed through the Fourier coefficient as in equation (2.12) and eventually, maximum drain efficiency for class-B can be evaluated as in equation (2.13) [69].

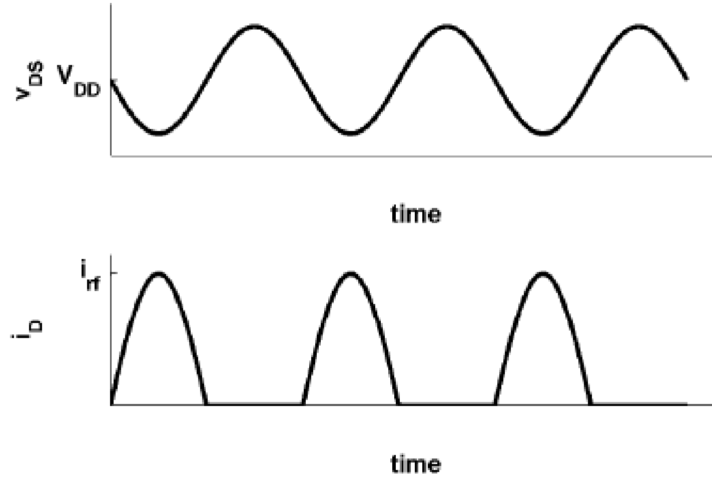

Figure 2.10 Drain voltage and current waveforms in an ideal Class-B [69]

$$i_{D,\text{ fund}} = \frac{2}{T}\int_0^{T/2} i_{rf}\sin(\omega t)\sin(\omega t)dt = \frac{i_{rf}}{2} \tag{2.11}$$

$$\overline{i_D} = \frac{1}{T}\int_0^{T/2} \frac{2V_{DD}}{R_L}\sin(\omega t)dt = \frac{2V_{DD}}{\pi R_L} \tag{2.12}$$

$$DE = \frac{P_{out,\max}}{P_{DC}} = \frac{V_{DD}^2 / 2R_L}{2V_{DD}^2 / \pi R_L} = \frac{\pi}{4} \approx 0.785 \tag{2.13}$$

It is clear that class-B has more efficiency than class-A, albeit at the expense of higher distortion. Moreover, the gain is reduced by around 6-dB compared to class-A,