UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2022/2023 Academic Session

July/August 2023

EEE348 – Introduction to Integrated Circuit Design

Duration : 2 hours

Please check that this examination paper consists of **SEVEN (7)** pages of printed material including appendix before you begin the examination.

Instructions : This paper consists of **FOUR (4)** questions. Answer **all** questions.

1. Design the schematic of the logic circuit for the following Boolean Functions:

a) $Y = \overline{(AB + C)(D + E)}$

(30 marks)

b) $Y = \overline{A.B.C}$

(15 marks)

c) $Y = \overline{A(D + E) + BC}$

(30 marks)

d) $Y = A.B.C$

(25 marks)

2. a) With an aid of a diagram, analyze the principle of operation of the following:

(i). nMOS transistor.

(15 marks)

(ii) pMOS transistor

(15 marks)

b) Figure 1 illustrates the mask sets of a CMOS circuit. Construct the equivalent

(i). Cross section of the circuit.

(40 marks)

(ii). Schematic of the circuit.

(10 marks)

(iii). Switching diagram and the truth table of the circuit.

(10 marks)

(iv). The general full custom design flow of the circuit.

(10 marks)

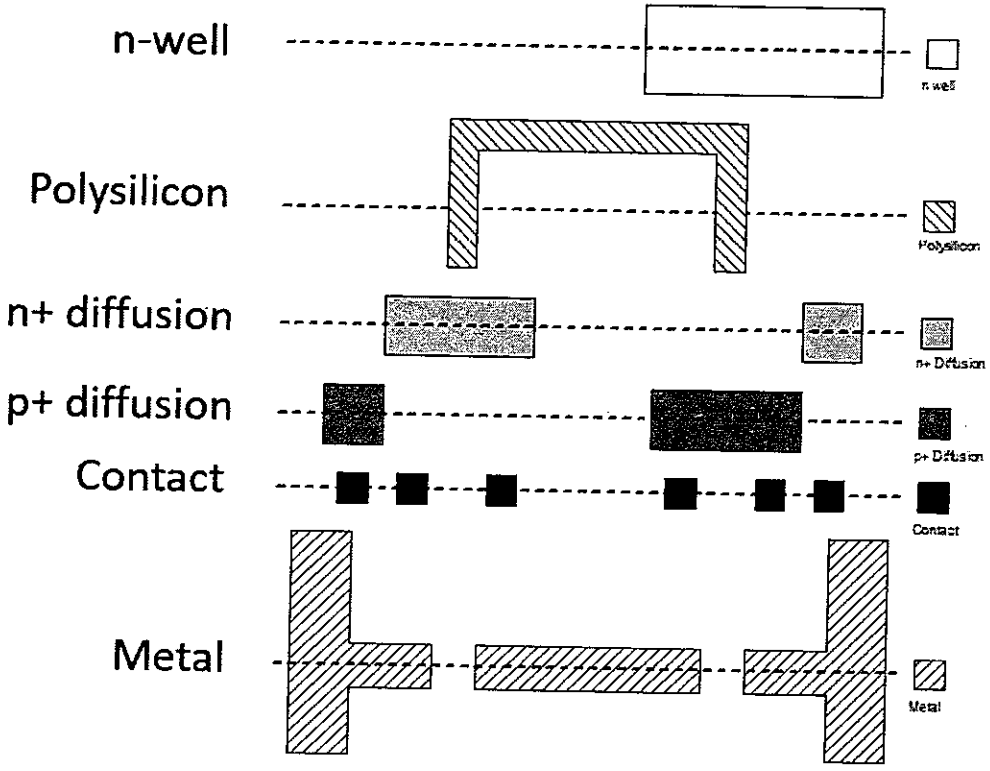

Figure 1

3. Design a digital circuit based on following specification using Verilog HDL. An 8-bit input **in** that will be inserted to the circuit one for each clock cycle. An output **out** is as follows: -

(i). If number of bit "0" in the input **in** of the current clock cycle is equal or more than number of bit "1", **x1** is the total number of bit "0". Otherwise, **x1** is the total number of bit "1".

(ii). If number of bit "0" in the input **in** of the previous clock cycle is equal or more than number of bit "1", **x2** is the total number of bit "0". Otherwise, **x2** is the total number of bit "1".

(iii). Output **out** is the difference between **x1** and **x2**.

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The circuit is positive edge triggered and synchronous reset. The circuit starts to process the input signal **in** based on positive edge triggered and also when the **rst** is equal to 1. Assume that the input signal **in** is available at every clock cycle. You may refer to Appendix A for an example of the simulation results. You may use any type of description. Needs to develop also the test bench to verify the circuit. No need to test all combinations.

(100 marks)

4. Consider a sequence detector that can detect input of "110" for the last three clock cycles . Design a digital circuit by drawing a FSM and developing Verilog HDL codes for the sequence detector based on following specification.

The inputs of the detector are as follows.

(i). A reset signal **rst** (active low) to initialize the FSM
(ii). A 1-bit input **in**
(iii). A 1-bit **clk** for the clock

The output of the detector is as follows.

(i). Output **out** that will be "1" for one clock cycle when the input **in** for the last 3 clock cycles are "110"

You may refer to Appendix B for an example of simulation results. No need to develop the test bench.

(100 marks)

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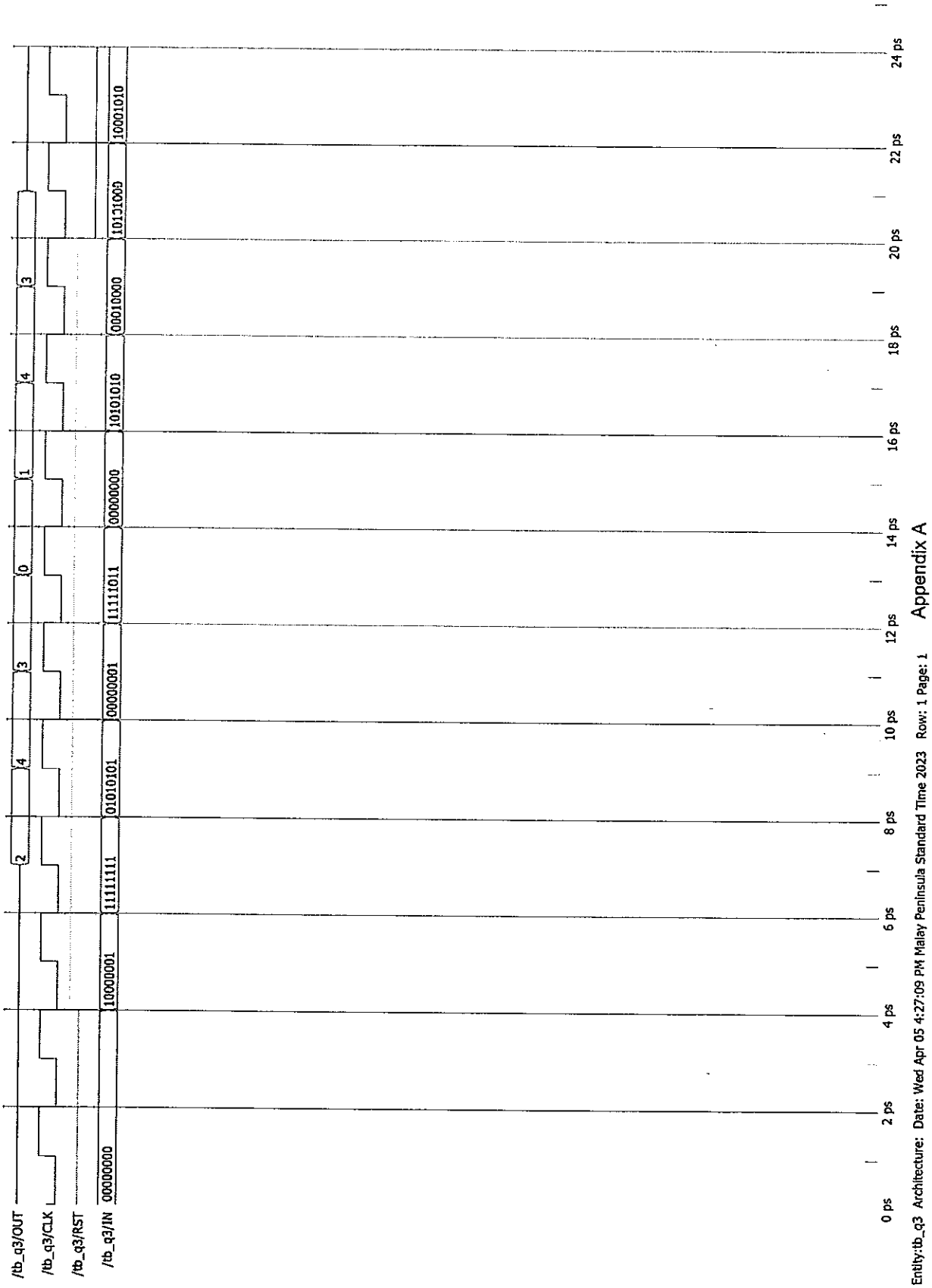
APPENDIX A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/tb_q3/RST
/tb_q3/IN
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11111111
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00010000
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0 ps
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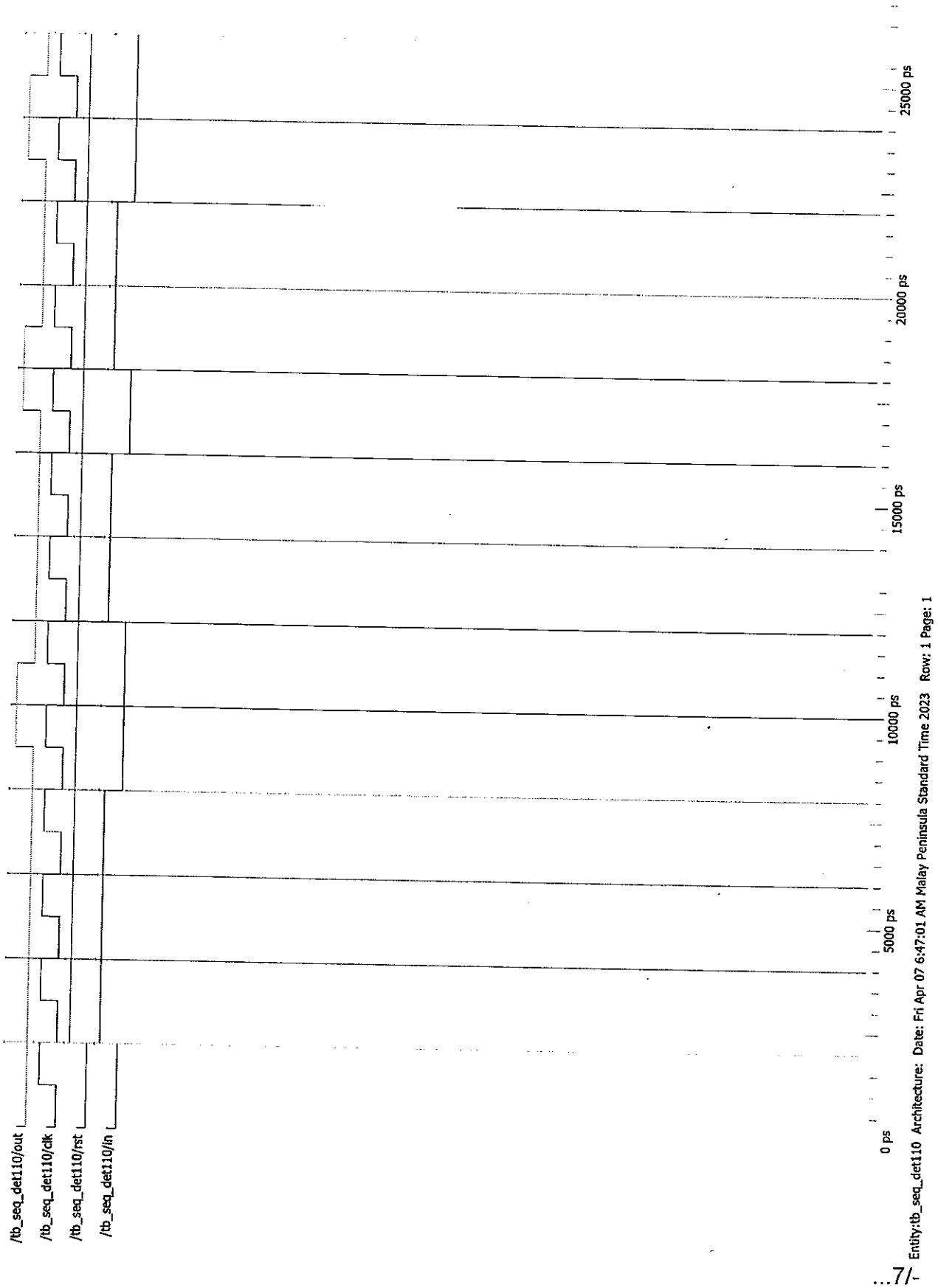
Appendix A

...6/-

APPENDIX B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/tb_seq_det110/rst
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10000 ps
15000 ps
20000 ps
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...7/-

APPENDIX C

Question	Course Outcome (CO)	Programme Outcome (PO)
1	1	PO1
2	1	PO1
3	2	PO1
4	2	PO1