UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2022/2023 Academic Session

July/August 2023

EEE344 – VLSI System

Duration : 2 hours

Please check that this examination paper consists of **NINE(9)** pages of printed material including appendices before you begin the examination.

Instructions: This paper consists of **FOUR (4)** questions. Answer **FOUR (4)** questions.

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1. a) Describe the three main components of the load capacitance C_{load}, when a logic gate is driving other fan-out gates. Sketch the equivalent circuit of the model of parasitic MOSFET capacitances.

(15 marks)

b) Refer to Figure 1.

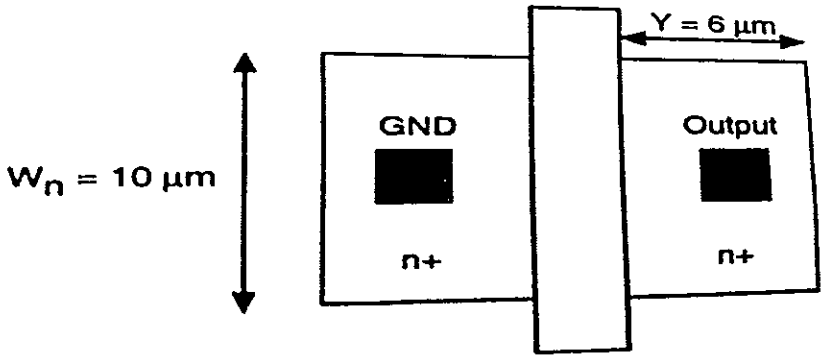

Figure 1. Layout view of a transistor

Consider the layout of an nMOS transistor shown in Figure 1. The process parameters are:

$N_D = 2 \times 10^{20}$ cm^{-3}
$N_A = 1 \times 10^{15}$ cm^{-3}
$X_j = 0.5$ µm
$L_D = 0.5$ µm
$t_{ox} = 0.05$ µm
$V_{TO} = 0.8$ V

Channel stop doping = 16.0 x (p-type substrate doping)

Find the effective drain parasitic capacitance when the drain node voltage changes from 5 V to 2.5 V.

(35 marks)

c) Consider a CMOS inverter with the following parameters:

nMOS $V_{TO,n}$ = 0.6 V
$\mu_n C_{Ox}$ = 60 $\mu A/V^2$
pMOS $V_{TO,p}$ = -0.7 V
$\mu_p C_{Ox}$ = 25 A/V^2
(W/L)n = 8
(W/L)p = 12

Calculate the noise margins and the switching threshold (V_{th}) of this circuit. The power supply voltage is V_{DD} = 3.3 V. Comment on the condition of the inverter based on the value of noise margins.

(50 marks)

2. a) Consider a CMOS inverter, which has the following device parameters.

nMOS $V_{TO,n}$ = 0.8 V
pMOS $V_{TO,p}$ = -1.0 V
$\mu_n C_{Ox}$ = 50 $\mu A/V^2$
$\mu_p C_{Ox}$ = 20 $\mu A/V^2$

The power supply voltage is V_{DD} = 5 V. Both transistors have a channel length of $L_n = L_p$ = 1 um. The total output load capacitance of this circuit is C_{out} = 2 pF, which is independent of transistors dimensions.

(i) Determine the channel width of the nMOS and the pMOS transistors such that the switching threshold voltage is equal to 2.2 V, and the output rise time is τ_{rise} = 5 ns.

(20 marks)

(ii) Calculate the average propagation delay time τ_p for the circuit designed in (i).

(20 marks)

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(iii) How do the switching threshold (V_{th}) and the delay times change if the power supply voltage is dropped from 5 V to 3.3 V. Provide the interpretation of the results.

(20 marks)

b) Consider a CMOS ring oscillator consisting of an odd number (n) of identical inverters connected in a ring configuration as shown in Figure 2. The layout of the ring oscillator is such that the interconnection (wiring) parasitics can be assumed as zero. Therefore, the delay of each stage is the same and the average gate delay is called the intrinsic delay (tp) as long as identical gates are used. The ring oscillator circuit is often used to quote the circuit speed of a particular technology using the ring oscillator frequency (*f*).

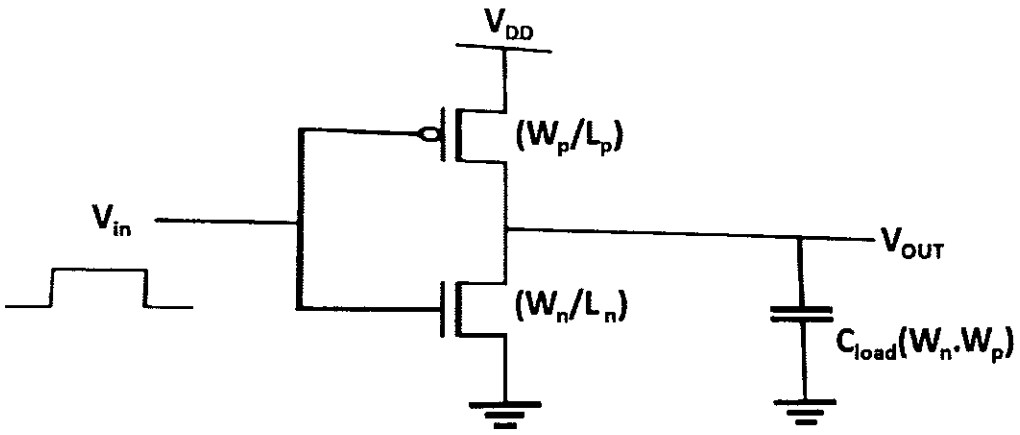

Figure 2

(i) Derive an expression for the intrinsic delay (τ_p) in terms of the number of stages *n*.

(20 marks)

(ii) Show the τ_p is independent of the transistor size, i.e. it remains the same when all gates are scaled the uniformly up or down.

(20 marks)

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3. Consider two logic functions F = A+B+C and G = A+B+C+D. Assume both true and complementary signals are available.

   a) Implement these functions in dynamic CMOS as cascaded Φ stages so as to minimize the total transistor count.

   (40 marks)

   b) Discuss any conditions under which this implementation in part a) would fail to operate properly.

   (20 marks)

   c) Design an np-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part b).

   (40 marks)

4. Consider a standard 6-T SRAM cell as shown in Figure 4. Due to Random Dopant Fluctuation (RDF), transistors in a single cell may have different threshold voltages than that of what was designed for. Assume that the cell is designed for V_{DD} = 1 V, V_{tn} = 0.3 V, and V_{tp} = -0.3 V. Consider that due to RDF, a variation of ± 30 mV in threshold voltage can happen. Clearly and concisely answer the following questions with an explanation. Write your assumptions, if any.

   a) Determine the threshold voltages of all the transistors for worst case read operation.

   (50 marks)

   b) Determine the threshold voltages of all the transistors for worst case write operation.

   (50 marks)

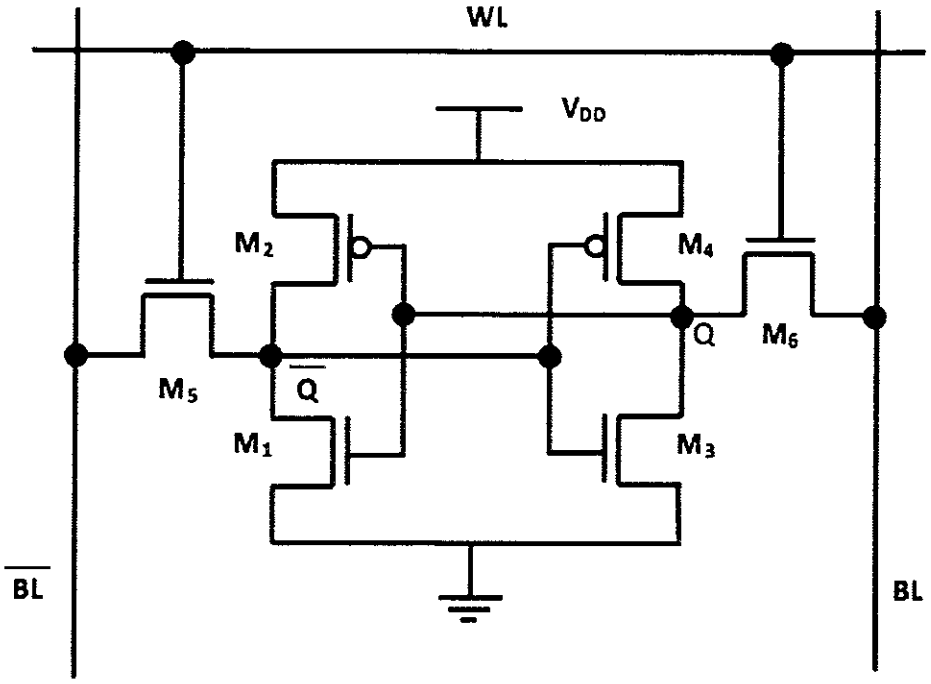

Figure 4. Standard 6-T SRAM Cell

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APPENDIX

Question	Course Outcome (CO)	Programme Outcome (PO)
1	1	PO3
2	2	PO3
3	3	PO3
4	4	PO3

...8/-

APPENDIX

Drain Current Equations for nMOSFET:

1.

$$I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad for \quad V_{GS} \geq V_T$$

$$and \quad V_{DS} < V_{GS} - V_T$$

2.

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad for \quad V_{GS} \geq V_T$$

$$and \quad V_{DS} \geq V_{GS} - V_T$$

Drain Current Equations for pMOSFET:

1.

$$I_D(lin) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad for \quad V_{GS} \leq V_T$$

$$and \quad V_{DS} > V_{GS} - V_T$$

2.

$$I_D(sat) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad for \quad V_{GS} \leq V_T$$

$$and \quad V_{DS} \leq V_{GS} - V_T$$

CMOS inverter Switching threshold.

1.

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} - |V_{T0,p}|)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

CMOS inverter Propagations delay Times:

1.

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right]$$

2.

$$\tau_{PLH} = \frac{C_{load}}{k_n(V_{DD} - |V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right]$$