Second Semester Examination
2022/2023 Academic Session

July/August 2023

EEE301 – SEMICONDUCTOR DEVICE TEST AND MEASUREMENT

Duration: 2 hours

Please ensure that this examination paper consists of SEVEN (7) pages before you begin the examination.

Instructions: This question paper consists of **FIVE (5)** questions. Answer **ALL** questions. All questions carry the same marks.

1. a) Explain the purpose(s) for performing integrated circuit (IC) testing from industry's perspectives.

(20 marks)

b) Apply the generic integrated circuit (IC) test flows (TF) to each of the three different IC types and provide a brief explanation.

(60 marks)

c) For a digital integrated circuit (IC) testing, Figure 1 shows the execution of one vector with Edge-strobe method to determine the output logic state. Explain the alternative method to determine the output voltage.

(20 marks)

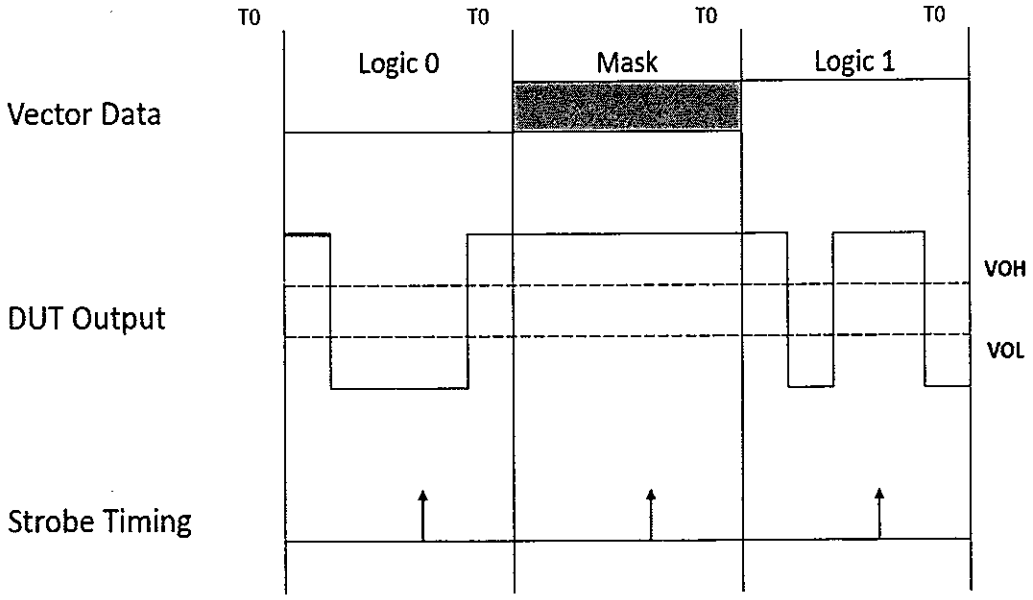

Figure 1

2. a) The test for MOSFET maximum drain current (drain-to-source leakage current) is depicted in the datasheet in Table 2.1. Apply the required test using appropriate test plan and provide a pseudo-code.

(50 marks)

Table 2.1

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	150	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120V, V_{GS} = 0V	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V			±100	nA

b) The MOSFET test plan and datasheet for drain to source ON resistance test, r_{DS}, is shown in Table 2.2. Assuming the contact resistance, R_C = 0.1 Ω, discuss the potential issues with this test plan. Given:

$$\text{Measured } V_{DSON} = I_{DSON}(2R_C) + I_{DSON}(R_{DSON})$$

(50 marks)

Table 2.2

Electrical Characteristics (T_C = 25°C unless otherwise noted)

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 9A, V_{GS} = 10V	-	0.045	0.054	Ω
		I_D = 4A, V_{GS} = 6V	-	0.050	0.075	
		I_D = 9A, V_{GS} = 10V, T_C = 175°C	-	0.126	0.146	

3. a) In a manufacturing environment of integrated circuit (IC) testing, explain the overall Test System normally implemented in the production line.

(40 marks)

b) Referring to Figure 3, assuming the input voltage is 10 V, create a complete test plan for each of the DC test instance.

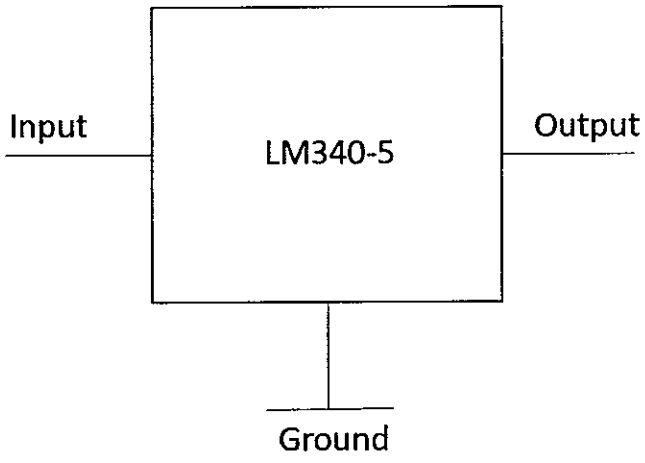

Figure 3

(i) V_{out} @ I_{load} = 0; upper and lower specification of 5.050 V and 4.950 V.

(20 marks)

(ii) V_{out} @ $I_{load} \neq 0$; upper and lower specification of 5.000 V and 4.900 V.

(20 marks)

(iii) I_{GND} @ $I_{load} \neq 0$; upper and lower specification of 18 µA V and 5 µA.

(20 marks)

4. a) The operational amplifier in Figure 4.1 might be having stability problem especially when driving capacitive loads like tester channels that have 50 to 100 pF of stray capacitances due to coaxial, PCB layout and distance. Analyze the test system and provide possible solution(s) to the mentioned problem.

(40 marks)

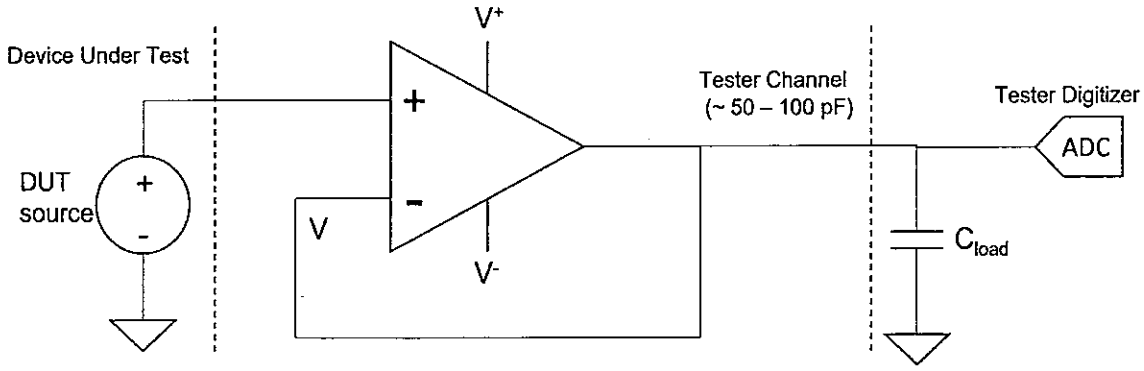

Figure 4.1

b) Refer to the Figure 4.2 on DC level testing. Apply another circuit configuration to perform V_{OH}/V_{OL} level test that can either source or sink currents (I_{OL}/I_{OH}). Explain your test procedure for V_{OL}/V_{OH} test instances.

(60 marks)

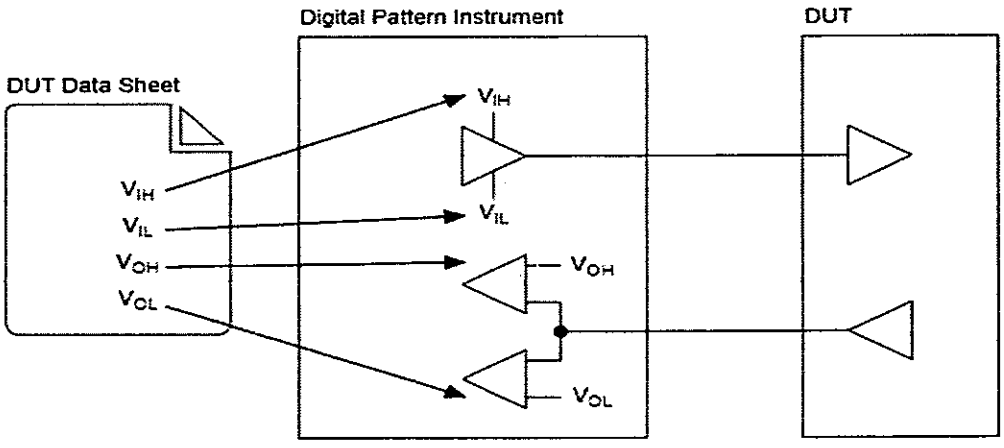

Figure 4.2

5. a) Functional tests are done in the tester (ATE) that will drive the device inputs and compare the outputs as depicted in Figure 5. Apply a simple functional test on the NAND gate by generating the Test Pattern and draw the corresponding timing diagram.

(50 marks)

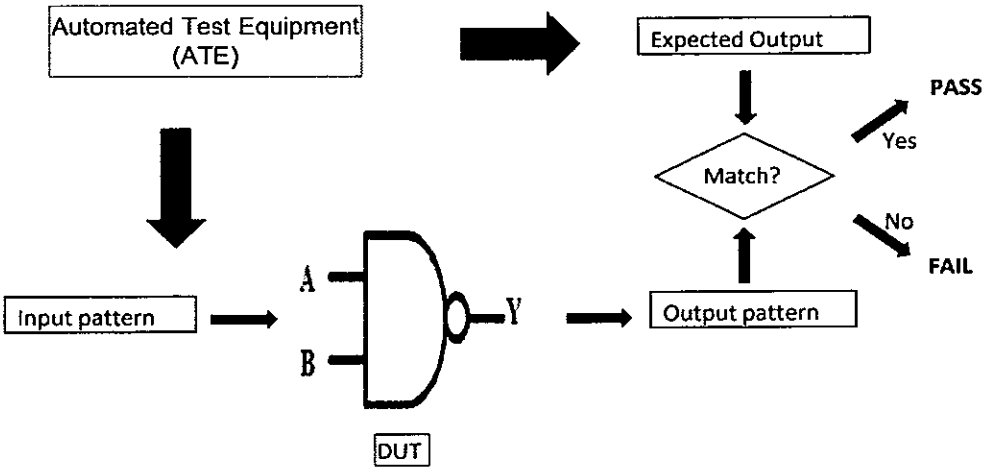

Figure 5

b) Explain the input level test of V_{IL}/V_{IH} from the datasheet in Table 5. You may use appropriate diagrams to assist in the explanation.

(50 marks)

Table 5

Electrical Characteristics

Symbol	Parameter	Test Conditions	Vcc	Min	Typ	Max	Unit
V_{IH}	Minimum high level input voltage	V_{out} = 0.1V or V_{cc} - 0.1V |Iout|< 20μA	2.0	1.5	-	-	V
			4.0	3.15	-	-	
			6.0	4.2	-	-	
V_{IL}	Maximum low level input voltage	V_{out} = 0.1V or V_{cc} - 0.1V |Iout|< 20μA	2.0	-	-	0.5	V
			4.0	-	-	1.35	
			6.0	-	-	1.8	

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APPENDIX

Question	Course Outcome (CO)	Programme Outcome (PO)
1	1	PO1
2	2	PO2
3	3	PO3
4	2	PO2
5	3	PO3