First Semester Examination
2022/2023 Academic Session

February 2023

EEE241 – (Analog Electronics I)
(Elektronik Analog I)

Duration : 3 hours
(Masa : 3 jam)

Please check that this examination paper consists of **TEN (10)** pages of printed material including an appendix before you begin the examination.

*[Sila pastikan bahawa kertas peperiksaan ini mengandungi **SEPULUH (10)** muka surat yang bercetak termasuk lampiran sebelum anda memulakan peperiksaan ini.]*

Instructions : This paper consists of **SIX (6)** questions. Answer **SIX (6)** questions.

*[**Arahan** : Kertas ini mengandungi **ENAM (6)** soalan. Jawab **ENAM (6)** soalan.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

...2/-

1. Figure 1 illustrates an op-amp. Find:

Rajah 1 menunjukkan sebuah penguat kendalian. Kira:

(a) Voltage gain in dB.

Gandaan voltan dalam dB.

(90 marks/*markah*)

(b) Input resistance.

Rintangan masukan.

(5 marks/*markah*)

(c) Output resistance.

Rintangan keluaran.

(5 marks/*markah*)

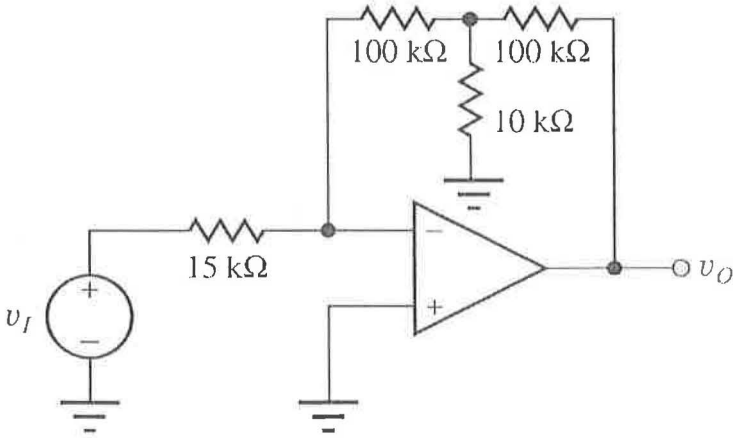

Figure 1

Rajah 1

2. Consider the circuit in Figure 2. Op amp has an open-loop gain, A_o of 90 dB, an input resistance, R_{id} of 20 kΩ, and output resistance, R_o of 1 kΩ. Assume that a signal voltage drives the op-amp with 2-kΩ source resistance, R_I and output voltage is connected to load resistance, R_L of 1-kΩ. Feedback network is implemented with R_2 = 92 kΩ and R_1 = 10 kΩ. Hence,

Pertimbangkan litar Rajah 2. Penguat kendalian mempunyai nilai gandaan gelung-terbuka, A_o sebanyak 90 dB, rintangan masukan, R_{id} 20 kΩ dan juga rintangan keluaran, R_o sebanyak 1 kΩ. Anggap bahawa penguat kendalian tersebut dipacu oleh isyarat voltan masukan dengan rintangan sumber, R_I bernilai 2-kΩ, dan isyarat voltan keluaran dihubungkan kepada rintangan beban, R_L 1-kΩ. Jaringan suapbalik diimplementasi menggunakan rintangan-rintangan R_2 = 92 kΩ dan R_1 = 10 kΩ. Maka,

(a) Find closed-loop gain of the circuit, A_v.

Dapatkan gandaan gelung-tertutup bagi litar, A_v.

(60 marks/*markah*)

(b) Draw the circuit for finding the R_{in}^{D} based on Figure 2. Then, find input resistance of the circuit, R_{in}.

Lakarkan litar untuk mencari R_{in}^{D} berdasarkan Rajah 2. Kemudian dapatkan rintangan masukan litar, R_{in}.

(40 marks/*markah*)

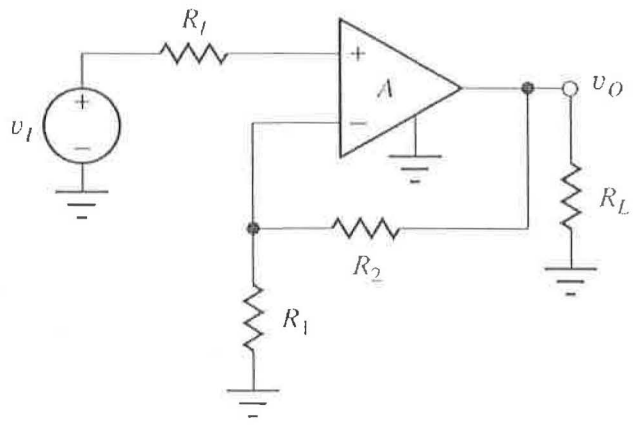

Figure 2

Rajah 2

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3.

(a) Design an inverting amplifier with A_v = 43 dB that can deliver a 15-V signal to a 5-$k\Omega$ load resistor. Your op-amp can supply only 4 mA of output current. Use standard resistor 5% values in your design. Calculate:

Reka bentuk penguat penyongsangan dengan Av = 43 dB yang boleh menghantar isyarat 15-V kepada perintang beban 5-kΩ. Op-amp anda boleh membekalkan hanya 4 mA arus keluaran. Gunakan nilai 5% perintang standard dalam reka bentuk anda. Kira:

(i). The minimum resistance of R_1 and R_2 that could satisfy the design requirement.

Rintangan minimum R1 dan R2 yang boleh memenuhi keperluan reka bentuk.

(25 marks/*markah*)

(ii). The final gain of your design.

Gandaan akhir reka bentuk anda.

(25 marks/*markah*)

Use Appendix B for the resistor's values.

Guna Apendik B untuk dapatkan nilai rintangan perintang.

(b) Calculate the voltage (V = V1 − V2) appearing across the 10 $k\Omega$ resistor in Figure 3. Then find:

Kira voltan (V = V1 − V2) yang terdapat pada perintang 10 kΩ dalam Rajah 3. Kemudian cari:

(i). Value of V.

Nilai V.

(10 marks/*markah*)

(ii). Common-mode voltage associated with V (VCM = (V1 + V2)/2).

Voltan mod-sepunya yang dikaitkan dengan V (VCM = (V1 + V2)/2).

(20 marks/*markah*)

(iii). CMRR value required by the voltmeter if we are to measure V with an error of less than 0.01%.

CMRR yang diperlukan oleh voltmeter jika kita hendak mengukur V dengan ralat kurang daripada 0.01%.

(20 marks/*markah*)

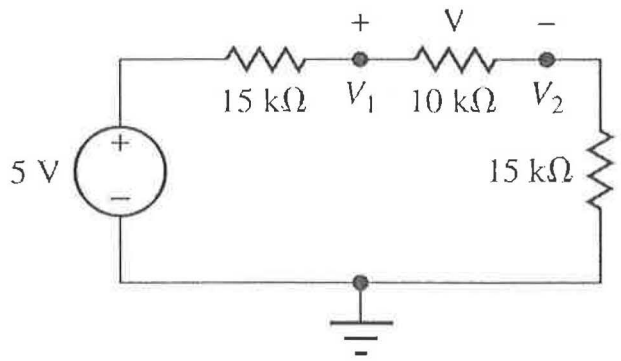

Figure 3

Rajah 3

4. For the circuit in Figure 4, R_E = 0.6 kΩ, R_C = 5.6 kΩ, β = 120, $V_{BE\ (on)}$ = 0.7 V, V_T = 26 mV, R_1 = 250 kΩ, and R_2 = 75 kΩ.

Untuk litar dalam Rajah 4, R_E = 0.6 kΩ, R_C = 5.6 kΩ, β = 120, $V_{BE\ (on)}$ = 0.7 V, V_T = 26 mV, R_1 = 250 kΩ, dan R_2 = 75 kΩ.

(a) For V_A = ∞, sketch the small-signal equivalent circuit and determine the small-signal voltage gain, Av.

Untuk V_A = ∞, Lukis litar setara isyarat kecil dan tentukan gandaan voltan, Av litar isyarat kecil.

(50 marks/*markah*)

(b) Determine the input resistance looking into the base of the transistor.

Tentukan rintangan masukan melihat ke dalam tapak transistor.

(10 marks/*markah*)

(c) For $V_A = \infty$, if a bypass capacitor is added in parallel with the emitter resistor, redraw the small signal equivalent circuit and calculate the voltage gain. Comment on the difference in the voltage gain with and without a bypass capacitor.

Untuk $V_A = \infty$, jika kapasitor pintasan ditambah selari dengan perintang pemancar, lukis semula litar setara isyarat kecil dan kirakan semula gandaan voltan. Ulas tentang perbezaan keuntungan voltan dengan dan tanpa kapasitor pintasan.

(40 marks/*markah*)

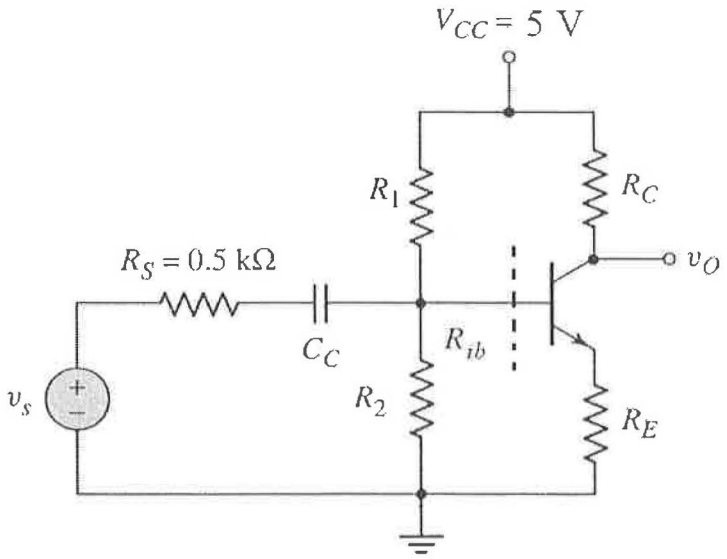

Figure 4

Rajah 4

5.

(a) For the NMOS common-source amplifier in Figure 5.1, the transistor parameter threshold voltage, V_{TN} = 0.6 V, conduction parameter, K_n = 0.5 mA/V^2, channel length modulation parameter, λ = 0, base resistance R_1 = 1 MΩ, base resistance R_2 = 250 kΩ, source resistance, R_S = 2 kΩ and drain resistance, R_D = 10 kΩ. Determine:

Untuk penguat sumber biasa NMOS dalam Rajah 5.1, voltan ambang parameter transistor, V_{TN} = 0.6 V, parameter pengaliran, Kn = 0.5 mA/V^2, parameter modulasi panjang saluran, λ = 0, rintangan asas R_1 = 1 MΩ, rintangan asas R_2 = 250 kΩ , rintangan punca, R_S = 2 kΩ dan rintangan longkang, R_D = 10 kΩ. Tentukan:

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(i). Quiescent point (Q-point) values of I_{DQ} and V_{DSQ}.

Nilai titik senyap (Q-point) bagi I_{DQ} dan V_{DSQ}.

(40 marks/*markah*)

(ii). Small-signal voltage gain, Av.

Gandaan voltan, Av litar isyarat kecil.

(10 marks/*markah*)

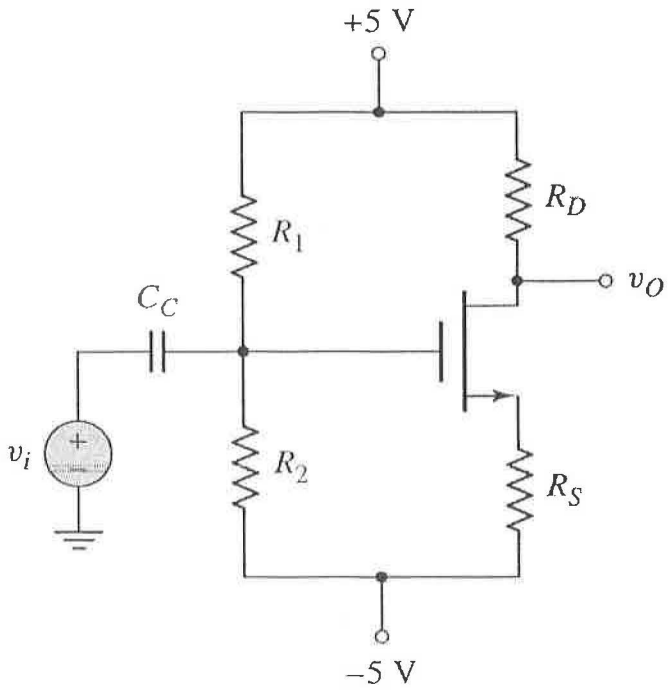

Figure 5.1

Rajah 5.1

(b) The transistor parameters for the circuit in Figure 5.2 are V_{TN} = 0.4 V, K_n = 0.5 mA/V^2 and λ = 0. The circuit elements are V_{DD} = 3 V and R_i = 300 kΩ.

Parameter transistor untuk litar dalam Rajah 5.2 ialah V_{TN} = 0.4 V, K_n = 0.5 mA/V^2 dan λ = 0. Bacaan litar ialah V_{DD} = 3 V dan R_i = 300 kΩ.

(i). Determine the values of R_S, R_1 and R_2 of the circuit with the value of I_{DQ} = 0.25 mA and V_{DSQ} = 1.5 V.

Tentukan nilai R_S, R_1 dan R_2 litar dengan nilai I_{DQ} = 0.25 mA dan V_{DSQ} = 1.5 V.

(40 marks/*markah*)

(ii). Determine the small-signal voltage gain, A_v.

Tentukan gandaan voltan, Av litar isyarat kecil.

(10 marks/*markah*)

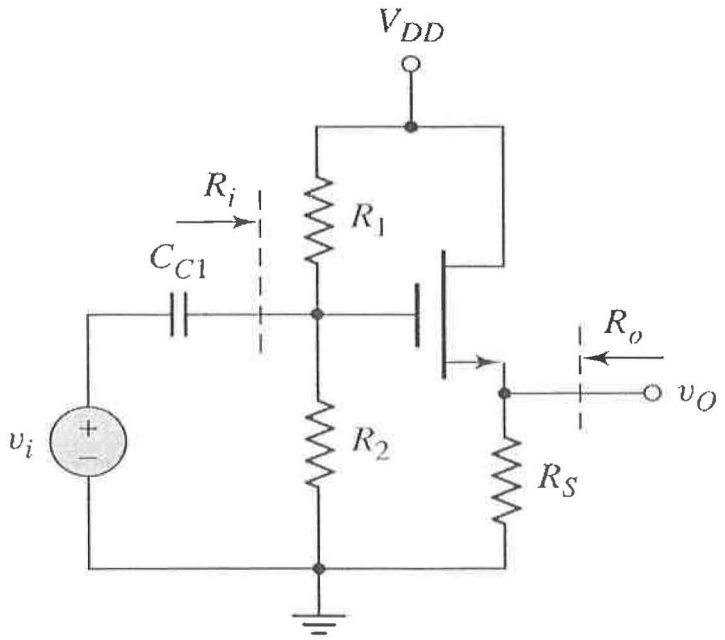

Figure 5.2

Rajah 5.2

6. Figure 6 illustrates a type of amplifier operating with of g_m = 0.6 mS, R_I = 50 Ω, R_4 = 3 kΩ and R_L = 82 kΩ. Calculate the following:

Rajah 6 menunjukkan sejenis penguat beroperasi dengan g_m = 0.6 mS, R_I = 50 Ω, R_4 = 3 kΩ dan R_L = 82 kΩ. Hitung yang berikut:

(a) The input resistance, R_{in} and output resistance R_{out}.

Rintangan dalaman, R_{in} dan rintangan luaran R_{out}.

(7 marks/*markah*)

(b) The voltage gain, A_v.

Gandaan voltan, A_v.

(35 marks/*markah*)

(c) The current gain, A_i.

Gandaan arus, A_i.

(35 marks/*markah*)

(d) What is the small signal limit for the value of v_i in this circuit?

Apakah batasan isyarat kecilan bagi v_i dalam litar ini?

(23 marks/*markah*)

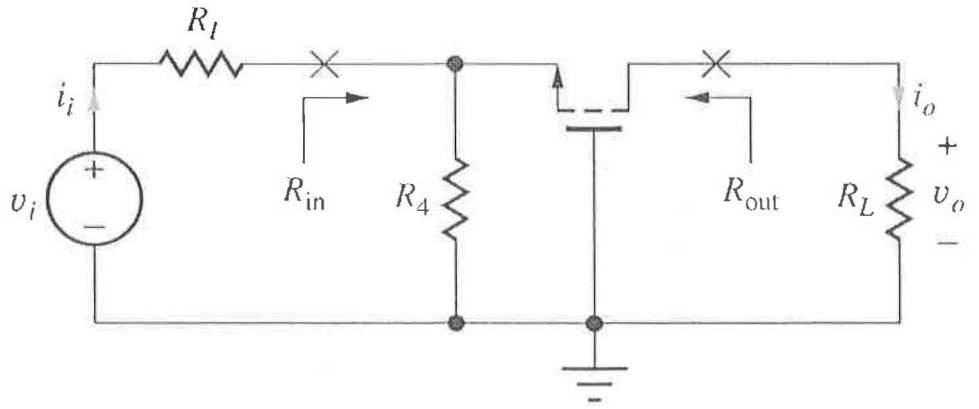

Figure 6

Rajah 6

APPENDIX A

LAMPIRAN A

Question	Course Outcome (CO)	Programme Outcome (PO)
1	1	1
2	1	1
3	1	1
4	1	1
5	1	1
6	1	1

APPENDIX B

LAMPIRAN B

Standard resistor values (All values available with a 5 percent tolerance. Bold values are available with 10 percent tolerance.)

				Ω				MΩ	
1.0	**5.6**	**33**	**180**	**1000**	**5600**	**33000**	**180000**	**1.0**	**5.6**
1.1	6.2	36	200	1100	6200	36000	200000	1.1	6.2
1.2	**6.8**	**39**	**220**	**1200**	**6800**	**39000**	**220000**	**1.2**	**6.8**
1.3	7.5	43	240	1300	7500	43000	240000	1.3	7.5
1.5	**8.2**	**47**	**270**	**1500**	**8200**	**47000**	**270000**	**1.5**	**8.2**
1.6	9.1	51	300	1600	9100	51000	300000	1.6	9.1
1.8	**10**	**56**	**330**	**1800**	**10000**	**56000**	**330000**	**1.8**	**10**
2.0	11	62	360	2000	11000	62000	360000	2.0	11
2.2	**12**	**68**	**390**	**2200**	**12000**	**68000**	**390000**	**2.2**	**12**
2.4	13	75	430	2400	13000	75000	430000	2.4	13
2.7	**15**	**82**	**470**	**2700**	**15000**	**82000**	**470000**	**2.7**	**15**
3.0	16	91	510	3000	16000	91000	510000	3.0	16
3.3	**18**	**100**	**560**	**3300**	**18000**	**100000**	**560000**	**3.3**	**18**
3.6	20	110	620	3600	20000	110000	620000	3.6	20
3.9	**22**	**120**	**680**	**3900**	**22000**	**120000**	**680000**	**3.9**	**22**
4.3	24	130	750	4300	24000	130000	750000	4.3	
4.7	**27**	**150**	**820**	**4700**	**27000**	**150000**	**820000**	**4.7**	
5.1	30	160	910	5100	30000	160000	910000	5.1	

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