UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2022/2023 Academic Session

July/August 2023

EEE133 – Electronic Devices and Circuits

Duration : 3 hours

Please check that this examination paper consists of **NINE (9)** pages of printed material including appendix before you begin the examination.

Instructions : This paper consists of **FOUR (4)** questions. Answer **ALL** questions.

1. a) Figure 1.1 illustrates the bonding diagram of a doped silicon. Si is silicon atom whereas B is the doped atom. Based on Figure 1.1, answer the followings:

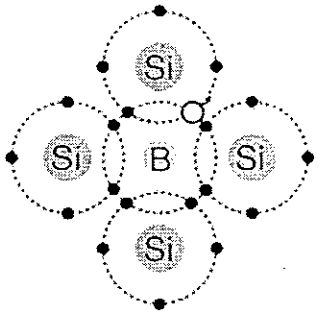

Figure 1.1 Bonding diagram of a doped silicon.

i. Sketch the energy band diagram of the doped silicon.

ii. Redraw Table 1 and fill in the blanks.

Table 1. Doped silicon parameters

Doped Silicon Parameters	
Impurity type	
Majority carriers	
Minority carriers	
Type of fixed charges	

(20 marks)

b) A silicon sample is doped with phosphorus with concentration of 5×10^{14} cm^{-3}. At room temperature the intrinsic carrier concentration of silicon is 9.65×10^{9} cm^{-3}, electron and hole mobility, μ_e = 1400 cm^2/Vs and μ_h = 450 cm^2/Vs respectively. Find the conductivity of the doped material by

taking into account both majority and minority carrier contributions. Based on your results, comment on the significance of minority carrier contributions as compared to majority carriers.

(30 marks)

c) An abrupt silicon P-N junction with doping concentrations of N_A = 3.5 x 10^{16} cm^{-3} and N_D = 4.5 x 10^{16} cm^{-3} respectively is biased at V = 0.7 V. Determine the ideal forward current assuming that the N-type region is much smaller than the minority carrier diffusion length with a length of l_n = 1 µm and assuming a "long" P-type region, sufficiently enough for the minority carriers to diffuse in. Use carrier mobility values of μ_e = 1350 cm^2 /Vs and μ_h = 550 cm^2 /Vs for electron and hole, respectively, in your calculation. The minority carrier lifetime in P-type is given as 60 µs and the height of the structure = width of the structure = 100 µm. Intrinsic carrier density is 1 x 10^{10} cm^{-3}. Discuss what happens to the forward current when the voltage is increased even further under same temperature environment. Will the saturation current change?

(50 marks)

2. a) Assuming that the diodes are identical, determine I, I_{D1}, I_{D2} and V_{OUT} in Figure 2.1 under the following conditions:

i. The diodes are assumed to be ideal;

ii. The potential barrier, V_O of the diodes are considered (where V_O = 0.7 V);

iii. The potential barrier, V_O and the internal resistance, r_d of the diodes are considered (where V_O = 0.7 V and r_d = 10 Ω).

(60 marks)

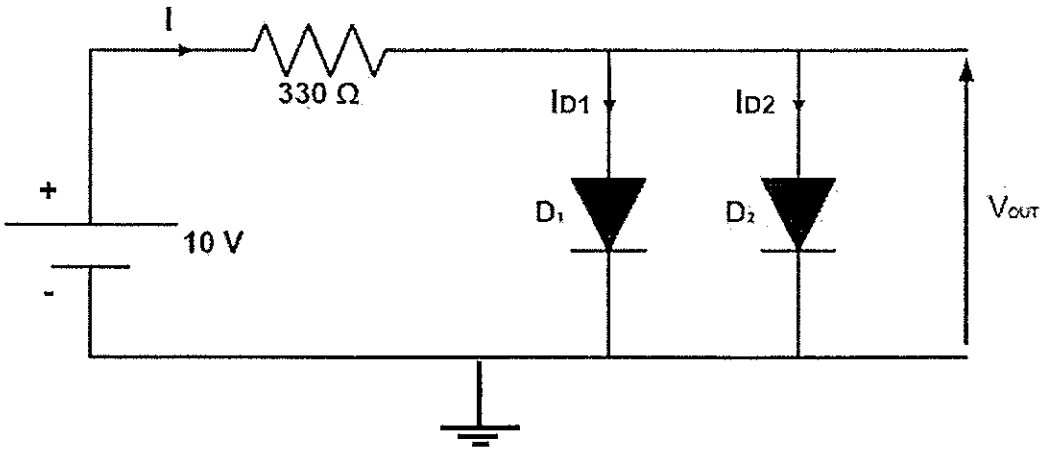

Figure 2.1

b) Figure 2.2 shows the full wave voltage rectification from the output of the transformer using bridge configuration. Assuming that the diodes are identical and they all have a potential barrier, V_O = 0.7 V, determine:

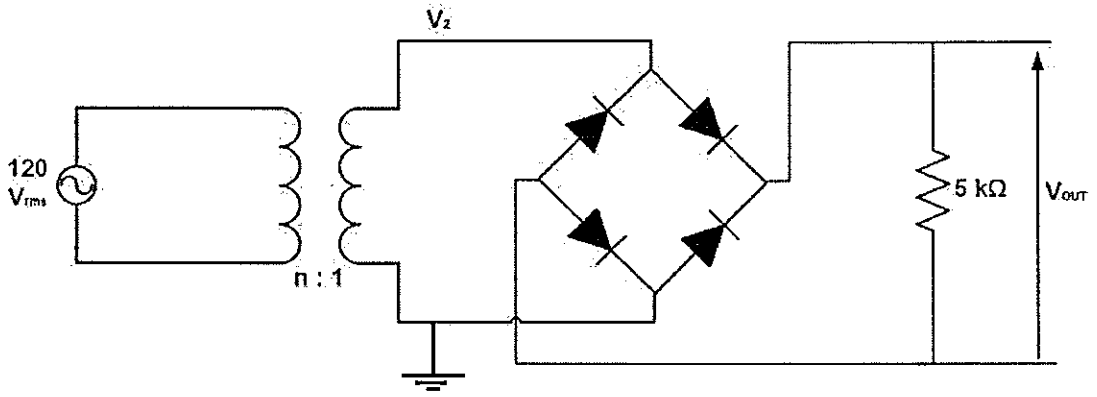

Figure 2.2

i. The value of turns, n required to give a voltage of amplitude 5 V at V_2 (n should be rounded to an integer).

ii. The peak voltage at the output, V_{OUT} for V_2 = 5 V.

iii. The peak current flowing through any of the diodes.

(25 marks)

c) By referring to Figure 2.3, state;

i. The name of the circuit;

ii. The function of the circuit;

iii. The main application of the circuit.

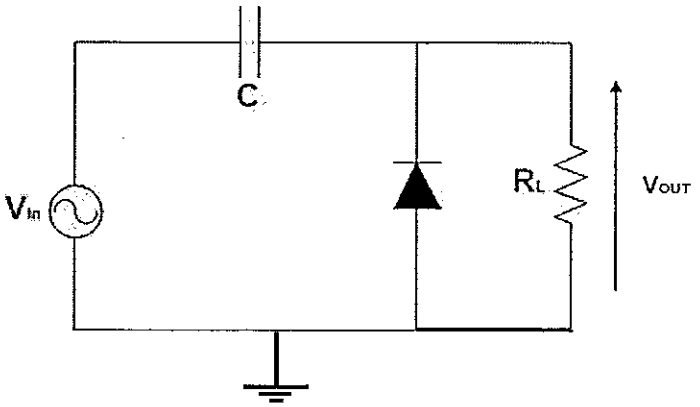

Figure 2.3

(15 marks)

3. Figure 3.1 shows the npn transistor circuit with $\beta = 100$. Given $V_{CC} = 10$ V, $R_C = 2$ kΩ, $V_{BE} = 0.7$ V, $V_{BE\,(sat)} = 0.8$ V, and $V_{CE\,(sat)} = 0.2$ V,

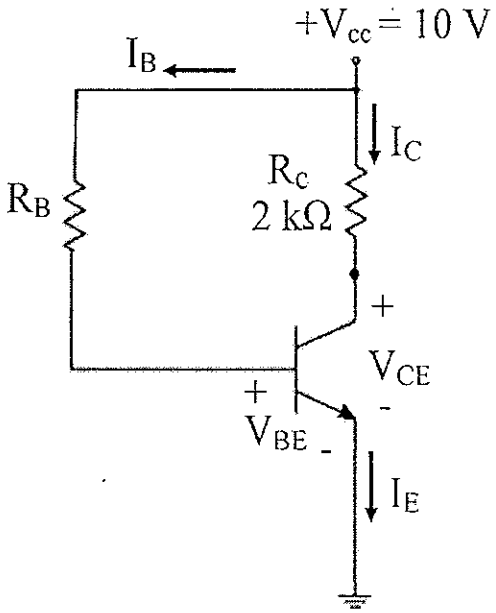

Figure 3.1

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a) Determine the region of operation (i.e., active or saturation) and the values of $I_B, I_C,$ and V_{CE} for:

i. $R_B = 500\ \text{k}\Omega$

(25 marks)

ii. $R_B = 120\ \text{k}\Omega$

(30 marks)

b) Consider the circuit of Figure 3.1 with $R_B = 500\ \text{k}\Omega$, sketch the DC load line and determine its operating point (Q-point). Then, calculate the new operating point if β is changed to 150.

(25 marks)

c) You are to bias an NPN transistor to function as an amplifier. The requirement is for the the NPN to be maintained or stable in the forward active region throughout its operation. Sketch and label the circuit of the two biasing techniques that you know which can fulfill this application.

(20 marks)

4. a) Compare and list four differences between BJT and FET.

(20 marks)

b) An N-channel JFET fixed-bias amplifier circuit as shown in Figure 4.1 has a voltage supply $V_{GG} = 2\ V$ and $V_{DD} = 10\ V$. Given $R_D = 1\ \text{k}\Omega$, $R_G = 1\ \text{M}\Omega$, $I_{DSS} = 8\ mA$ and $V_{GS(off)} = -5\ V$, determine the values of I_D and V_{DS}.

(30 marks)

c) Calculate the values of V_{GS}, K, I_D, and V_{DS} for the E-MOSFET circuit shown in Figure 4.2. Given that $I_{D(on)} = 3\ mA$, $V_{GS} = 4\ V$, $V_{GS(th)} = 2\ V$, and $V_{DD} = 10\ V$.

(50 marks)

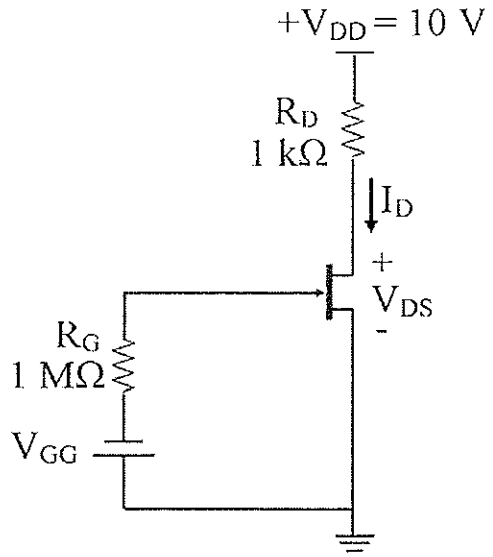

Figure 4.1

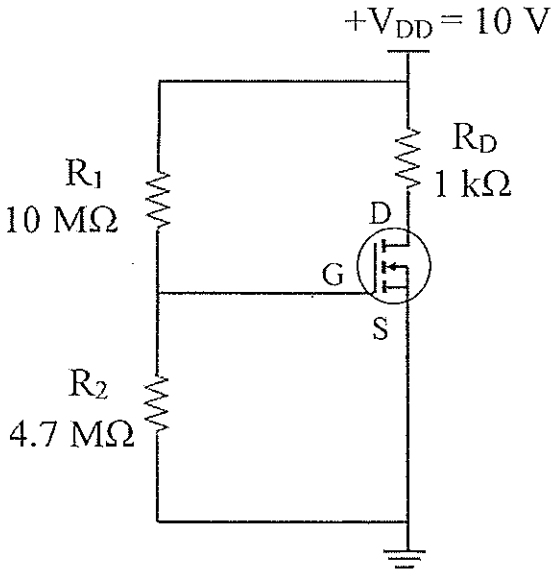

Figure 4.2

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APPENDIX I

Electronic charge, $q = 1.6 \times 10^{-19} C$

Room temperature, $27°C = 300K$

Thermal voltage, $V_T = \frac{kT}{q} \approx 26mV$

Carrier velocity, $u = \mu E$

Conductivity of material, $\sigma = nq\mu_e + pq\mu_h$

Current density, $J = (nq\mu_e + pq\mu_h)E$

*Hole current in n-type semiconductor, $I_{pn} = \frac{AqD_p p_n}{L_p}\left(e^{\frac{V}{V_T}} - 1\right)$

*Electron current in p-type semiconductor, $I_{np} = \frac{AqD_n n_p}{L_n}\left(e^{\frac{V}{V_T}} - 1\right)$

Diode current, $I = I_S\left(e^{\frac{V}{V_T}} - 1\right)$

*Note: the expressions are for the assumption that the minority carrier diffusion length is shorter than the length of the substrate.

APPENDIX II

Question	Course Outcome (CO)	Programme Outcome (PO)
1	1	PO1
2	2	PO2
3	3	PO1
4	4	PO2