UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2022/2023 Academic Session

July/August 2023

EEE130 – Digital Electronic I

Duration: 3 hours

Please check that this examination paper consists of **TWENTY (20)** pages of printed material including appendix before you begin the examination.

Instructions:

(i) This paper consists of **TWO (2)** Parts – Part A and Part B. Each part consists of TWO (2) questions. Answer all **FOUR (4)** questions.

(ii) Answer **Questions 1** and **2** in the **answer booklet**.

(iii) **Question 3** must be answered in **Appendix B**, while **Question 4** must be answered in **Appendix C**. Attach both appendices with your answer booklet.

PART A

Part A consists of Questions 1 and 2. You must answer both questions. Answer Questions 1 and 2 in the answer booklet.

1. (a) Based on Figure 1.1, answer the following questions:

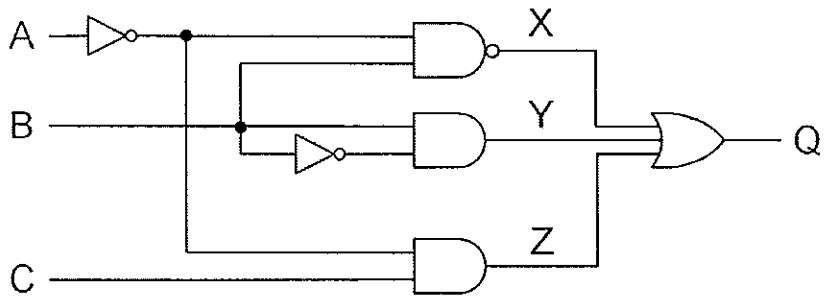


Figure 1.1

(i) Write the Boolean expression for the output Q, as it is drawn in the circuit. Then, **using Boolean algebra**, simplify Q to its simplest sum-of-product (SOP) form. Draw the final circuit.

(40 marks)

(ii) If the input sequence in the timing diagram in Figure 1.2 is applied to the circuit, draw the resulting waveform for output Q. **Show also the waveforms for X, Y and Z.**

(30 marks)

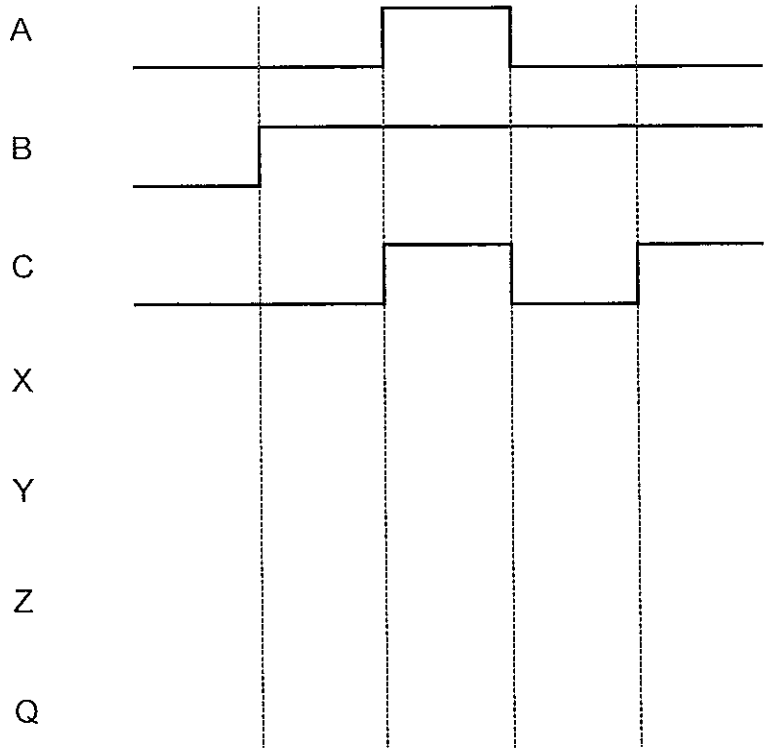


Figure 1.2

(b) The input sequence in the timing diagram in Figure 1.3 is applied to the circuit in Figure 1.4. Draw the resulting waveform for output K and show also the waveforms for G and H.

(30 marks)

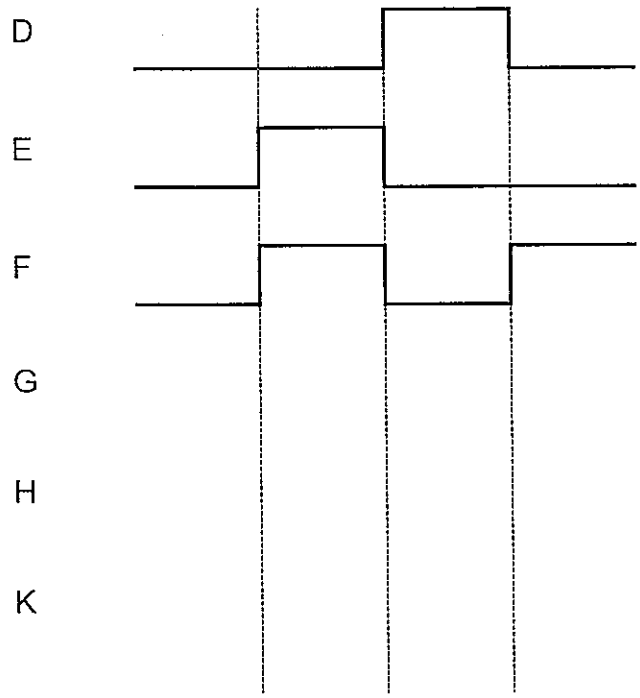


Figure 1.3

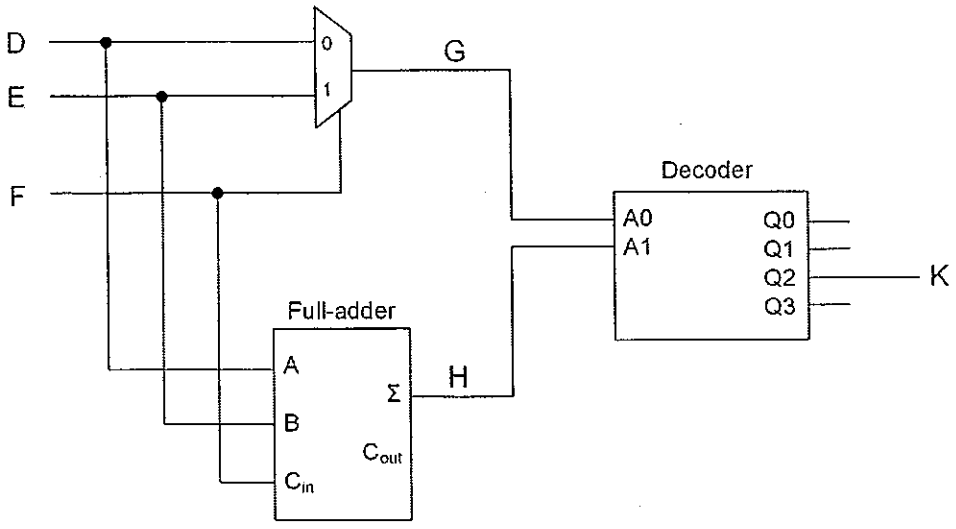


Figure 1.4

2. (a) Based on the truth table in Table 2.1, design a circuit that will implement the **minimal sum-of-product (SOP)** of the function. Draw the resulting AND-OR circuit. Assume that complemented inputs are available.

(30 marks)

Table 2.1

A	B	C	D	Output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

(b) A seven-segment display is shown in Figure 2.1. For a binary-coded-decimal (BCD) input W, X, Y, Z, design a circuit that will output a HIGH when the input corresponds to a number that will light up the segment circled in Figure 2.1. Assume that inputs that do not occur in the BCD sequence are "don't care"s. Your circuit must implement the **minimal product-of-sum (POS)** of the function. Draw your circuit. Assume that complemented inputs are available.

(40 marks)

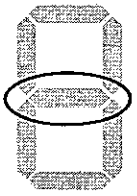


Figure 2.1

(c) Design a circuit that will implement the Boolean expression below, using only **one 8-to-1 multiplexer**. Hint: Begin by writing the truth table.

$$\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + AB$$

(30 marks)

PART B

Part B consists of Questions 3 and 4. You must answer both questions. Question 3 must be answered in Appendix B, while Question 4 must be answered in Appendix C. Please attach both appendices with your answer booklet.

3. (a) Identify whether the following statements are true or false. Briefly explain your answer. Provide your answer in Table B.1 in Appendix B.

(i) For an S-R latch constructed using NAND gates, the invalid state occurs when $S = R = 1$, which produces $Q = \bar{Q} = 1$.

(10 marks)

(ii) A 2-bit asynchronous counter and 6-bit synchronous counter are constructed using J-K flip-flops. The propagation delay of each J-K flip-flop is 10 ns. The constructed 2-bit asynchronous counter has higher propagation delay as compared to that of the constructed 6-bit synchronous counter.

(10 marks)

(iii) An asynchronous counter needs 9 J-K flip-flops to count up to 256_{10}.

(10 marks)

(iv) For the same number of flip-flops, the number of states for a Ring Counter is twice that of a Johnson Counter.

(10 marks)

(b) Based on Figure 3.1, fill in the truth table shown in Table B.2 in Appendix B.

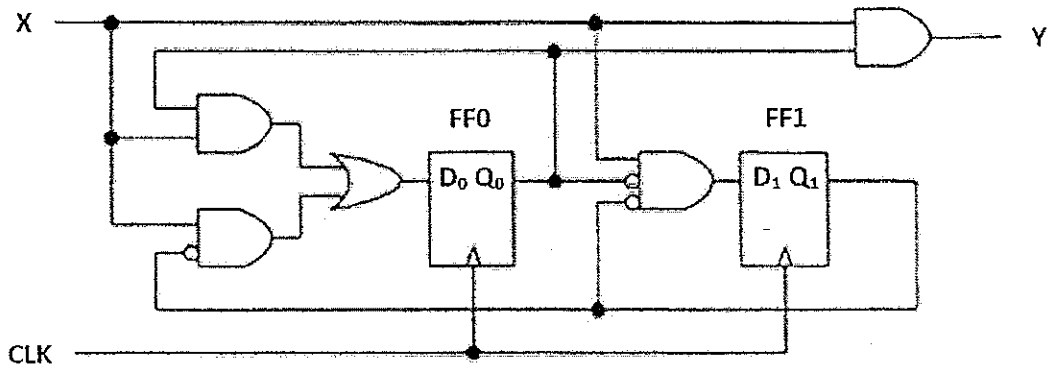


Figure 3.1

(24 marks)

(c) Figure 3.2 shows a block diagram of a mod-N asynchronous counter constructed using 8-bit asynchronous counter with J-K flip-flops. The $\overline{PRE}$ and $\overline{CLR}$ are used to PRESET and CLEAR all J-K flip-flops respectively. Based on this figure, answer the following questions:
(Note: Provide your answer in Table B.3 in Appendix B.)

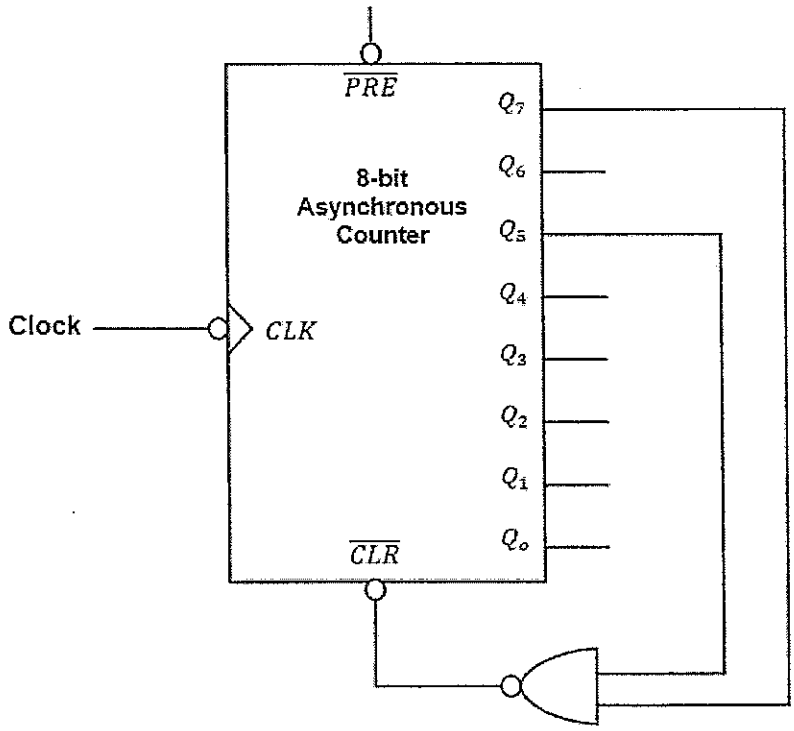


Figure 3.2

(i) Determine the value of N.

(8 marks)

(ii) If the counter is holding the count 01010101_2, what will be the count in binary after 80 clock pulses?

(10 marks)

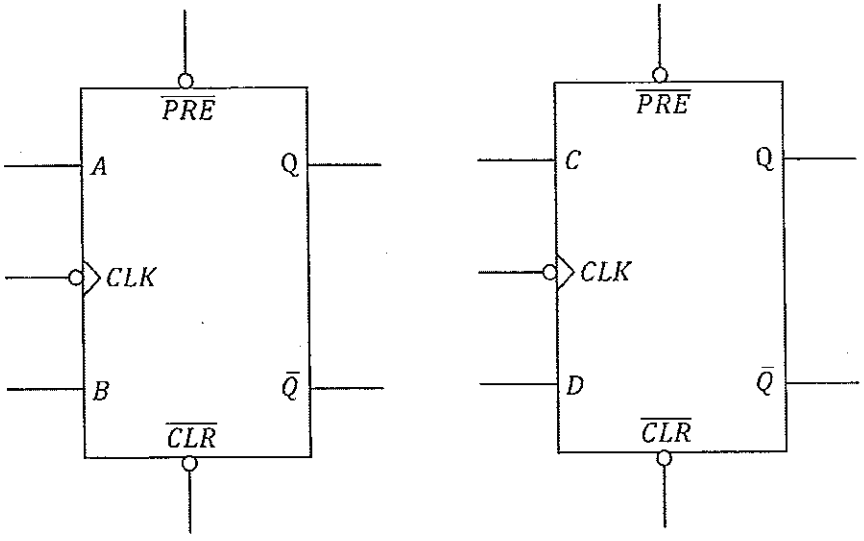
(ii) If the clock period is 25 μs, determine the frequency of the output of MSB.

(10 marks)

(iii) If the propagation delay of each J-K flip-flop is 6 ns, determine the propagation delay for the mod-N asynchronous counter.

(8 marks)

4. (a) Figures 4.1(a) and (b) show block diagrams of two new flip-flops known as A-B and C-D flip-flops respectively. Tables 4.1(a) and (b) tabulate the truth table of A-B and C-D flip-flops respectively. Based on this information, answer the following questions. Provide your answer in Appendix C.



(a) (b)

Figure 4.1

Table 4.1

(a)

Input		Output
A	B	Q^+
0	0	Toggle
0	1	Set
1	0	Reset
1	1	No change

(b)

Input		Output
C	D	Q^+
0	0	Set
0	1	Invalid
1	0	Toggle
1	1	Reset

(i) Fill in the excitation tables shown in Table C.1(a) and (b) in Appendix C for A-B and C-D flip-flops respectively.

(16 marks)

(ii) Design A-B flip-flop from C-D flip-flops. Follow the procedures as stated in Appendix C – Question 4(a)(ii).

(27 marks)

(iii) C-D flip-flops are used to design a mod-4 asynchronous counter. Sketch the circuit in Figure C.1 in Appendix C. You may use all or some of the C-D flip-flops in the figure.

(17 marks)

(b) Figure 4.2 shows a block diagram of 74LS93 4-bit asynchronous counter IC. By cascading two 74LS93 4-bit asynchronous counter ICs, you are required to design a Mod-M asynchronous counter with the specifications tabulated in Table 4.2. Based on this information, answer the following questions:

(i) What is the type of flip-flop used in the IC? Briefly explain your answer.

(10 marks)

(ii) Based on the specifications tabulated in Table 4.2, determine the value of M.

(10 marks)

(iii) Draw the circuit of the Mod-M asynchronous counter in Figure C.2 in Appendix C. You are not allowed to use any external gates. Please clearly assign LSB and MSB.

(20 marks)

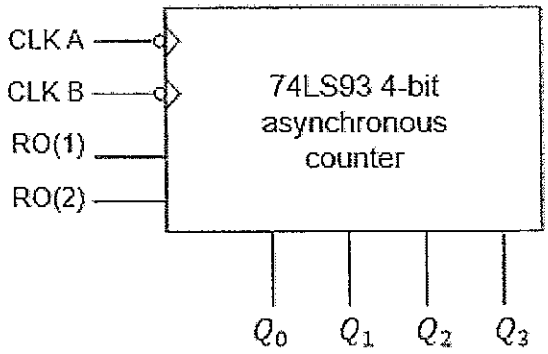


Figure 4.2

Table 4.2

Specifications	Values
Clock frequency	144 kHz
Frequency of MSB	750 Hz

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APPENDIX A

Question	Course Outcome (CO)	Programme Outcome (PO)
1	1	PO1
2	2	PO2
3	3	PO1
4	4	PO2

APPENDIX B

Answer sheet for Question 3. Please attach with your answer booklet.

Question 3(a)

Table B.1

Ques-tion	True or False	Explanation/reasons
(i)		
(ii)		
(iii)		
(iv)		

Question 3(b)

Table B.2

Input	Present State		Next State		Output
X	Q_1	Q_0	Q_1^+	Q_0^+	Y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Question 3(c)

Table B.3

Question	Your Answer
(i)	The value of N = _____
(ii)	
(iii)	
(iv)	

APPENDIX C

Answer sheet for Question 4. Please attach with your answer booklet.

Question 4(a)(i)

Table C.1

(a)

Present state	Next state	Inputs	
Q	Q^+	A	B
0	0		
0	1		
1	0		
1	1		

(b)

Present state	Next state	Inputs	
Q	Q^+	C	D
0	0		
0	1		
1	0		
1	1		

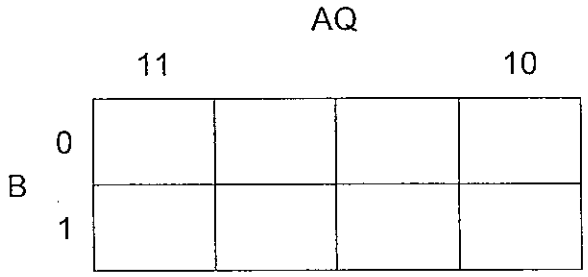
Question 4(a)(ii)

Step 1: Transition table

Inputs for A-B flip-flop		Present state	Next state	Inputs for C-D flip-flop	
A	B	Q	Q^+	C	D
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

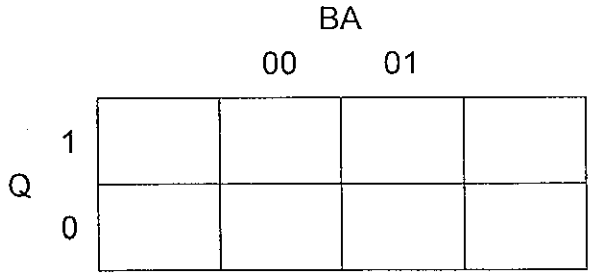
Step 2: K-maps and simplified Boolean equation

For input C



Simplified Boolean equation for input C

For input D



Simplified Boolean equation for input D

Step 3: Sketch the circuit

Question 4(a)(iii)

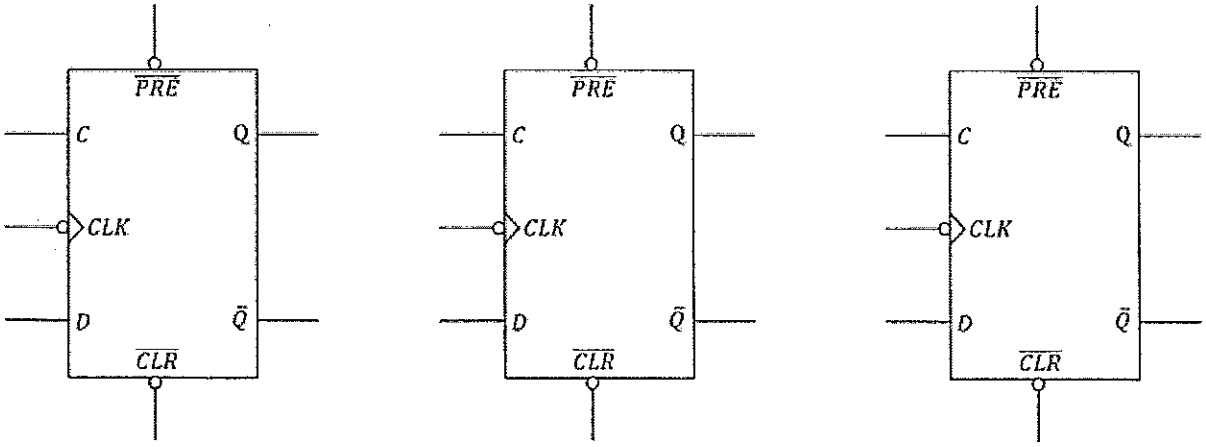


Figure C.1

Question 4(b)(i)

Question 4(b)(ii)

Question 4(b)(iii)

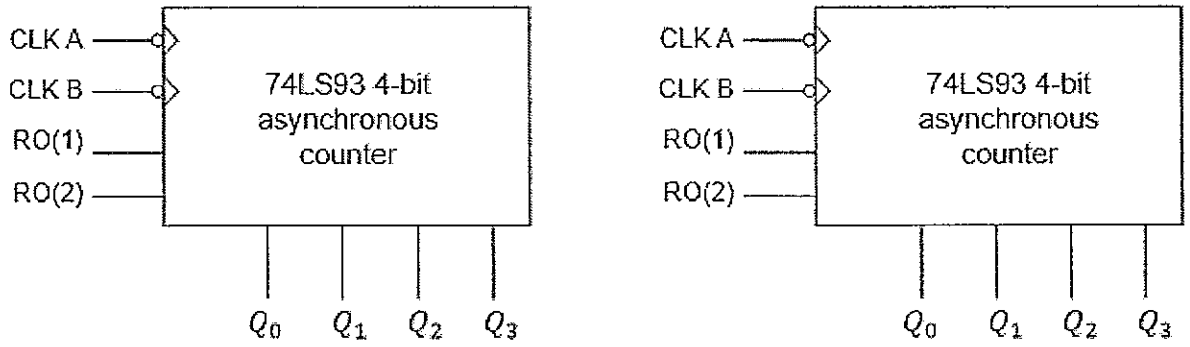


Figure C.2