IMPLEMENTING MOBILE COMMUNICATION SYSTEM USING FPGA

Oleh

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ABSTRACT

Global System for Mobile Communication (GSM) is a digital cellular communication network that has been used by most of the countries around the world. GSM mobile phone is used since 1991, and uses variety of error detection and error correction techniques in communication system to improve the services' quality. Thus, a research has been done on six parts of encoder and six parts of decoder in the GSM mobile phone communication system in order to produce chipsets using VHDL. The communication system is important for detecting errors, correcting and protecting speech data during transmission and receiving. Xilinx ISE 7.1i software in VHDL description is used as a tool in the research to enable each part of encoder and decoder to be modeled synthesized, simulated and implemented before downloaded on the FPGA device Spartan3 XC3S1500E-FG676. Furthermore, the FPGA device is capable to be programmed many times using different design. In this research, the simulation result for each part of encoder and decoder shows that 260 until 592 speech bits are gained in 20 ms based on the GSM standard. The download result is also similar to the simulation result for each part of encoder and decoder. After the download process, the chipsets of GSM mobile phone communication system are produced.

ABSTRAK

Sistem Global untuk Komunikasi Mudahalih (GSM) merupakan rangkaian komunikasi digital bersel yang digunakan oleh kebanyakan negara di seluruh dunia. Telefon mudahalih GSM mula digunakan pada tahun 1991 dan menggunakan pelbagai pengesan dan pembetul ralat dalam system perhubungan untuk meningkatkan kualiti perkhidmatan. Oleh itu, kajian telah dijalankan ke atas enam bahagian pengekod dan enam bahagian penyahkod dalam system perhubungan telefon mudahalih GSM bagi menghasilkan cipset dengan menggunakan VHDL. Sistem perhubungan ini penting bagi mengesan dan membetulkan ralat serta melindungi data suara semasa penghantaran dan penerimaan. Perisian Xilinx ISE 7.1i bentuk VHDL digunakan sebagai peralatan utama dalam kajian ini kerana ia membolehkan setiap bahagian pengekod dan penyahkod dimodel, disintesis, disimulasi dan seterusnya dilaksana sebelum dimuat turn ke atas peranti Field Programmable Gate Array (FPGA) iaitu Spartan3 XC3S1500E-FG676. Tambahan pula, peranti FPGA ini berkemampuan untuk deprogram berulang kali menggunakan rekabentuk yang berlainan. Dalam kajian ini, keputusan simulasi bagi setiap bahagian pengekod dan penyahkod menunjukkan 260 sehingga 592 bit data suara diperolehi dalam lingkungan masa 20 ms bersesuaian dengan piawaian GSM. Keputusan muat turun juga didapati sama dengan keputusan simulasi bagi setiap bahagian pengekod dan penyahkod. Setelah melalui proses muat turun, maka cipset-cipset system perhubungan telefon mudahalih GSM dapat dihasilkan.

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INTRODUCTION

1.1 History of GSM

During the early 1980s, analog cellular telephone systems were experiencing rapid growth in Europe, particularly in Scandinavia and the United Kingdom, but also in France and Germany. Each country developed its own system, which was incompatible with everyone else's in equipment and operation. This was an undesirable situation, because not only was the mobile equipment limited to operation within national boundaries, which in a unified Europe were increasingly unimportant, but there was also a very limited market for each type of equipment, so economies of scale and the subsequent savings could not be realized [9].

In 1982, the development of a pan-European standard for digital cellular mobile radio was started by the *Groupe Spécial Mobile* of CEPT (Conférence Européenne des Administrations des Postes et des Télécommunications) [1]. The proposed system had to meet certain criteria [9]:

- Good subjective speech quality
- Low terminal and service cost
- Support for international roaming
- Ability to support handheld terminals
- Support for range of new services and facilities
- Spectral efficiency
- ISDN compatibility

The task of GSM was to define a new standard for mobile communications in the 900 MHz range. It was decided to use digital technology. In the course of time, CEPT evolved into a new organization, the *European Telecommunications Standard Institute* (ETSI) in 1989. After the rapid worldwide proliferation of GSM networks, the name has been reinterpreted as *Global System for Mobile Communication*. That, however, did not change the task of GSM. The goal of GSM was to replace the purely national, already

overloaded, and thus expensive technologies of the member countries with an international standard [2].

After a series of incompatible analog networks had been introduced in parallel in Europe, e.g. *Total Access Communication System* (TACS) in the UK, *NMT* in Scandinavia, and the *C-Netz* in Germany, work on the definition of a Europe-wide standard for digital mobile radio was started in the late 1980s. The GSM was founded, which developed a set of technical recommendations and presented them to ETSI for approval. These proposals were produced by the *Special Mobile Group* (SMG) in working groups called *Sub Technical Committees* (STCs). In the meantime, the *Third Generation Partnership Project* (3GPP) has been founded in cooperation with other standardization committees worldwide. Finally, in July 2000, ETSI announced the closure of the SMG which has been responsible for setting GSM standards for the last 18 years. Their remaining and further work has been transferred to groups inside and outside ETSI; most of the ongoing work has been handed over to the 3GPP[1].

The Phase 1 of the GSM specifications was published in 1990. Commercial service was started in mid-1991, and by 1993 there were 36 GSM networks in 22 countries. In 1991, the first GSM systems were ready to be brought into so-called friendly-user operation. The meaning of the acronym GSM was changed that same year to stand for Global System for Mobile Communications [9]. The year 1991 also was the definition of the first derivative of GSM, the Digital Cellular System 1800 (DCS 1800), which more or less translates the GSM system into the 1800 MHz frequency range [2]. Although standardized in Europe, GSM is not only a European standard. Over 200 GSM networks (including DCS1800 and PCS1900) are operational in 110 countries around the world [9].

In the United States, DCS 1800 was adapted to the 1900 MHz band (Personal Communication System 1900, or PCS 1900). The next phase, GSM Phase 2, will provide even more end-user features than Phase 1 of GSM did. In 1991, only “insides” believed such a success would be possible because mobile communications could not be considered a mass market in most parts of Europe [2].

By 1992, many European countries had operational networks, and GSM started to attract interest worldwide [2]. By 1993 there were 36 GSM networks in 22 countries. In the beginning of 1994, there were 1.3 million subscribers worldwide, which had grown to more than 55 million by October 1997 [9]. Time has brought substantial technological progress to the GSM hardware. GSM has proved to be a major commercial success for the system manufactures as well as for network operators [2].

The developers of GSM chose an unproven (at the time) digital system, as opposed to the then-standard analog cellular systems like AMPS in the United States and TACS in the United Kingdom. They had faith that advancements in compression algorithms and digital signal processors would allow the fulfillment of the original criteria and the continual improvement of the system in terms of quality and cost. The over 8000 pages of GSM recommendations try to allow flexibility and competitive innovation among suppliers, but provide enough standardization to guarantee proper inter-working between the components of the system. This is done by providing functional and interface descriptions for each of the functional entities defined in the system [9].

The various satellite communications systems that now push into the market are another, possible decisive, factor in providing mobile communications on a global basis [2].

1.2 Services provided by GSM

From the beginning, the planners of GSM wanted ISDN compatibility in terms of the services offered and the control signaling used. However, radio transmission limitations, in terms of bandwidth and cost, do not allow the standard ISDN B-channel bit rate of 64 kbps to be practically achieved.

Using the ITU-T definitions, telecommunication services can be divided into bearer services, teleservices, and supplementary services. The most basic teleservice supported by GSM is telephony. As with all other communications, speech is digitally encoded and transmitted through the GSM network as a digital stream. There is also an emergency

service, where the nearest emergency-service provider is notified by dialing three digits (similar to 911) [9].

A variety of data services is offered. GSM users can send and receive data, at rates up to 9600 bps, to users on POTS (Plain Old Telephone Service), ISDN, Packet Switched Public Data Networks, and Circuit Switched Public Data Networks using a variety of access methods and protocols, such as X.25 or X.32. Since GSM is a digital network, a modem is not required between the user and GSM network, although an audio modem is required inside the GSM network to interwork with POTS.

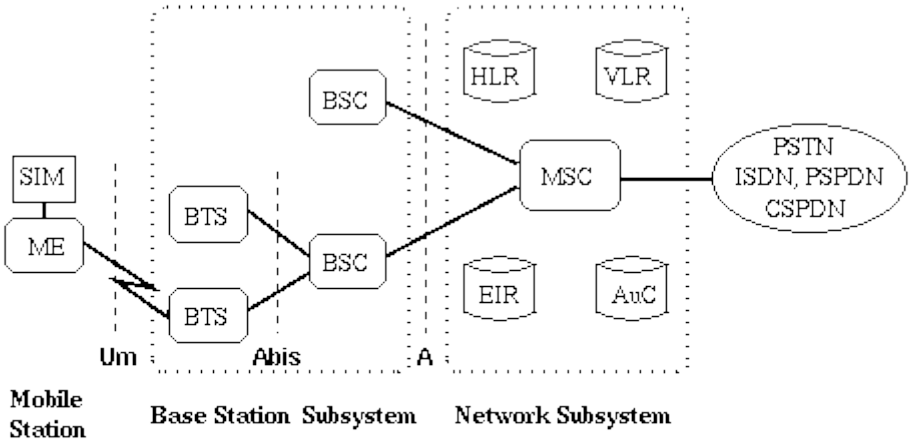
Other data services include Group 3 facsimile, as described in ITU-T recommendation T.30, which is supported by use of an appropriate fax adaptor. A unique feature of GSM, not found in older analog systems, is the Short Message Service (SMS). SMS is a bidirectional service for short alphanumeric (up to 160 bytes) messages. Messages are transported in a store-and-forward fashion. For point-to-point SMS, a message can be sent to another subscriber to the service, and an acknowledgement of receipt is provided to the sender. SMS can also be used in a cell-broadcast mode, for sending messages such as traffic updates or news updates. Messages can also be stored in the SIM card for later retrieval.

Supplementary services are provided on top of tele-services or bearer services. In the current (Phase I) specifications, they include several forms of call forward (such as call forwarding when the mobile subscriber is unreachable by the network), and call barring of outgoing or incoming calls, for example when roaming in another country. Many additional supplementary services will be provided in the Phase 2 specifications, such as caller identification, call waiting, multi-party conversations.

1.3 Architecture of the GSM network

A GSM network is composed of several functional entities, whose functions and interfaces are specified. *Figure 1.1* shows the layout of a generic GSM network. The GSM network can be divided into three broad parts. The Mobile Station is carried by the subscriber. The Base Station Subsystem controls the radio link with the Mobile Station.

The Network Subsystem, the main part of which is the Mobile services Switching Center (MSC), performs the switching of calls between the mobile users, and between mobile and fixed network users. The MSC also handles the mobility management operations. Not shown is the Operations and Maintenance Center, which oversees the proper operation and setup of the network. The Mobile Station and the Base Station Subsystem communicate across the Um interface, also known as the air interface or radio link. The Base Station Subsystem communicates with the Mobile services Switching Center across the A interface.



SIM Subscriber Identity Module
ME Mobile Equipment
BTS Base Transceiver Station
BSC Base Station Controller
HLR Home Location Register
VLR Visitor Location Register
MSC Mobile services Switching Center
EIR Equipment Identity Register
AuC Authentication Center

Figure 1.1: General architecture of a GSM network [9]

1.4 Mobile Station

The Mobile Stations (MS) are pieces of equipment which are used by mobile service subscribers for access to services [1]. It consists of the mobile equipment (the terminal) and a smart card called the Subscriber Identity Module (SIM). The SIM provides personal mobility, so that the user can have access to subscribed services irrespective of a specific terminal. By inserting the SIM card into another GSM terminal, the user is able to receive calls at that terminal, make calls from that terminal, and receive other subscribed services [9].

The mobile equipment is uniquely identified by the International Mobile Equipment Identity (IMEI) [9]. The SIM card contains the International Mobile Subscriber Identity (IMSI) used to identify the subscriber to the system, a secret key for authentication, and other information. The IMEI and the IMSI are independent, thereby allowing personal mobility. The SIM card may be protected against unauthorized use by a password or personal identity number.

1.5 Base Station Subsystem

The Base Station Subsystem is composed of two parts, the Base Transceiver Station (BTS) and the Base Station Controller (BSC). These communicate across the standardized Abis interface, allowing (as in the rest of the system) operation between components made by different suppliers [9].

A GSM cell is expanded around the radio area of a Base Transceiver Station; *transmitter + receiver = transceiver* [3]. Base Transceiver Station houses the radio transceivers that define a cell and handles the radio-link protocols with the Mobile Station. In a large urban area, there will potentially be a large number of BTSs deployed, thus the requirements for a BTS are ruggedness, reliability, portability, and minimum cost [9].

The Base Station Controller manages the radio resources for one or more BTSs. It handles radio-channel setup, frequency hopping, and handovers, as described below. The BSC is the connection between the mobile station and the Mobile service Switching Center (MSC).

1.6 Network Subsystem

The central component of the Network Subsystem is the Mobile services Switching Center (MSC). It acts like a normal switching node of the PSTN or ISDN, and additionally provides all the functionality needed to handle a mobile subscriber, such as registration, authentication, location updating, handovers, and call routing to a roaming subscriber. These services are provided in conjunction with several functional entities, which together form the Network Subsystem [9]. The MSC provides the connection to

the fixed networks (such as the PSTN or ISDN). Signaling between functional entities in the Network Subsystem uses Signaling System Number 7 (SS7), used for trunk signaling in ISDN and widely used in current public networks.

The Home Location Register (HLR) and Visitor Location Register (VLR), together with the MSC, provide the call-routing and roaming capabilities of GSM. The HLR is used to store information that is specific to each subscriber [3]. It contains all the administrative information of each subscriber registered in the corresponding GSM network, along with the current location of the mobile. The location of the mobile is typically in the form of the signaling address of the VLR associated with the mobile station. The actual routing procedure will be described later. There is logically one HLR per GSM network, although it may be implemented as a distributed database.

The Visitor Location Register (VLR) stores the data of all mobile stations which are currently staying in the administrative area of the associated MSC [3]. It contains selected administrative information from the HLR, necessary for call control and provision of the subscribed services, for each mobile currently located in the geographical area controlled by the VLR. Although each functional entity can be implemented as an independent unit, all manufacturers of switching equipment to date implement the VLR together with the MSC, so that the geographical area controlled by the MSC corresponds to that controlled by the VLR, thus simplifying the signaling required. Note that the MSC contains no information about particular mobile stations --- this information is stored in the location registers [9].

The other two registers are used for authentication and security purposes. The Equipment Identity Register (EIR) is a database that contains a list of all valid mobile equipment on the network, where each mobile station is identified by its International Mobile Equipment Identity (IMEI). EIR is used to store three different lists of IMEIs. The *white* list contains the series of IMEIs that have been allocated to MEs that may be used on the GSM network. The *black* list contains the IMEIs of all MEs that must be barred from using the GSM network. This will contain the IMEIs of stolen and malfunctioning MEs. Finally, the network operator may also use a *grey* list to hold the IMEIs of MEs that must

be tracked by the network for evaluation purposes [3]. The Authentication Center (AuC) is a protected database that stores a copy of the secret key stored in each subscriber's SIM card, which is used for authentication and encryption over the radio channel.

1.7 Radio link aspects

The International Telecommunication Union (ITU), which manages the international allocation of radio spectrum (among many other functions), allocated the bands 890-915 MHz for the uplink (mobile station to base station) and 935-960 MHz for the downlink (base station to mobile station) for mobile networks in Europe. Since this range was already being used in the early 1980s by the analog systems of the day, the CEPT had the foresight to reserve the top 10 MHz of each band for the GSM network that was still being developed. Eventually, GSM will be allocated the entire 2x25 MHz bandwidth.

1.8 Multiple access and channel structure

Since radio spectrum is a limited resource shared by all users, a method must be devised to divide up the bandwidth among as many users as possible. The method chosen by GSM is a combination of Time- and Frequency-Division Multiple Access (TDMA/FDMA). The FDMA part involves the division by frequency of the (maximum) 25 MHz bandwidth into 124 carrier frequencies spaced 200 kHz apart. One or more carrier frequencies are assigned to each base station. Each of these carrier frequencies is then divided in time, using a TDMA scheme. The fundamental unit of time in this TDMA scheme is called a *burst period* and it lasts 15/26 ms (or approx. 0.577 ms). Eight burst periods are grouped into a *TDMA frame* (120/26 ms, or approx. 4.615 ms), which forms the basic unit for the definition of logical channels. One physical channel is one burst period per TDMA frame.

Channels are defined by the number and position of their corresponding burst periods. All these definitions are cyclic, and the entire pattern repeats approximately every 3 hours. Channels can be divided into *dedicated channels*, which are allocated to a mobile station, and *common channels*, which are used by mobile stations in idle mode.

1.9 Traffic channels

A traffic channel (TCH) is used to carry speech and data traffic. Traffic channels are defined using a 26-frame multiframe, or group of 26 TDMA frames. However, only the *time slot 3* for every frame is used as user data. The length of a 26-frame multiframe is 120 ms, which is how the length of a burst period is defined (120 ms divided by 26 frames divided by 8 burst periods per frame). Out of the 26 frames, 24 are used for traffic, *frame 12* is used for the Slow Associated Control Channel (SACCH) and *frame 25* is currently unused (idle frame) as shown in *Figure 1.2*. During this idle frame time interval period, a mobile can receive other control channels and measure the received signal level from neighboring cells [4]. TCHs for the uplink and downlink are separated in time by 3 burst periods, so that the mobile station does not have to transmit and receive simultaneously, thus simplifying the electronics. User data is transmitted at the 3rd time slot in each frame.

In addition to these *full-rate* TCHs, there are also *half-rate* TCHs defined, although they

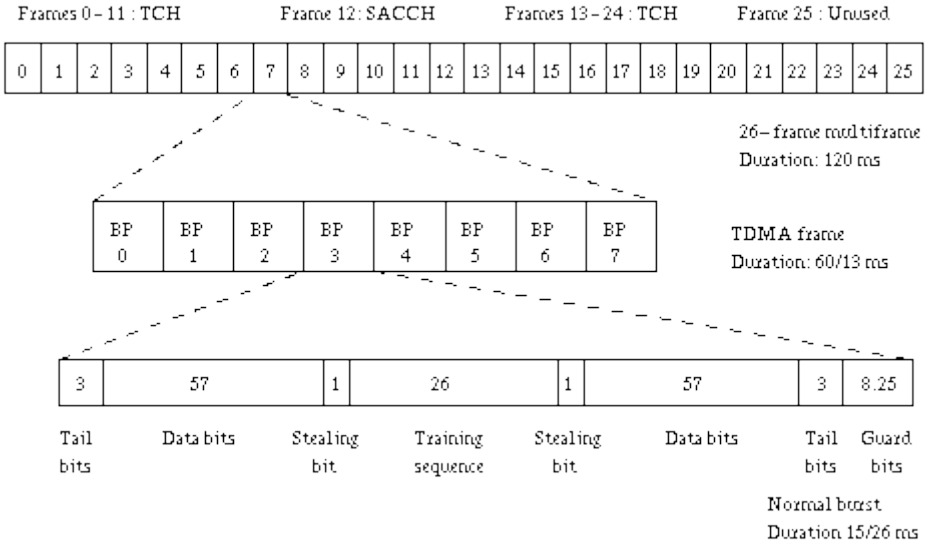


Figure 1.2: Organization of bursts, TDMA frames, and multiframes for speech and data

are not yet implemented. Half-rate TCHs will effectively double the capacity of a system once half-rate speech coders are specified (i.e., speech coding at around 7 kbps, instead of 13 kbps). Eighth-rate TCHs are also specified, and are used for signaling. In the recommendations, they are called Stand-alone Dedicated Control Channels (SDCCH) [9].

1.10 Control channels

Common channels can be accessed both by idle mode and dedicated mode mobiles. The common channels are used by idle mode mobiles to exchange the signaling information required to change to dedicated mode. Mobiles already in dedicated mode monitor the surrounding base stations for handover and other information. The common channels are defined within a 51-frame multiframe, so that dedicated mobiles using the 26-frame multiframe TCH structure can still monitor control channels. The common channels include:

Broadcast Control Channel (BCCH)

- Continually broadcasts, on the downlink, information including base station identity, frequency allocations, and frequency-hopping sequences.

Frequency Correction Channel (FCCH) and Synchronization Channel (SCH)

- Used to synchronize the mobile to the time slot structure of a cell by defining the boundaries of burst periods, and the time slot numbering. Every cell in a GSM network broadcasts exactly one FCCH and one SCH, which are by definition on time slot number 0 (within a TDMA frame).

Random Access Channel (RACH)

- Slotted Aloha channel used by the mobile to request access to the network.

Paging Channel (PCH)

- Used to alert the mobile station of an incoming call.

Access Grant Channel (AGCH)

- Used to allocate an SDCCH to a mobile for signaling (in order to obtain a dedicated channel), following a request on the RACH.

1.11 Basic elements of GSM transmission chain

Figure 1.3 gives a schematic overview of the basic elements of the GSM transmission chain. GSM transmission system consists of source coding, block coding, convolutional coding, interleaving, burst formatting, ciphering and differential coding at transmitter. At receiver, it consists of source decoding, block decoding, Viterbi decoding, deinterleaving, burst deformatting, deciphering and differential decoding. Besides, transmission medium is used to transmit signals from transmitter to receiver.

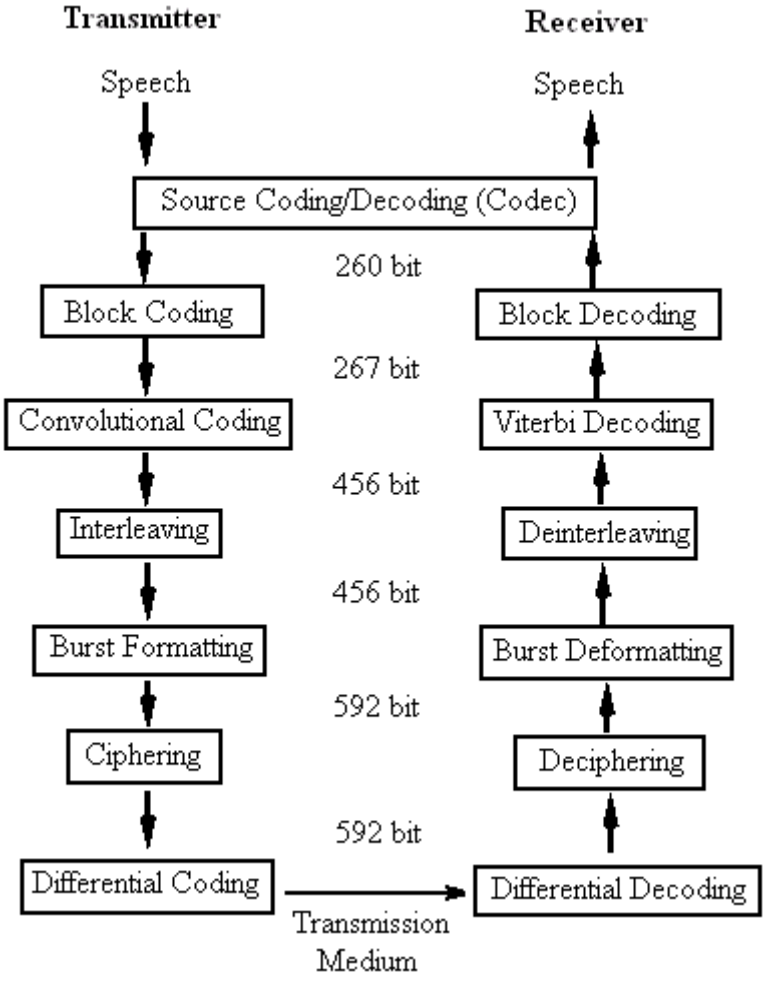


Figure 1.3: Basic elements of GSM transmission chain

1.11.1 Source coding/decoding

GSM is a digital system, so speech which is inherently analog, has to be digitized. The method employed by ISDN, and by current telephone systems for multiplexing voice lines over high speed trunks and optical fiber lines, is Pulse Coded Modulation (PCM). The output stream from PCM is 64 kbps, too high a rate to be feasible over a radio link. The 64 kbps signal, although simple to implement, contains much redundancy. The GSM group studied several speech coding algorithms on the basis of subjective speech quality and complexity (which is related to cost, processing delay, and power consumption once implemented) before arriving at the choice of a Regular Pulse Excited -- Linear Predictive Coder (RPE--LPC) with a Long Term Predictor loop. Basically, information from previous samples, which does not change very quickly, is used to predict the current sample. The coefficients of the linear combination of the previous samples, plus an encoded form of the residual, the difference between the predicted and actual sample, represent the signal [9].

The analog speech signal at the transmitter is sampled at a rate of 8000 samples/s, and the samples are quantized with a resolution of 13 bits. This corresponds to a bit rate of 104 kbit/s for the speech signal. At the input to the speech codec, a speech frame containing 160 samples of 13 bits arrives every 20 ms. The speech codec compresses this speech signal into a source-coded speech signal of 260-bit blocks at a bit rate of 13 kbit/s. Thus the GSM speech coder achieves a compression ratio of 1 to 8 [1]. This is the so-called Full-Rate speech coding. Recently, an Enhanced Full-Rate (EFR) speech coding algorithm has been implemented by some North American GSM1900 operators. This is said to provide improved speech quality using the existing 13 kbps bit rate.

Basically, the encoder divides the speech into short-term predictable parts, long-term predictable part and the remaining residual pulse. Then, it encodes that pulse and parameters for the two predictors. The decoder reconstructs the speech by passing the residual pulse first through the long-term prediction filter, and then through the short-term predictor. A simplified block diagram of the RPE-LTP codec is shown in *Figure 1.4.*

Speech data generated with a sampling rate of 8000 samples/s and 13 bit resolutions arrive in blocks of 160 samples at the input of the coder. The speech signal is then decomposed into three components: a set of parameters for the adjustment of the short-term analysis filter (LPC) also called *reflection coefficients*; an excitation signal for the RPE part with irrelevant portions removed and highly compressed; and finally a set of parameters for the control of the LTP long-term analysis filter. The LPC and LTP analyses supply 36 filter parameters for each sample block, and the TPE coding compresses the sample block to 188 bits of RPE parameters. This results in the generation of a frame of 260 bits every 20 ms, equivalent to a 13 kbit/s GSM speech signal rate.

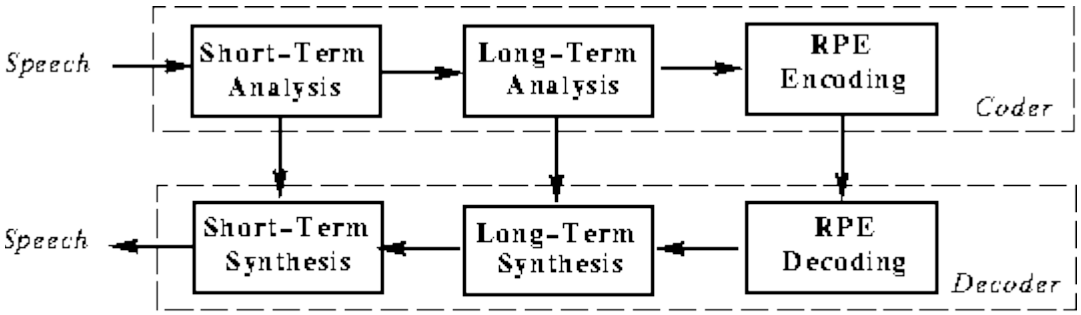


Figure 1.4: Block diagram of the RPE-LTP codec

The speech codec produces a 260 bit block for every 20 ms speech sample. From subjective testing, it was found that some bits of this block were more important for perceived speech quality than others. The bits are thus divided into three classes:

- ✓ Class 1A - 50 bits
  - most sensitive to bit errors
  - have a 3 bit Cyclic Redundancy Code added for error detection
  - if an error is detected, the frame is judged too damaged to be comprehensible and it is discarded
- ✓ Class 1B - 132 bits
  - moderately sensitive to bit errors

- 4 bit tail sequence are input into a 1/2 rate convolutional encoder of constraint length 4
- each input bit is encoded as two output bits, based on a combination of the previous 4 input bits

✓ Class 2 - 78 bits
- least sensitive to bit errors
- unprotected

1.11.2 Digital encoder and decoder

The block coding stage in GSM has the purpose of generating parity bits for a block of data, which allow the detection of errors in this block [1]. Three Cyclic Redundancy Code bits will be added into Class 1A for error detection [9]. At block decoding stage, source information from the output of demodulator will reconstruct and detect possible errors using the CRC parity bit [4]. If an error is detected, the frame is judged too damaged to be comprehensible and it is discarded. It is replaced by a slightly attenuated version of the previous correctly received frame.

Convolutional coding consists in transmitting the results of convolutions of the source sequence using different convolution formulas. The GSM convolutional code consists in adding 4 bits (set to ``0'') to the initial 185 bit sequence and finally is filled to 189 bits. It has the purpose of detecting and correcting the single bit error that might be introduced during transmission [4]. Convolutional decoding can be performed using a Viterbi algorithm. A Viterbi decoder logically explores in parallel every possible user data in sequence. It encodes and compares each one against the received sequence and picks up the closest match.

The errors in the transmitted bits tend to occur in bursts as the MS moves into and out of deep fades. Interleaving is meant to decorrelate the relative positions of the bits respectively in the code words and in the modulated radio bursts. The aim of the interleaving algorithm is to avoid the risk of loosing consecutive data bits. Deinterleaving

consists in performing the reverse operation. It puts the bits of the different bursts back in order to rebuild the original code words [4].

The burst formatting stage has the purpose of mapping each interleaving block directly onto a burst [1]. At burst deformatting side consists in performing the reverse operation.

A protection has been introduced in GSM by means of transmission ciphering through encryption algorithm, *A5*. The ciphering method does not depend on the type of data to be transmitted (speech, user data or signaling) but is only applied to normal bursts. Deciphering modifies the bits by reversing the ciphering code [4].

Differential modulation transforms the binary signal into an analogue signal at the right frequency. Thereby signal can be transmitted as radio waves. At differential demodulation stage, the received radio signal will be transformed into a binary signal [4].

1.12 Objective

The purpose of this project is to design a mobile communication system using FPGA. Besides, also need to produce the chipsets of GSM mobile phone communication system. This design is based on Xilinx software and implement with VHDL (*Very High Speed Integrated Circuit Hardware Description Language*).

Beside the technical objectives, this project is also meant to improve and develop soft skills such as planning, communication, organizing project and preparing formal documentation. The objectives are listed as the below:

1. To learn and develop technical knowledge such as VHDL. Learn to use proper and organized design methodologies and efficient resource searching during the course of the project.
2. Coming up with the best prototyping and testing methods available under constraining situations through software simulation and hardware testing.
3. Practice the good habit of naming components meaningfully based on their functions and including comments to clearly explain the circuit described.

4. Learning to handle projects in one person effort; distributing work load efficiently and effectively in a balanced ratio.
5. Dedicated to job assignments including follow-up meetings and emergency meetings with supervisor to sort arising problems and difficulties.
6. To be inquisitive and pro-active when solving problems including exhaustive referrals to relate websites and reference materials as well as consultations with my supervisor.
7. Inculcating good time management where all distributed work is done according to schedule.
8. Learn to prepare formal document such as proposal, progress report and thesis.
9. Improve communication skills through project presentation and meeting with supervisor.

Chapter 2

DESIGN METHODOLOGY

2.1 Field Programmable Gate Array (FPGA)

The *Field Programmable Gate Array* or FPGA as it is more widely called is a type of programmable device. Programmable devices are a class of general-purpose chips that can be configured for a wide variety of applications. The first programmable device, which achieved a widespread use, was the PROM (Programmable Read-Only Memory). PROMs, a one-time programmable device comes in two basic versions [10]:

1. The Mask-Programmable Chip programmed only by the manufacturer.
2. The Field-Programmable Chip programmed by the end-user.

The Field Programmable PROM developed into two types, the Erasable Programmable Read-Only Memory (EPROM) and the Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM has the advantage of being erasable and reprogrammable many times. Unlike most other microchips they do not come with a predefined function, but the user (the engineer who is designing some kind of electronic device) can design a function for the chip by designing a circuit for it on a computer. Then the design can be programmed into the FPGA. If the design does not what one wants, it's easy to change it on the computer and change the way the chip works [10].

There are four main categories of FPGAs currently commercially available: symmetrical array, row-based, hierarchical PLD, and sea-of-gates. In all of these FPGAs, the interconnections and how they are programmed vary. Currently there are four technologies in use which are static RAM cells, anti-fuse, EPROM transistors, and EEPROM transistors. Depending upon the application, one FPGA technology may have features desirable for that application.

Static RAM technology

- In the Static RAM FPGA programmable connections are made using pass transistors, transmission gates, or multiplexers that are controlled by SRAM cells.

- The advantage of this technology is that it allows fast in-circuit reconfiguration. The major disadvantage is the size of the chip required by the RAM technology.

Anti-Fuse technology

- An anti-fuse resides in a high-impedance state; and can be programmed into low impedance or “fused” state.
- A less expensive than the RAM technology, this device is a program once device.

EPROM /EEPROM technology

- This method is the same as used in the EEPROM memories. One advantage of this technology is that it can be reprogrammed without external storage of configuration; though the EPROM transistors cannot be reprogrammed in-circuit.

The FPGAs provide the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array. The FPGAs are customized by loading configuration data into the internal memory cells.

2.2 Architecture of FPGA

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-four different signal standards, including seven high-performance differential standards. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.

- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in *Figure 2.1*. A ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18-Kbit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns [7].
The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing [7].

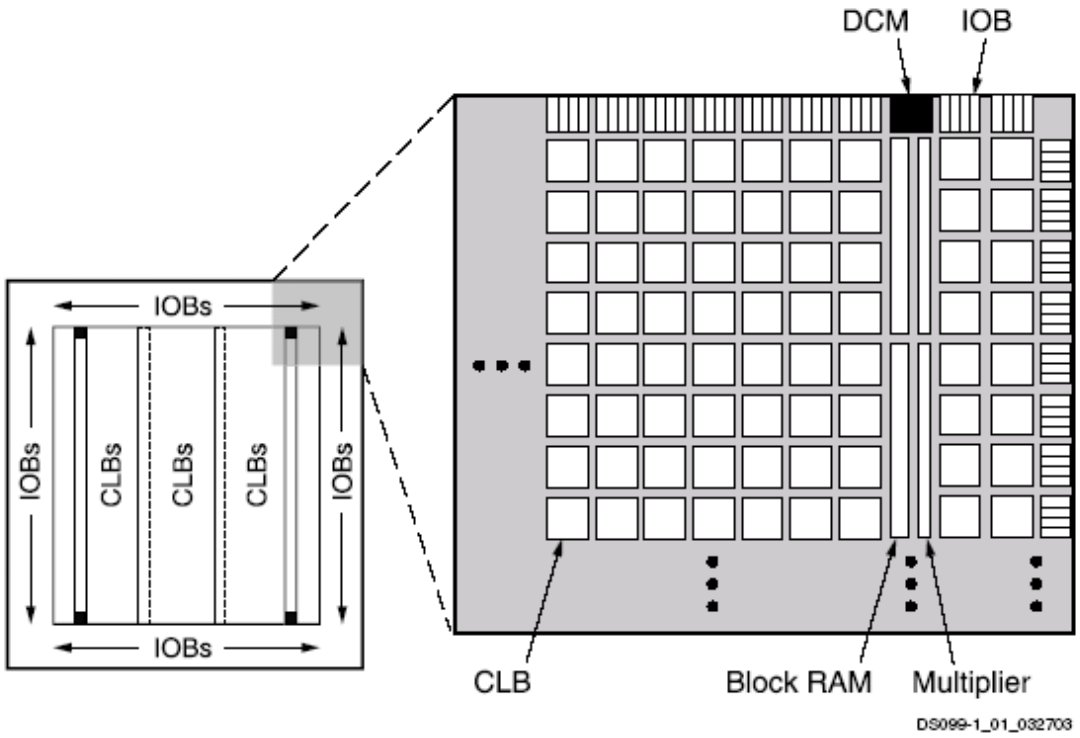


Figure 2.1: Spartan-3 family architecture [7]

2.3 VHDL

VHDL is a *Very High Speed Integrated Circuit Hardware Description Language* because it is used to describe hardware. The word ‘hardware’, however, is used in a wide variety of contexts which range from complete systems like personal computers on one side to the small logical gates on their internal integrated circuits on the other side.

This is why different descriptions exist for the hardware functionality. Complex systems are often described by the behavior that is observable from the outside. Abstract behavioral models are used in this case that hides all the implementation details. In this example the print protocol will be executed whenever a PPRINTREQUEST occurs. This can be a pressed key or a software command, etc. The description of a basic logic gate, on the other hand, may consist of only one Boolean equation. This is a very short and precise description.

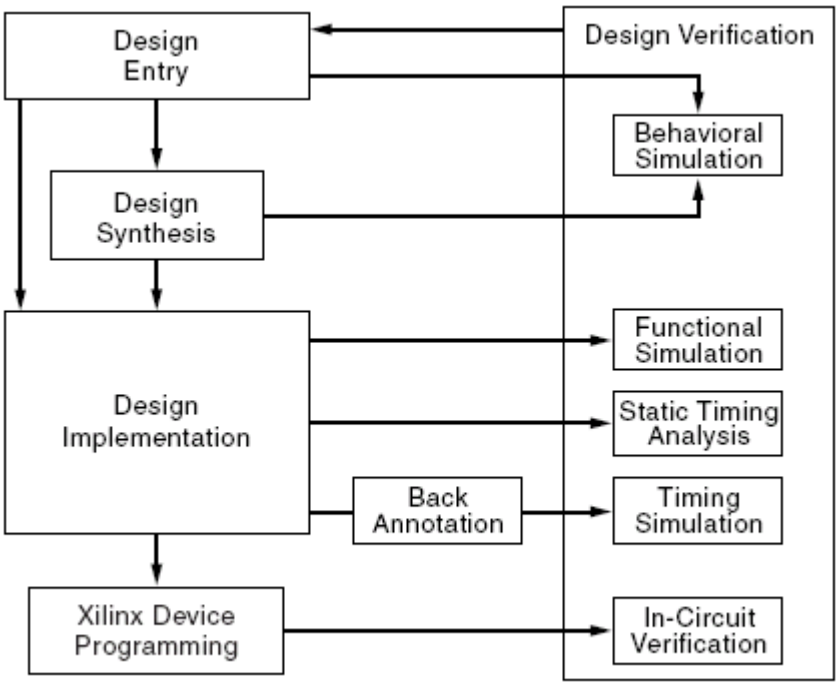


Figure 2.2: FPGA design flow

The language VHDL covers the complete range of applications and can be used to model (digital) hardware in a general way.

The basic component describe in VHDL is a module, which is specified by inputs, outputs, functions and delays. The inputs and outputs are specified by a design entity, composed by an entity name and an entity declaration, which each input and each output is represented by a port declaration.

The function of the module is described by architecture bodies. A given modules may have several architecture bodies, which correspond to different levels of details in the description or to alternatives module. There are three types of architecture bodies, behavioral and structural.

In the behavior architecture, the functionality of the entire module is describe as a whole using high level expressions and language constructs. The behavior of module is described as a process whose body consists of a set of statements.

For structural architecture, the module is described as the interconnection of simpler modules (hierarchical description). The simpler modules are described independently. The functionality of the higher level modules is determined from the behavior of the simpler modules and their interconnections.

2.4 SP305 Spartan-3 FPGA board

The FPGA board is a fully functional stand alone system. As shown in the *Figure 2.3*, the input/output pins of the device can be used directly. All the features are mentioned as below [8]:

- Spartan-3 FPGA (XC3S1500-FG676-10)
- 64MB DDR SDRAM, 32-bit interface running up to 266 MHz data rate
- One differential clock input pair and differential clock output pair with SMA connectors
- One 100 MHz clock oscillator (socketed) plus one extra open 3.3V clock oscillator socket
- General purpose DIP switches, LEDs, and push buttons
- Rotary Encoder with a push button shaft

- Expansion header with 32 single-ended I/O, 16 LVDS capable differential pairs, 14 spare I/O's, power, JTAG chain expansion capability, and IIC bus expansion
- Stereo AC97 audio codec with line-in, line-out, 50-mW headphone, and microphone-in (mono) jacks
- Two RS-232 serial port (one stand alone and one attached to the USB Chipset)
- 16-character x 2-line LCD display
- 4Kb IIC EEPROM

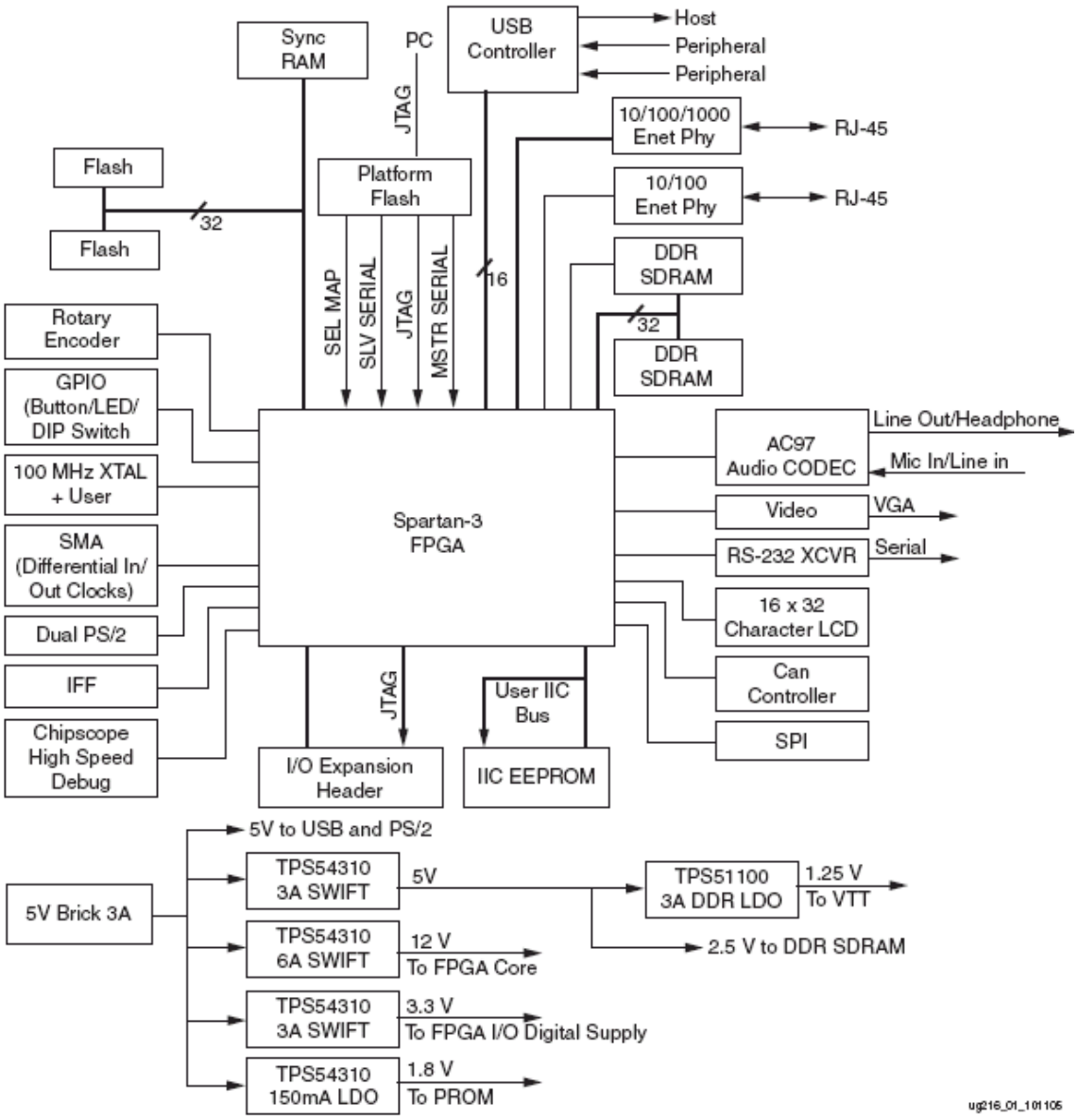


Figure 2.3: Spartan-3 SP-305 Development Platform Block Diagram [8]

- VGA output with 50 MHz / 24-bit video DAC
- PS/2 mouse and keyboard connectors
- ZBT synchronous SRAM (9Mb) on 32-bit data bus with four parity bits
- Intel StrataFlash (or compatible) linear flash memory chips (8MB)
- 10/100 Ethernet Mac-PHY transceiver
- 10/100 Ethernet PHY transceiver
- USB interface chip (Cypress CY7C67300) with host and peripheral ports
- CAN and SPI interface ports
- IFF one wire encryption device
- Xilinx XCF32P Platform Flash configuration storage device
- JTAG configuration port for use with Parallel Cable III or Parallel Cable IV cable
- Onboard power supplies for all necessary voltages
- 5V @ 3A AC adapter
- Power indicator LED

2.5 HP logic analyzer 1660E

Oscilloscope (OSK) and a logic analyzer are different in several aspects. Most of the people are more familiar to oscilloscope than a logic analyzer. Generally, an oscilloscope is the instrument to use when high vertical or voltage resolution is needed. It can be used to measure the time interval between two events with very high accuracy. Logic analyzer grew out of oscilloscope. It presents data in the same general way than the scope does. The horizontal axis is the time and the vertical axis is voltage amplitude. But the logic analyzer does not provide as much voltage resolution or time interval accuracy as the scope. However, it can be used to capture and display eight or more signal at once, something that the scope cannot do.

Chapter 3

GSM ENCODER DESIGN SPECIFICATION

3.1 Encoder entity design

There are 3 input pins (CLK1, CLK2, DATAIN) and 1 output pin (DATAOUT) in every encoder entity as shown in *Figure 3.1*. CLK1 and CLK2 period are different for different part of encoder which depends to total bits pass through the entity within 20 ms. Therefore, CLK1 represents the input data bit period and CLK2 represents the output data bit period. Besides, DATAIN displays the input data bits whether are '0' or '1' bit Finally, DATAOUT displays the output data bits from encoder.

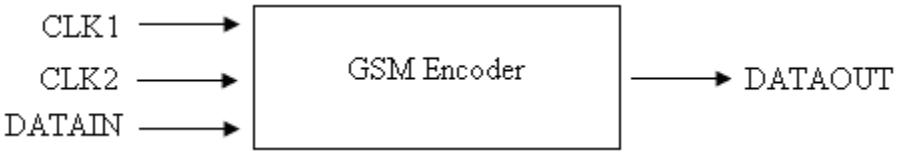


Figure 3.1: Schematic of GSM encoder

3.2 Block coding

3.2.1 Block coding operation

At block coding stage, parity bits will be generated for error detection. Probably the most reliable redundancy checking technique for error detection is a convolutional coding scheme call cyclic redundancy checking (CRC). With CRC, approximately 99.999% of all transmission errors are detected. With CRC, the entire data stream is treated as a long continuous binary number and CRC considered a *systematic code*. Cyclic block codes are often written as (*n, k*) cyclic code where *n* equal to bit length of transmission and *k* is bit length of message. Therefore, the length of CRC bits is

$$CRC = n - k \tag{3.1}$$
$$= 53 - 50$$
$$= 3$$