DESIGN OF RECEIVER LOWPASS FILTER FOR UWB APPLICATION USING 0.18μM CMOS TECHNOLOGY

Oleh

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ABSTRAK

Rekabentuk dan analisis penuras laluan rendah frekuensi rendah untuk aplikasi UWB di bahagian depan penerima dipersembahkan dalam laporan ini. Objektif projek ini adalah untuk merekabentuk satu penuras laluan rendah yang beroperasi pada voltan 1.8V dan mempunyai lebar jalur 264MHz dengan menggunakan teknologi 0.18µm SMCMOS daripada prosess Silterra. Transkonduktor-capasitor adalah antara jenis penuras yang telah dipilih untuk merekabentuk and melakukan analisis ke atas penuras laluan rendah kerana kebolehannya untuk beroperasi pada frekuensi yang tinggi. Tertib pertama hingga tertib keempat Gm-C penuras laluan rendah telah direkabentuk dan prestasi mereka telah dibandingkan untuk membolehkan pemilihan tertib penuras yang paling sesuai untuk dijadikan penuras untuk applikasi UWB. Tertib pertama Gm-C penuras laluan rendah mempunyai jalur lebar 264.00MHz dan gandaan DC sebanyak -0.25dB. Titik 1dB tertekan ialah 3.68dBm dan titik persilangan tertib ketiga ialah 11.69dBm. Jumlah kuasa yang digunakan oleh penuras tertib pertama adalah 5.00mW. Penuras tertib kedua pula mempunyai lebar jalur sebanyak 264.00MHz, gandaan DC sebanyak -0.13dB, titik 1dB tertekan pada -0.64dBm, titik persilangan tertib ketiga pada 6.05dBm dan jumlah kuasa yang digunakan adalah 10.01mW. Penuras tertib ketiga pula mempunyai lebar jalur sebanyak 264.00MHz, gandaan DC sebanyak -0.38dB, titik 1dB tertekan pada -0.077dBm, titik persilangan tertib ketiga pada 6.61dBm dan jumlah kuasa yang digunakan adalah 15.02mW. Penuras tertib keempat pula mempunyai lebar jalur sebanyak 264.00MHz, gandaan DC sebanyak -0.26dB, titik 1dB tertekan pada -1.92dBm, titik persilangan tertib ketiga pada 4.50Bm dan jumlah kuasa yang digunakan adalah 20.02mW. Tertib ketiga Butterworth Gm-C penuras laluan rendah telah dipilih sebagai penuras untuk applikasi UWB disebabkan perubahan yang tajam semasa peralihan daripada jalur laluan ke jalur henti jika dibandingkan dengan tertib pertama dan kedua penuras, dan penuras tertib ketiga ini juga mempunyai kelinearan yang lebih baik daripada penuras tertib keempat. Penuras tertib ketiga mempunyai 72 transistor dan 3 MIM kapasitor serta mempunyai saiz layout sebanyak $294\mu m \times 286\mu m$. Penuras yang direkabentuk ini akan dihantarkan ke Silterra untuk difabrikkan menjadi satu cip.

ABSTRACT

The design and analysis of a baseband lowpass filter for UWB application in front end receiver is presented in this report. The objective of this project is to design a lowpass filter which operates with voltage 1.80V and has a bandwidth 264.00MHz by using Silterra 0.18um SMCMOS technology. Transconductor-capacitor filter is the filter architecture being chosen to design and analysis the lowpass filter due to its capability to operate in high frequency, but low power and low cost as compared to passive filter. First to fourth order Gm-C Butterworth lowpass filter is designed and their performance is compared to allow effective filter order selection. First order Gm-C Butterworth lowpass filter has bandwidth 264.00MHz and DC gain of -0.25dB. The 1dB compression point of first order filter is 3.68dBm and third order intercepts point (IP3) at 11.69dBm. The power consumption of first order filter is 5.00mW. Second order filter has bandwidth of 264.00Mhz, DC gain of -0.13dB, 1dB compression point at -0.64dBm, IP3 at 6.05dBm and power consumption of 10.01mW. The third order Gm-C filter has bandwidth 264.00MHz, DC gain of -0.38dB, 1dB compression point at -0.077dBm IP3 at 6.61dBm, power consumption of 15.02mW. The forth order Gm-C filter has bandwidth 264.00MHz, DC gain of -0.26dB, 1dB compression point at -1.92dBm IP3 at 4.50dBm, power consumption of 20.02mW. Third order Gm-C Butterworth lowpass filter has been chosen as baseband filter due to its sharper rolloff in transition from passband to stopband than first and second order filter, and has a better linearity than fourth order filter. The third order filter consists of 72 transistors and 3 MIM capacitor. The size of layout of third order Gm-C filter is $294\mu m \times 286\mu m$. The designed filter will be sent to Silterra for fabrication into chip and furthermore chip characterization and measurement will be carried out to make sure the measurement of real filter chip can match well as closed as to the simulated result of filter design.

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CHAPTER 1

INTRODUCTION

1.1. Background of Project

Since the past few years, there has been a rapidly growing interest in UWB systems. Ultra-Wideband (UWB) is an alternative wireless communication technology that offers the promise of high bandwidth wireless communication without the constraints of spectrum allocation.

However, this wide bandwidth complicates the circuit implementation of key RF blocks such as the power amplifier (PA), low noise amplifier (LNA) mixers and filter in an UWB radio. For transceiver realizations, CMOS technology is more desirable for a single-chip, low-cost solutions if compared to the expensive technologies like SiGe (Silicon-Germanium) or GaAs (Gallium-Arsenide). However, some inherent limitations of CMOS (low breakdown voltage, poor passive components, lack of accurate models etc.) has resulted the design of CMOS RFIC's (Radio Frequency Integrated Circuits) at such high frequencies and such a wide bandwidth to be a challenging task. Nevertheless, with current technology scaling and advances in CAD based models like SMCMOS 0.18µm, CMOS is still the preferred choice for RFIC's. [Jose, 2004]

RF lowpass filters are one of the key functional blocks in wireless communication systems and are used to attenuate interference signal in undesired frequency bands while allowing signals in desired frequency bands to pass through with gain or loss. The integration of filter on-chip offers several advantages. First, the transceiver's overall size will be reduced because the filter can be integrated on the same silicon like other RF block. Second, the cost of RF transceiver will be reduced because fewer external components will be required. Finally, the power dissipation will also be reduced as RF signal does not need to travel off-chip filter through pins.

1.2. Objective and Scope of Project

The objective of this project is to design a low pass filter (LPF) with a bandwidth of 264MHz utilizing Silterra 0.18µm submicron (SM) complementary metal oxide semiconductor (CMOS) technology. The application of the low pass filter is as RF filter for a front end direct conversion architecture receiver for Ultra-wideband communication.

The scope of this project is to conduct analysis on a various order filters, which is from first order to fourth order filter. The analysis includes filter gain response, phase response, transient response, linearity analysis and power consumption. After simulation and optimization, the performance of filters will be compared and the order filter which gives the best overall performance will be chosen to be implemented as baseband filter for UWB application. The major concerns on the low pass filter design are its filter gain, cutoff frequency and linearity. The layout of the circuit will be drawn. The designed filter will be sent to Silterra for fabrication into chip and therefore the testing and measurement will be done on the chip.

1.3. Structure of Report

This report is divided into 5 chapters. Chapter 1 is the introduction to the project. The scope and objective of project are also discussed in this chapter.

Chapter 2 provides a brief overview and theory on aspects relate to the projects. Overview of UWB technology, MB-OFDM architecture, receiver architecture and filter are studied. The reasons the transconductor-capacitor filter is chosen as baseband filter in this project is also discussed in this chapter.

Chapter 3 presents all the step in designing the Gm-C Butterworth Lowpass filter. This chapter explains the design of transconductor cell and circuit analysis on this transconductor cell. 1^{st}, 2^{nd}, 3^{rd}, and 4^{th} order Gm-C filter are designed in this chapter.

Chapter 4 lists out all the simulation result of 1^{st}, 2^{nd}, 3^{rd}, and 4^{th} order Gm-C filter. Discussions are given in this chapter to help in explaining the simulation result.

Chapter 5 presents the conclusion based on the perfomance of 1^{st}, 2^{nd}, 3^{rd}, and 4^{th} order Gm-C lowpass filter carried out.

CHAPTER 2

OVERVIEW AND THEORY

2.1 Overview of Ultra-Wideband (UWB) Technology

Since the past few years, there has been a rapidly growing interest in UWB systems. Ultra-Wideband (UWB) is an alternative wireless communication technology that offers the promise of high bandwidth wireless communication without the constraints of spectrum allocation. Unlike conventional radio frequency communications, UWB relies on a series of narrow, precisely timed pulses to transmit digital data. UWB systems make use of ultra-short duration (<10ns) pulses which yield ultra-wide bandwidth signals characterized by extremely low power spectral densities. UWB systems are particularly promising for short-range wireless communication, low cost solution, low probability of intercept, immunity to multi-path fading, ability of penetrating walls, and multi-user capabilities. [Zhang, 2004]

On 14 February 2002, the Federal Communications Commission (FCC) opened up the spectrum from 3.1 GHz to 10.6 GHz for unlicensed use of the UWB technology. The main concern regarding UWB is that it occupies a portion of spectrum where other narrowband systems already operate, so a regulation is necessary in order to avoid co-existence problems. Therefore FCC fixed strict limitations in the maximum emission for unlicensed UWB signals thus guaranteeing protection to the already existing and planned radio services (see Figure 2.1). The UWB transmission, following the FCC rules, is therefore undetectable having a power spectral density below the thermal noise level. The spectral mask for both indoor and outdoor emissions is shown in Figure 2.2.

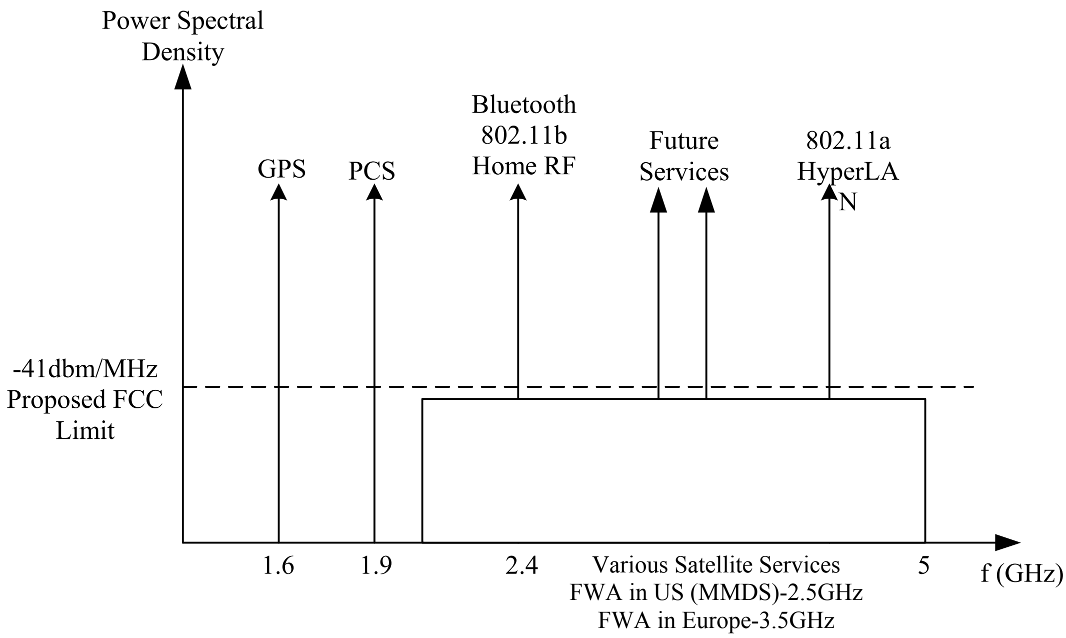

Figure 2.1: Co-existence of narrowband and UWB system and FCC power spectral density limit for UWB

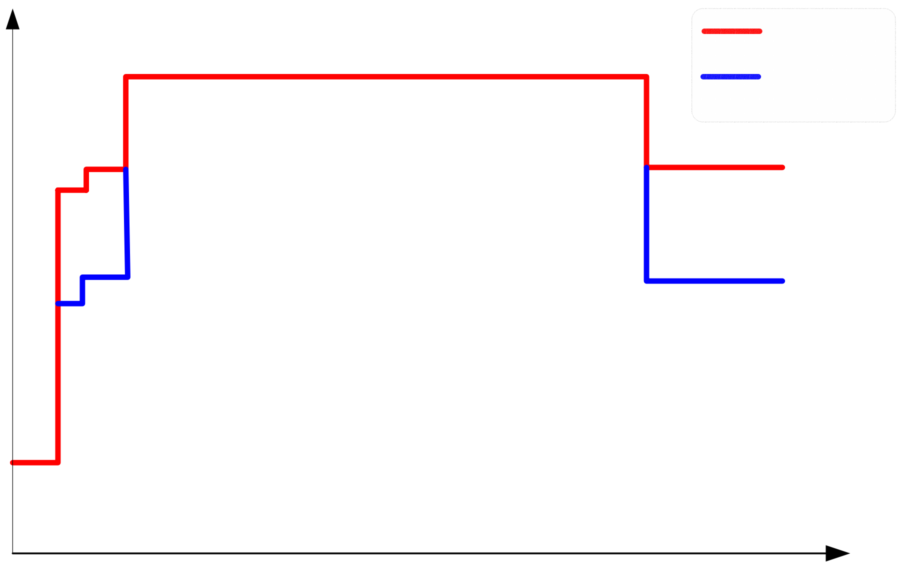

Figure 2.2: Spectral mask for UWB indoor and outdoor application.

The FCC defines a UWB transmitter as "an intentional radiator that, at any point in time, has a fractional bandwidth equal to or greater than 0.20 or has a UWB bandwidth equal to or greater than 500 MHz, regardless of the fractional bandwidth".

Fractional bandwidth is the bandwidth expressed as a fraction of the center frequency and is defined as

$$\eta = \frac{2(f_H - f_L)}{f_H + f_L} \tag{2.1}$$

where f_H and f_L are the upper and lower frequencies of the -10 dB emission point.

Shannon's channel capacity theorem helps in explaining why the wide spectrum allocated to UWB can directly translate into a wireless channel with high spatial capacities. According to Shannon's channel capacity theorem:

$$C = B \log_2(1 + SNR) \tag{2.2}$$

where C is the channel capacity in bits/second, B is the bandwidth in Hertz and SNR is the Signal-to-Noise Ratio.

Expression (2.2) shows a linear relation of the channel capacity with bandwidth and logarithmic relation with the SNR. Unlike narrowband systems whose data rate is limited by the bandwidth and SNR, UWB systems can achieve high data rates while operating below the noise floor. Nevertheless UWB is power limited which indirectly limits the overall channel capacity.

2.2. Overview of MB-OFDM

MB-OFDM (Multi-Band Orthogonal Frequency Division Multiplexing) is the most famous architecture that being used to implement UWB transceiver. The MB-OFDM (Multi-Band Orthogonal Frequency Division Multiplexing) has been proposed by a group of major companies like Intel, Texas Instrument etc. In this approach, the spectrum is divided into 14 bands (each with bandwidth equal to 528 MHz), and devices are allowed to statically or dynamically select which bands to use for transmission. Furthermore, OFDM is used in each of these bands. The entire spectrum is divided into 4 distinct groups. Only Group-A spectrum is intended for first generation devices because of current technology limitations. Other groups have been reserved for future use. Figure 2.3 shows the frequency allocation of sub-bands for a multi-band OFDM system.

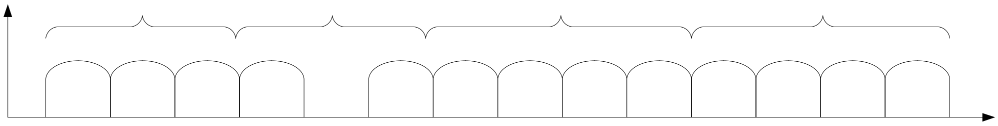

Figure 2.3: Frequency allocation of sub-bands for a multi-band OFDM system [Jose, 2004].

Orthogonal frequency division multiplexing (OFDM) techniques use multi-carrier, multi-band systems to transmit the information on each of the sub-bands. The main advantages are that it is easier to collect multi-path energy using a single RF chain, relaxed switching times, insensitivity to group delay variations, and ability to deal with narrowband interference at the receiver without having to sacrifice sub-bands or data rate. The only drawback of this type of system is that the transmitter is slightly more complex because it requires an IFFT and the peak-to-average ratio may be slightly higher than that of the pulse-based multi-band approaches. Figure 2.4 shows the OFDM multi-carrier modulation technique.

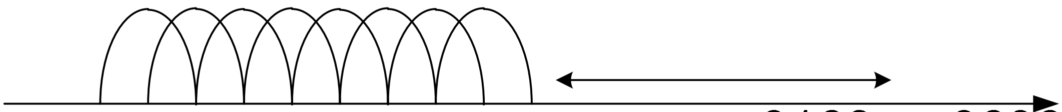

Figure 2.4: OFDM multi-carrier modulation technique [Matiae, 1998].

2.3. Receiver Architecture

The functions of a wireless receiver are to detect a low-level modulated RF signal in the presence of noise and unwanted signals, to accurately amplify and process this signal to extract the modulating digital or analog information that is presented in the received RF energy. There are two common receiver architectures available for communication system, such as super-heterodyne and direct conversion (homodyne)

2.3.1 Super-heterodyne Receiver

Super-heterodyne receiver uses a local oscillator to mix a radio frequency signal to a more convenient intermediate frequency. The mixer generates upper and lower sidebands, either which may be filtered out if desired. The block diagram for super-heterodyne receiver is shown in Figure 2.5. The main drawback in super-heterodyne architecture is the image problem. The image power can be much higher than the desired signal, requiring proper ”image rejection” and the important drawback is the image reject filter is usually realized as a passive, external component [Razavi, 1998].

The other disadvantages of the super-heterodyne receiver architecture are its cost and large power consumption. A significant fraction of the cost goes into the IF and RF filters. The large power consumption is due to losses in these external filters (IF bandpass ceramic or SAW), which have to be compensated by amplifying sections. Hence these filters limit the level of miniaturization, the minimum cost level, and the minimal power dissipation that can be achieved [Vaucher & Kasperkovitz, 1998].

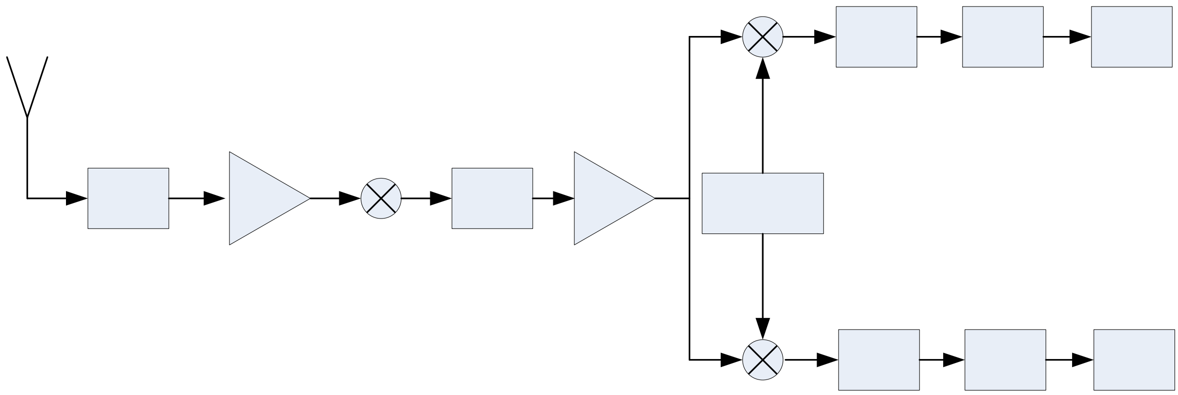

Figure 2.5: Super heterodyne receiver block diagram [2].

2.3.2 Homodyne Receiver

Direct-Conversion (zero IF), as shown in Figure 2.6, is an attractive architecture in radio design because it eliminates the need for expensive filters at radio frequencies (RF) for image rejection and at intermediate frequencies (IF) for channel selection and offers a high degree of integration.

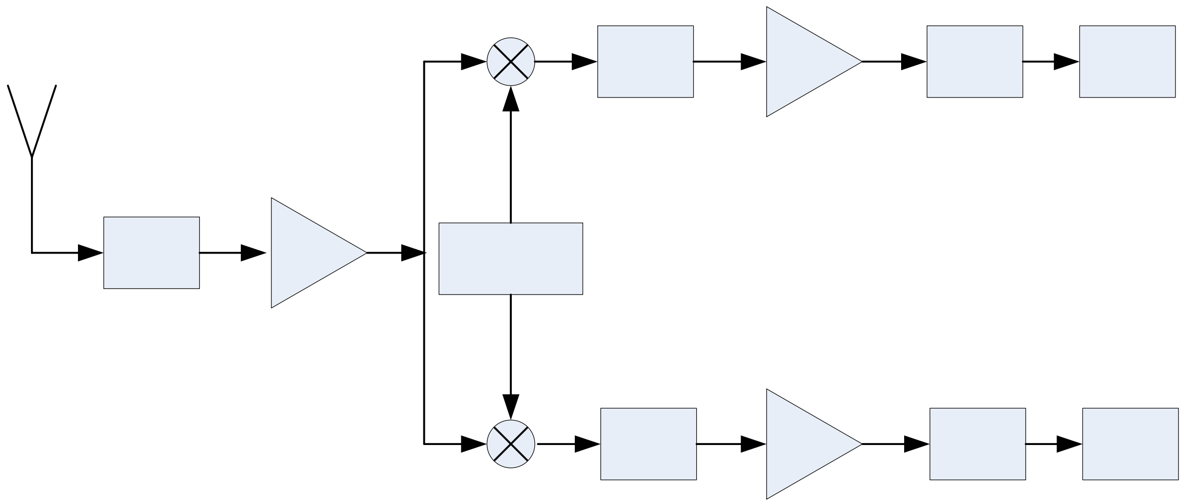

Figure 2.6: Homodyne receiver block diagram [2].

As referred from Figure 2.6, the antenna that has noisy RF signal passes through a band pass filter to attenuate out of band signals fulfilling the required dynamic range around 3.96GHz at the input of LNA. LNA (low noise amplifier) amplifies the RF signal with enough high gain to overcome the noise of the following stage such as mixer and filter. After that, the upper side band and lower side band of amplified signal are down-converted to baseband (zero frequency) signal by two identical mixer utilizing a 3.96GHz I/Q local oscillator. In-phase (I) local oscillator has a 90° different phase as compared to quadrature (Q) local oscillator. The baseband signal now passes through low pass filter with bandwidth 234MHz to suppress all out of band noise while allowing the useful information to be further processed by AGC, and subsequently be digitized by an analog to digital converter (ADC).

Direct conversion receivers provide a simpler means of down conversion. RF signals are translated down to baseband by a single conversion stage and a single LO that is at the same as the RF frequency. The direct conversion has the potential for reduced power consumption, multi-band operation, reduced dependence on off-chip filters, higher levels of integration, and reduced system complexity.

BPF

Direct-conversion avoids the image suppression problem because there are no image at zero-IF. A simple low-pass filter is used for channel selection. Therefore, the out-of-band energy is reduced, which could cause overload or distortion-generated products in the receiver. The price is that zero-IF receivers require matched LO I/Q quadrature signals covering the total input frequency range. The principal difficulties of direct-conversion are DC offsets, flicker noise (1/f) and sensitivity to even order distortion together with I/Q imbalances.

2.4. Overview of Filter

In circuit theory, a filter is an electrical network that alters the amplitude or phase characteristics of a signal in frequency domain. Ideally, a filter neither adds new frequencies to the input signal, nor changes the component frequencies of that signal, but it changes the relative amplitudes or their phase of the various frequency components [Lacanette, 1991]. Filters are often used in electronic systems to pass signals in desired frequency ranges and reject signals in other frequency ranges.

There are four types of filters. A low pass filter is frequency selective filter which passes all frequency components below a cutoff frequency ω_c and attenuates all other frequency components. A high pass filter is frequency selective filter which passes all frequency components above a cutoff frequency ω_c and attenuates all other frequency components. A band pass filter is frequency selective filter which passes all frequency components within a frequency range $\omega_L \leq \omega \leq \omega_U$ and attenuates all other out of band frequency components. A band stop filter is frequency selective filter which stoppes all frequency components within a frequency range $\omega_L \leq \omega \leq \omega_U$ and passes all other out of band frequency components.

2.5. Filter Response

There are a few different types of filter response such as Butterworth filter, Chebyshev filter, Bessel filter, and Elliptic filter.

2.5.1. Butterworth Filter

The Butterworth filter is the best-known filter approximation. The frequency response of Butterworth filter is maximally-flat without ripple in the passband. The roll off is smooth and monotonic, with a roll off rate of 20 dB/decade (6 dB/octave) for every pole [Lacanette, 1991]. The Butterworth is the only filter that maintains this same shape for higher orders (but with a steeper decline in the stopband) whereas the other varieties of filters (Bessel, Chebyshev, Elliptic) have different shapes at higher orders.

2.5.2. Chebyshev Filter

Chebyshev filters are filters which have a steeper roll-off and equal passband ripple than Butterworth filters. Chebyshev filters have the property that they minimize the error between the idealized filter characteristic and the actual over the range of the filter, but with ripples in the passband and hence poorer transient response. The greater the ripple amplitude allowed, the steeper the transition roll off [Soorapanth, 2002].

2.5.3. Bessel Filter

The Bessel filter is a filter that exhibits approximately linear phase shifting with frequency; hence this filter also has the maximally flat group delay. The higher the filter order, the Bessel's phase response will becomes more linear. The amplitude response of the Bessel filter is monotonic and smooth, but the Bessel filter's cutoff characteristic is quite gradual compared to either the Butterworth or Chebyshev.

2.5.4. Elliptic Filter

An elliptic filter (also known as a Causer filter) is a filter with equiripple behavior in both the passband and the stopband. The cutoff slope of an elliptic filter is the steepest when compared to Butterworth, Chebyshev, or Bessel filter. The disadvantage of Elliptic filter is it has ripples in both passband and stopband and it will cause a big phase distortion.

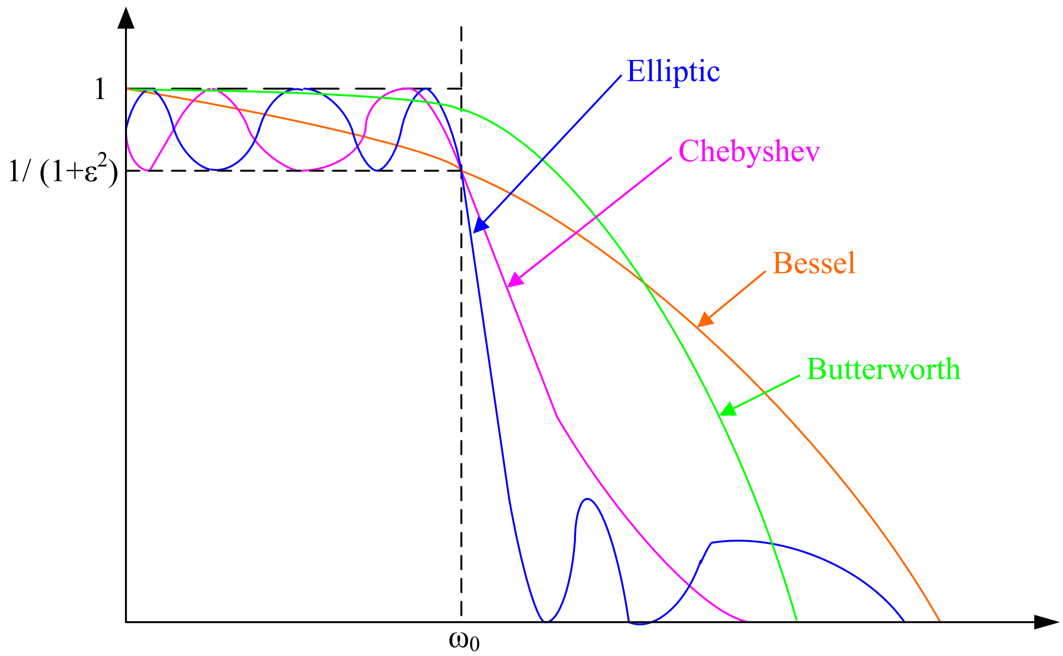

Figure 2.7: Lowpass magnitude response of various types of filter [Soorapanth, 2002].

2.6. CMOS Analog Filter

Although there are increasing many filtering applications are now handled with digital signal processing technique and digital filters because of its high immune to noise, but there are a number of situations in which analog filter is still favorable solution. First, the real world signal is in analog form. Signal needs to be discretized and digitized, i.e. sampled and converter to digital form before digital filter can processes signal. Hence, extra component such as analog to digital converter and sampling circuit are needed to perform the converter and sampling function. Second, filtering at very high frequency especially in front end receiver, require ultra-fast sampling and digital filter are not realistic and economical [Schaumann and Valkenburg, 2001].

Figure 2.8 shows the choice of various analog filter types as a function of operating frequency range. For our filter design, the operating frequency (cutoff frequency) is 264MHz, therefore, integrated analog active filters and passive LC filters are the only two choices among various analog filter that can be implemented to fulfill our design requirement.

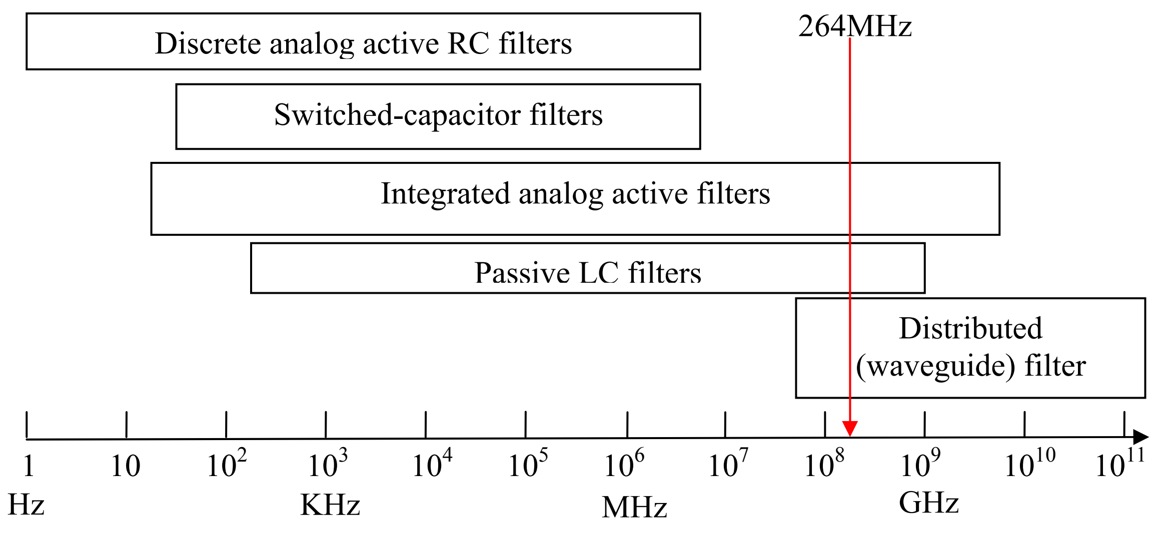

Figure 2.8: Choice of filter type as a function of operating frequency range [Schaumann and Valkenburg, 2001].

2.7. Passive Filter

The passive filters are made up of passive components: resistors, capacitors, and inductors. A passive filter is simply a filter that uses no amplifying elements (transistors, operational amplifiers, etc.). In this respect, it is the simplest implementation of a given transfer function. Passive filters have other advantages as well. Because they have no active components, passive filters require no power supplies. Since they are not restricted by the bandwidth limitations of op amps, they can work well at very high frequencies (can up to GHz). One of the disadvantage of passive filter is the inductor is the most difficult to realize in integrated form. This is especially true at low frequencies where inductors become bulky and have increased losses or equivalently lower Q factors. Besides that, inductors are expensive, unreliable, big, and can not be used in IC chips.

2.8. Integrated Analog Active filter

There are three main types of integrated analog active filters such as active-RC filters, MOSFET-C filters and Gm-C filters

2.8.1. Active-RC Filter

Active filters use amplifying elements, especially op amps, with resistors and capacitors in their feedback loops, to synthesize the desired filter characteristics. Active filters can have high input impedance, low output impedance, and virtually any arbitrary gain. They are also usually easier to design than passive filters [Lacanette, 1991]. Due to the lack of inductor in active-RC filter, the problems associated with inductor are eliminated. The disadvantage of active-RC filters is the use of op-amp generally limits the performance at high frequencies due to the gain-bandwidth product of the amplifying elements. As a rule of thumb, the active-RC filter is generally not designed to operate at frequency above 5 or 10% of the gain-bandwidth product of op-amp. The operating frequency of active-RC filter is limited to hundreds of kilo hertz.

2.8.2. MOSFET-C filters

MOSFET-C filters are similar to active-RC filters except the bulky resistor is replaced by an equivalent CMOS transistor which operates in triode region. The equivalent CMOS transistor is much smaller in layout size and can tunes to higher resistance value. However, MOSFET-C filters are generally slower response than Gm-C filter since they use Miller integration [John & Martin, 1997]. The operating frequency of MOSFET-C filters also limited to hundreds of kilo hertz due to the frequency response of op-amp.

2.8.3. Gm-C filters

Gm-C filters use only voltage-to-current transconductors and capacitors as basic component. Other components like integrator and inductor can be implemented by using these basic two components. Gm or transconductance amplifiers are voltage-controlled current sources which its output current I_o is proportional to the differential input voltage, $I_{out} = g_m V_{in}$. Compare with op-amp, Gm has a tunable transconductance value and can operate in high frequency up to hundreds of megahertz.

2.9. Design Goals

The scope of this project is to design a completely integrated low pass filter with a bandwidth 264MHz utilizing Silterra 0.18μm SMCMOS technology. Currently, many published journals are suggesting the using of transconductor-capacitor filter as the high frequency active filter. But there still does no have a standard specification for UWB low pass filter by using transconductor-capacitor filter. The basic requirements for UWB low pass filter are its bandwidth 264MHz, low power consumption and high linearity. Therefore, analysis on a various order Gm-C filters includes filter gain response, phase response, transient response, linearity, power consumption are conducted. The performance of filters will be compared and the order filter which gives the best overall performance will be chosen to be implemented as baseband filter for UWB application.

Table 2.1: Design goals for UWB low pass filter.

Parameters	
Cutoff frequency	264MHz
DC gain	0dB
1dB compression point	≥-1dBm
IP3	≥5dBm
Power consumption	≤30mW

2.10. Filter Characteristics

2.10.1 Gain and Phase

The filters are linear circuits that can be represented by the general two-port network shown in Figure 2.9 [Sedra & Smith, 1998].

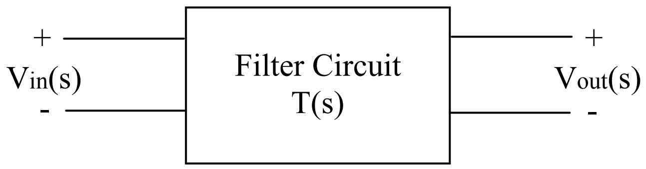

Figure 2.9: Filter represent by two-port network.

The filter transfer function T(s) is the ratio of the output voltage $V_{out}(s)$ to the input voltage $V_{in}(s)$,

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} \tag{2.3}$$

The filter transmission is found by evaluating T(s) for physical frequencies, s = jw, and can be expressed in terms of its magnitude and phase as

$$T(jw) = |T(jw)|e^{j\phi(w)} \tag{2.4}$$

The magnitude of transmission is often expressed in desibels in terms of the gain function

$$G_{dB} \equiv 20\log_{10}|T(jw)|$$

$$= 20\log_{10}\frac{V_{out}}{V_{in}} \tag{2.5}$$

A filter shapes the frequency spectrum of the input signal, $|V_{in}(jw)|$, according to the magnitude of the transfer function $|T(jw)|$, thus providing an output $V_{out}(jw)$ with a spectrum

$$\left|V_{out}(jw)\right| = \left|T(jw)\right| \cdot \left|V_{in}(jw)\right| \tag{2.6}$$

Also, the phase characteristics of the signal are modified as it passes through the filter according to the filter phase function $\phi(w)$.

2.10.2 Linearity

Linearity is an important parameter for any amplifier includes transconductor. It is desired that the amplifier operate with high linearity i.e., the output power be linear with input power. However, a device eventually saturates after a certain input power, and this introduces harmonics in the output power spectrum. Linearity in transconductor is of serious concern because they can be often made to operate in the non-linear region to deliver a large output power. 1-dB compression and third order intercept points are typically used to measure linearity.

2.10.2.1 1-dB compression

As the name suggests, 1-dB compression point is the point at when the input power at which the linear gain of the amplifier has compressed by 1 dB as shown in Figure 2.10. Active components like transconductor are limited to the amount of power that can be provided. When transconductor operating within the linear region, gain through the transconductor is constant for a given frequency. As the power of input signal is increased beyond 1 dB compression point, the power of the signal at the output is not amplified by the same amount as the input signal. A rapid decrease in gain will be experienced after the 1-dB compression point is reached. If the input power is increased to an extreme value, the component will be destroyed. The output referred 1-dB compression point (in dB) would then be given by the sum of the input referred 1-dB point (in dB) and the gain of the amplifier (in dB) as shown in Eq. (2.7)

$$\text{P1dB (output)} = [\text{P1dB (input)} + (\text{Gain} - 1)] \text{ dBm} \tag{2.7}$$

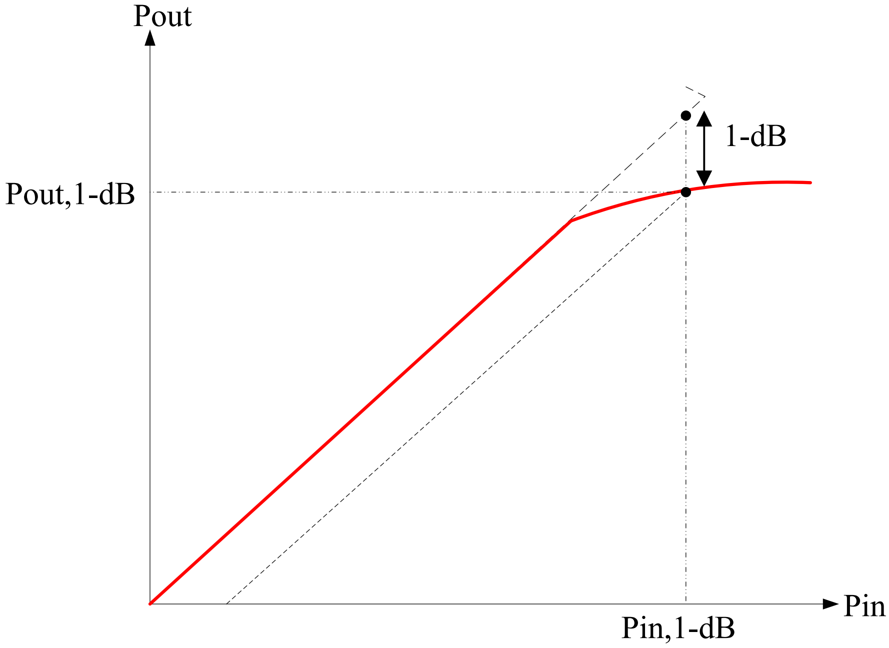

Figure 2.10: 1 dB compression point characteristic.

2.10.2.2 Third-order Intercept Point (IP3)

IP3 is a useful metric when comparing RF blocks with different specifications as it is independent of the input power levels. Assuming two interferers very close to the desired frequency, a non-linear output from the amplifier will generate inter-modulation (IM) products. The most important of the products is the third order product since it falls directly in the frequency band of interest. This situation is shown in Figure 2.11.

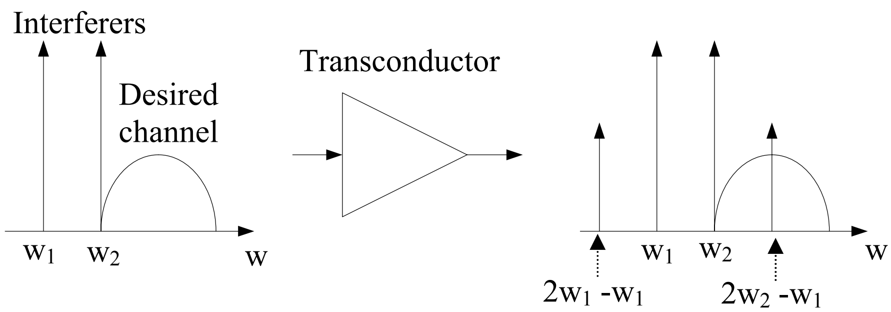

Figure 2.11: Forming of the third order products due to nearby interferers

The amplitude of this inter-modulation product (IM3) term increases in the order of cube of the fundamental amplitude and can be as significant as the fundamental tone after a certain input power. Figure 2.12 shows a plot of the IM3 product as a function of the input RF level. The third-order intercept point is the extrapolated intersection of this curve and the fundamental power. The input/output referred IP3 can be estimated from this plot.

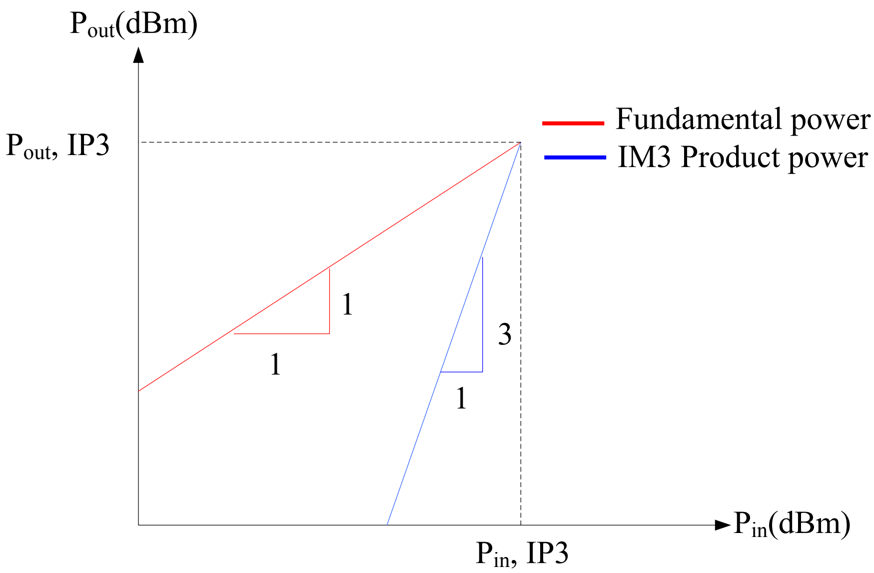

Figure 2.12: Third-order intercept point plot.

CHAPTER 3

DESIGN OF Gm-C LOWPASS FILTER

3.1. Introduction

The main building block for the proposed Butterworth Gm-C low pass filter is an integrator. In this thesis, the integrator will be implemented by a transconductance cell loaded with a capacitor. Therefore, a transconductance cell is designed to have a good characteristic such as high input and low output impedance, well define and tunable voltage to current conversion value (transconductance), large bandwidth and high DC gain.

3.2. Transconductance Cell

Transconductance cell is basically is act as an active element/amplifier to generate an output current I_o which is proportional to the differential input voltage as shown in Eq. (3.1). The transconductance cell is different from the operational transconductance amplifier (OTA) and operation amplifier (Op-amp). The output current of OTA is not linearly related to the supplied input voltage while the output voltage (no the output current) of op-amp is linearly proportional to the input voltage

$$I_o = g_m V_i \tag{3.1}$$

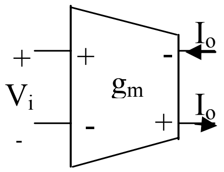

Figure 3.1: Single transconductance cell

For ideal transconductance, the input impedance is assumed to be infinite while output impedance is assumed to be zero.

$$R_i = \infty \qquad ; \quad R_{out} = 0$$

Eq. $R_i = \infty$ implies that an open circuit at the input of transconductor and hence draws no input current:

$$I_{i+} = I_{i-} = 0$$

Eq. $R_{out} = 0$ implies that an ideal current source (no voltage drop) and able to drive any load.

For practical transconductor, finite input and output impedance will exist as shown in Figure 3.2:

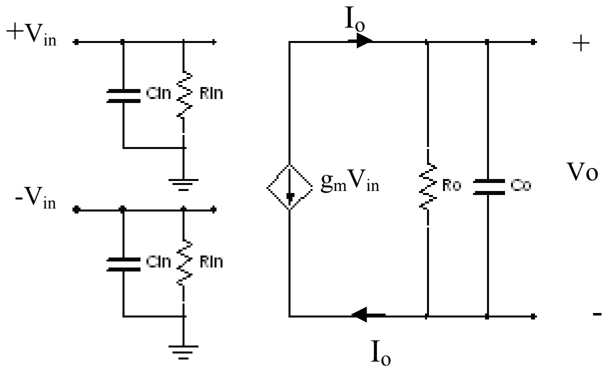

Figure.3.2: Small signal model for finite input and output impedance of a transconductance [Schaumann and Valkenburg, 2001].

The new transfer function for practical transconductor after takes into account input and output impedance is:

$$V_o = \frac{g_m R_o}{1 + sR_oC_o}\left(V_{in}\right) \tag{3.2}$$

From Eq. (3.2), the parasitic resistance introduces a small dc gain to inverter while the parasitic capacitance modifies the characteristics of frequency response (cutoff frequency and phase error). In order to avoid errors in the filter characteristic, integrator requires a sufficiently high dc gain while the parasitic poles should be located at frequency much higher than the cutoff frequency of the filter [Nauta, 1992].

3.3. Design of Transconductance Cell

A single Gm cell as proposed by Bram Nauta (1993) is basically consists of 6 standard CMOS logic inverters as shown in Figure 3.3. This design is using fully differential input and output structure, which implies that only the difference in voltage between inverter 1 and inverter 2 will be processed. The main advantages of differential operation over single-ended signaling are higher immunity to common mode noise and increase in maximum achievable voltage [Razavi, 2001] Moreover, the differential signal will have only odd-order distortion and free of even order distortion.

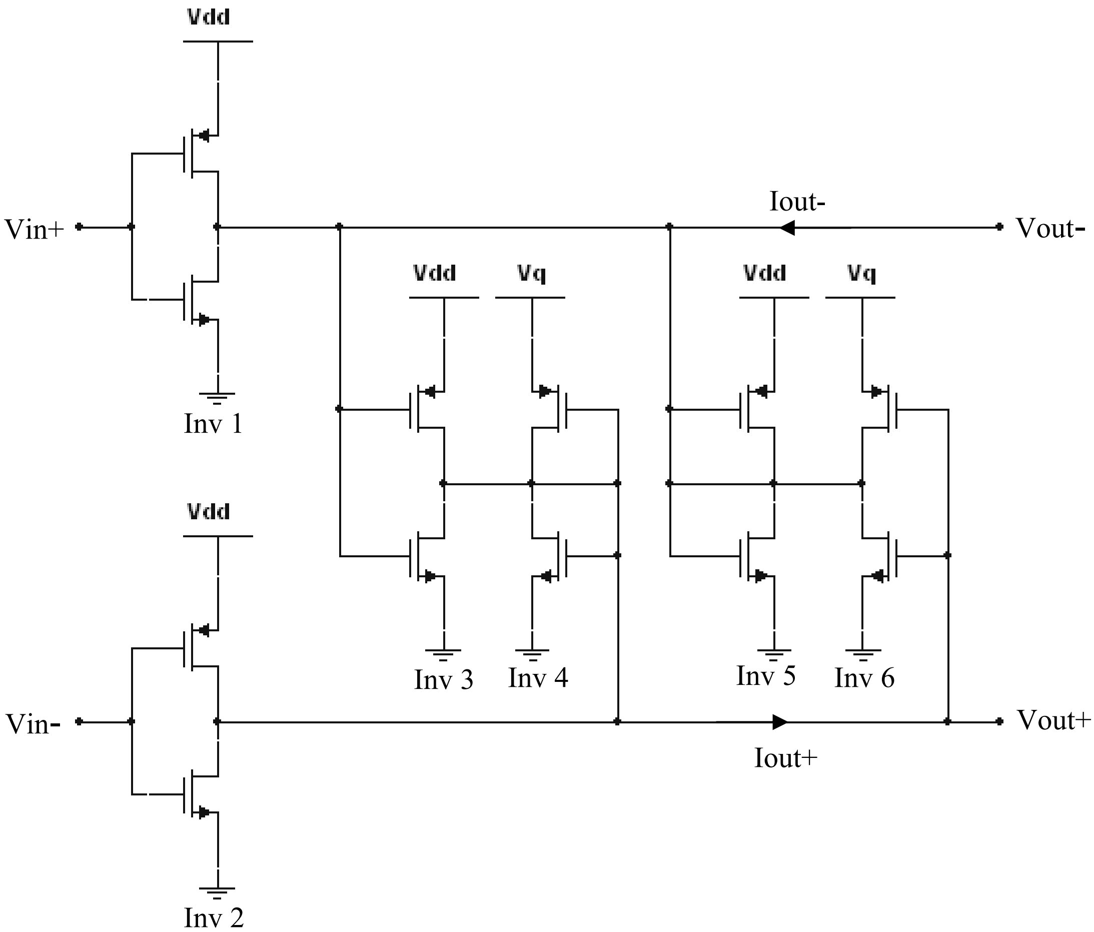

Figure 3.3: Nauta's balanced transconductance cell [Nauta, 1992].

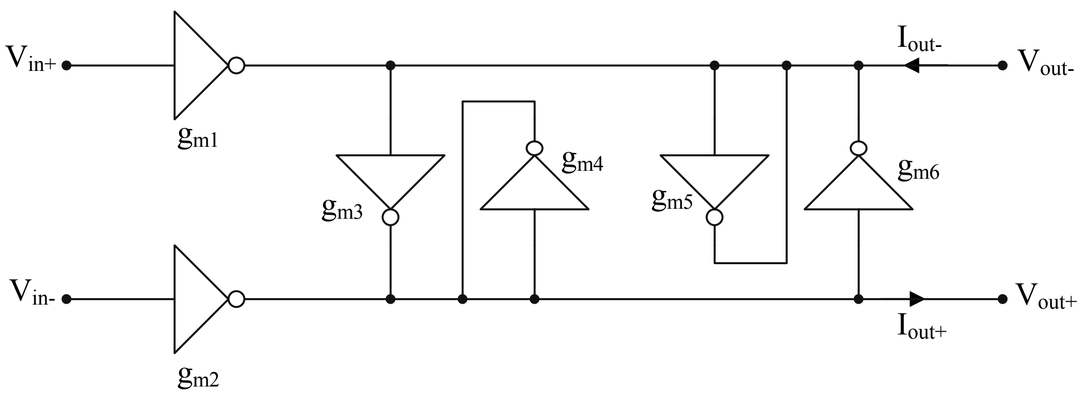

Figure 3.4: Nauta's balanced transconductance cell in term of inverter symbol

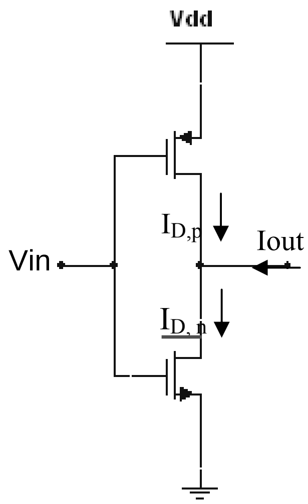

Figure 3.5: Schematic of single inverter

3.3.Design Approach

The design approach as proposed by [Low, 2005] is applied and modified to determine the width of every transistor in Figure 3.3

3.4.1. Inverter Circuitry

Inverter 1 and 2 are used to convert the differential input voltage into differential output current. To achieve maximum output voltage swing, both inverters are operating in saturation region and must be matched to drive differential signal to balance around common mode voltage at half of V_{DD}, i.e.0.9V. Therefore, the W/L ratio for PMOS and NMOS can be tuned to have the output voltage operates at 0.9V. The length L is chosen to be 0.18µm.

Consider only NMOS of a single inverter, the drain current, I_D is depending on the operation mode of NMOS.

i. For the transistor operating in cutoff region, the drain current is zero.

$$I_D = 0 \qquad \text{for } V_{GS} < V_{TH}$$

ii. For the transistor operating in triode region, the drain current is given by:

$$I_D = \mu_n C_{ox} \frac{W_n}{2L_n}(2V_{GS} - V_{TH})V_{DS} - V_{DS}^{\;2} \qquad \text{for} \quad V_{GS} > V_{TH} \; and \; V_{DS} < V_{DS,sat} \qquad (3.3)$$

iii. For the transistor operating in saturation region, the drain current is given by

$$I_D = I_{D,sat} = \mu_n C_{ox} \frac{W_n}{2L_n}(V_{GS} - V_{TH})^2 \qquad \text{for} \quad V_{GS} > V_{TH} \; and \; V_{DS} < V_{DS,sat} \qquad (3.4)$$

For the Eq. above, μ_n = carrier mobility electron

W = channel width

L = channel length

V_t = threshold voltage

C_{ox} = gate oxide capacitance per unit area

Transconductance, g_m for single transistor, NMOS is derived as:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS,cons\tan t}$$

$$g_m = \mu_n C_{ox} \frac{W_n}{L_n}(V_{GS} - V_{t,n}) \quad = \sqrt{2\mu_n C_{ox} \frac{W_n}{L_n} I_D} = k_n(V_{GS} - V_{t,p}) \qquad (3.5)$$

If the transconductor in Figure 3.3 has no internal nodes and the *k* factor of the n-channel and p-channel are matched for all CMOS inverter, then the transconductor will have a good linearity in voltage to current conversion. For analog design, the CMOS inverters have to be operating in saturation region and the hence drain current is defined as:

$$I_{D,n} = \frac{k_n}{2}\left(V_{GS,n} - V_{t,n}\right)^2 \quad \text{with} \quad k_n = \frac{\mu_n C_{ox} W_n}{L_n} \qquad \text{for NMOS} \qquad (3.6)$$

$$I_{D,p} = \frac{k_p}{2}\left(V_{GS,p} - V_{t,p}\right)^2 \quad \text{with} \quad k_p = \frac{\mu_p C_{ox} W_p}{L_p} \qquad \text{for PMOS} \qquad (3.7)$$

The output current of a single inverter is given by:

$$I_{out} = I_{D,n} - I_{D,p}$$

$$= \frac{k_n}{2}\left(V_{GS,n} - V_{t,n}\right)^2 - \frac{k_p}{2}\left(V_{GS,p} - V_{t,p}\right)^2$$

$$=\frac{k_n}{2}\left(V_{in}-V_{tn}\right)^2-\frac{k_p}{2}\left(V_{in}-V_{DD}-V_{t,p}\right)^2$$

$$=\frac{k_n}{2}\left(V_{in}-V_{t,n}\right)^2-\frac{k_p}{2}\left(V_{in}^2-2V_{in}V_{DD}+V_{DD}^2+V_{t,p}^2-2V_{in}V_{t,p}+2V_{DD}V_{t,p}\right)$$

$$=\frac{k_n}{2}\left(V_{in}-V_{t,n}\right)^2-\frac{k_p}{2}V_{in}^2+k_pV_{in}V_{DD}-\frac{k_p}{2}V_{DD}^2-\frac{k_p}{2}V_{t,p}^2+k_pV_{in}V_{t,p}-k_pV_{DD}V_{t,p}$$

$$=\frac{k_n}{2}\left(V_{in}-V_{t,n}\right)^2-\frac{k_p}{2}\left(V_{in}^2-2V_{in}V_{t,n}+V_{t,n}^2\right)+k_pV_{in}\left(V_{DD}-V_{t,n}+V_{t,p}\right)$$

$$+\frac{k_p}{2}\left(V_{t,n}^2-V_{DD}^2-V_{t,p}^2-2V_{DD}V_{t,p}\right)$$

$$=\frac{k_n}{2}\left(V_{in}-V_{t,n}\right)^2-\frac{k_p}{2}\left(V_{in}-V_{t,n}\right)^2+k_pV_{in}\left(V_{DD}-V_{t,n}+V_{t,p}\right)$$

$$+\frac{k_p}{2}\left(V_{t,n}^2-V_{DD}^2-V_{t,p}^2-2V_{DD}V_{t,p}\right)$$

$$=\frac{1}{2}\left(k_n-k_p\right)\left(V_{in}-V_{t,n}\right)^2+k_pV_{in}\left(V_{DD}-V_{t,n}+V_{t,p}\right)+\frac{k_p}{2}\left\{V^2{}_{t,n}-\left(V_{DD}+V_{t,p}\right)^2\right\}$$

$$=\frac{1}{2}\left(k_n-k_p\right)\left(V_{in}-V_{t,n}\right)^2+k_pV_{in}\left(V_{DD}-V_{t,n}+V_{t,p}\right)+\frac{k_p}{2}\left\{V^2{}_{t,n}-\left(V_{DD}+V_{t,p}\right)^2\right\}$$

$$=a\left(V_{in}-V_{t,n}\right)^2+bV_{in}+c \qquad (3.8)$$

with $a=\frac{1}{2}\left(k_n-k_p\right)$

$$b=k_p\left(V_{DD}-V_{t,n}+V_{t,p}\right)$$

$$c=\frac{k_p}{2}\left[V_{t,n}^2-\left(V_{DD}+V_{t,p}\right)^2\right]$$

For common mode input signal, I_{out} is equal to zero and V_{in} is equal to $V_{CM.}$ Derivation of common mode voltage, V_{cm} for the transconductor is shown as below:

$$I_{out}=I_{D,n}-I_{D,p}$$

$$I_{D,n}=I_{D,p}\quad\text{when } V_{in}=V_{cm}$$

$$\frac{k_n}{2}\left(V_{GS,n}-V_{t,n}\right)^2=\frac{k_p}{2}\left(V_{GS,p}-V_{t,p}\right)^2$$

$$\frac{k_n}{k_p}\left(V_{in}-V_{t,n}\right)^2=\left(V_{in}-V_{DD}-V_{t,p}\right)^2$$

$$\frac{k_n}{k_p}\left(V_{in} - V_{t,n}\right)^2 = \left(-V_{in} + V_{DD} + V_{t,p}\right)^2$$

$$\sqrt{\frac{k_n}{k_p}}\left(V_{cm} - V_{t,n}\right) = \left(-V_{cm} + V_{DD} + V_{t,p}\right)$$

$$\left\langle 1 + \sqrt{\frac{k_n}{k_p}} \right\rangle V_{cm} = V_{DD} + V_{t,p} + \sqrt{\frac{k_n}{k_p}} V_{t,n}$$

$$V_{cm} = \frac{V_{DD} + V_{t,p} + \sqrt{\frac{k_n}{k_p}} V_{t,n} - V_{t,n} + V_{t,n}}{1 + \sqrt{\frac{k_n}{k_p}}}$$

$$V_{cm} = \frac{V_{DD} + V_{t,p} - V_{t,n}}{1 + \sqrt{\frac{k_n}{k_p}}} + \frac{\left\langle 1 + \sqrt{\frac{k_n}{k_p}} \right\rangle V_{tn}}{1 + \sqrt{\frac{k_n}{k_p}}}$$

$$V_{cm} = \frac{V_{DD} - V_{t,n} + V_{t,p}}{1 + \sqrt{\frac{k_n}{k_p}}} + V_{t,n} \tag{3.9}$$

Whenever $V_{t,n}$ equal to $V_{t,p}$ and k_n equal to k_p, V_{cm} = 0.9V.
The all equations above had been proposed by [Nauta, 1992] and [Chan, 2003].

We know that $k_n = \frac{\mu_n C_{ox} W_n}{L_n}$ for NMOS and $k_p = \frac{\mu_p C_{ox} W_p}{L_p}$ for PMOS

If k_n equal to k_p, then $\frac{\mu_n C_{ox} W_n}{L_n} = \frac{\mu_p C_{ox} W_p}{L_p}$

where $L_{,n} = L_{,p}$ =0.18µm and C_{ox} is assumed to be same.
Therefore $\mu_n W_n = \mu_p W_p$
Given that $\mu_n \approx 3\mu_p$, $W_p \approx 3W_n$

Thus, width of PMOS transistor should be 3 times greater than width of NMOS transistor.

V_{cm} is exactly 0.9V when simulated with W_n =1.98µm and W_p = 6.17µm as shown in Figure 3.6.