

**DESIGN OF POWER AMPLIFIER FOR
ULTRA-WIDEBAND (UWB) APPLICATIONS
USING SILTERRA 0.18 μm CMOS TECHNOLOGY**

Oleh

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Abstrak

Penguat kuasa untuk sistem transceiver Ultra-Wideband (UWB) telah direkabentuk. UWB adalah satu teknologi perhubungan tanpa talian khas untuk jarak dekat (kurang daripada 10m) yang mampu mencecah kadar penghantaran data sehingga 480 Mbps. UWB adalah teknologi berkuasa rendah yang mampu wujud serentak dengan kehadiran teknologi Bluetooth, GPS dan WiFi. Penguatkuasa yang direkabentuk adalah khas untuk sistem transceiver UWB yang mengaplikasikan teknik “direct conversion” dan MB-OFDM (Multi-band Orthogonal Frequency Division Multiplexing) serta beroperasi dalam mod satu UWB iaitu frekuensi dalam lingkungan 3.1 GHz hingga 4.9 GHz. Penguat kuasa ini direkabentuk menggunakan teknologi Silterra 0.18 μ m CMOS dan hasil rekabentuk adalah dalam tiga versi iaitu IDEAL, SIL18RF dan ASITIC. Penguat kuasa ini telah direka menggunakan gegelung dalam SIL18RF dan gegelung ASITIC. Penguat kuasa dengan component ideal memperoleh $S_{11} < -31$ dB, $S_{12} < -75$ dB, $S_{21} = 19.45 \pm 0.64$ dB dan $S_{22} < -10$ dB. Kes IDEAL juga memperoleh input referred 1 dB compression point, -17.44 dBm dan kuasa keluran maximum, 1.49 dBm dengan menggunakan kuasa DC sebanyak 31.3 mW. Di samping itu, kes SIL18RF memperoleh $S_{11} < -10$ dB, $S_{12} < -82$ dB, $S_{21} = 16.39 \pm 0.68$ dB dan $S_{22} < -10.3$ dB sementara kes ASITIC memperoleh $S_{11} < -25$ dB, $S_{12} < -82$ dB, $S_{21} = 19.66 \pm 1.45$ dB dan $S_{22} < -10.8$ dB. SIL18RF mendapat input referred 1 dB compression point, -14.4 dBm dan kuasa keluaran maximum sebanyak 1.38 dBm sementara ASITIC mendapat input referred 1 dB compression point, -13.57 dBm dan kuasa keluaran maximum sebanyak 2.12 dBm. Kes SIL18RF dan ASITIC hanya menggunakan kuasa DC sebanyak 30.87 mW dan 31.63mW masing-masing. Layout SIL18RF iaitu 3.7mmx2.6mm adalah lebih besar daripada layout ASITIC yang dianggarkan sebanyak 0.55mmx0.85mm. Satu PCB (Printed Circuit Board) dengan dimensi 60mmx80mm telah direka untuk mengukur chip SIL18RF. Selain daripada rekabentuk penguatkuasa, satu kerja pengukuran telah dijalankan ke atas MAX2242EVKIT menggunakan alatan RF yang canggih. Daripada hasil pengukuran, didapati MAX2242 mengeluarkan kuasa keluaran sebanyak 26 dBm dengan kuasa masukan 5 dBm pada bekalan kuasa 3.3V.

Abstract

A power amplifier for Ultra-Wideband (UWB) transceiver system is presented. UWB is a high data rates (up to 480 Mbps) wireless communication technology for short distance (less than 10m) applications. UWB technology is a low power (-41.3 dBm/MHz) wireless communications that can coexist with the existing technology such as Bluetooth, GPS (Global Positioning System) and WiFi. The power amplifier is designed for UWB direct conversion (DICON) transceiver system that employs Multi-band Orthogonal Frequency Division Multiplexing (MB-OFDM) approach and operates in mode 1 (3.1 to 4.9GHz) of UWB spectrum. The power amplifier is designed using Silterra 0.18 μ m CMOS technology in three different version which consists of IDEAL, SIL18RF and ASITIC case. The power amplifier has been implemented in two versions which are SIL18RF inductor and ASITIC inductor. IDEAL case achieved $S_{11} < -31$ dB, $S_{12} < -75$ dB, $S_{21} = 19.45 \pm 0.64$ dB and $S_{22} < -10$ dB. IDEAL version also achieved input referred 1 dB compression point of -17.44 dBm and maximum output power of 1.49 dBm while consuming only 31.3 mW. On the other hand, SIL18RF version achieved $S_{11} < -10$ dB, $S_{12} < -82$ dB, $S_{21} = 16.39 \pm 0.68$ dB and $S_{22} < -10.3$ dB while ASITIC version achieved $S_{11} < -25$ dB, $S_{12} < -82$ dB, $S_{21} = 19.66 \pm 1.45$ dB and $S_{22} < -10.8$ dB. SIL18RF version obtained input referred 1 dB compression point of -14.4 dBm and maximum output power of 1.38 dBm while ASITIC version achieved input referred 1 dB compression point of -13.57 dBm and maximum output power of 2.12 dBm. SIL18RF and ASITIC version only consume 30.87 mW and 31.63mW respectively. The layout dimension of SIL18RF version is 3.7mm x 2.6mm which is bigger than ASITIC version estimated to be 0.55mm x 0.85mm. A PCB (Printed Circuit Board) with dimension of 60mm x 80mm has been designed to characterize SIL18RF fabricated chip. Beside power amplifier design, a measurement task has been carried out to evaluate the performance of MAX2242EVKIT using radio frequency high end tools. From measurement results, MAX2242 can produce +26 dBm output power at 5 dBm input power and 3.3V power supply.

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CHAPTER 1

INTRODUCTION

1.1 Introduction to Ultra-Wideband (UWB) Technology

Communications technology has undergone rapid development for wireless applications over the last few decades. Nowadays, there are new challenges to be faced for a new receiver technology due to the fact that high frequency signal in current narrow-band and wide-band technologies cannot meet the demands for high data rate transmission, secure communication and better material penetration. As a result, a new technology, namely Ultra-Wideband (UWB) is introduced.

The Federal Communication Commission (FCC) has allocated 7.5 GHz (from 3.1 GHz to 10.6 GHz) bandwidth for unlicensed use of Ultra-Wideband (UWB) technology on February 14, 2002[Intel, 2005]. Since then, interest has been renewed in both academic and industrial circles to exploit this vast spectrum for short range, high data rate wireless applications [Barr et. al, 2003]. In fact, the industries have focused on UWB for Wireless Personal Area Network (WPAN) [Barr et. al, 2003] applications. Two proposals for IEEE 802.15.3a (standard for WPAN) [Barr et. al, 2003] show that data rate up to 110 Mb/s can be obtained merely using low frequency band (3.1 to 4.9 GHz) out of the total 7.5 GHz bandwidth through MB-OFDM (Multi-band Orthogonal Frequency Division Multiplexing) [Welborn, 2003] and DS-SS (Direct Sequence Code Division Multiple Access) [McCorkle, 2003] approach respectively. Thus, the low frequency band has been allocated for the first generation of UWB system though the standard approach has not yet being finalized.

Actually, UWB is not a new but existing wireless radio technology originally developed for secure military communication and radar system which is now declassified. In the future, UWB technology will be ideally suited for data transmission between consumer electronics (CE), PC peripherals, and mobile devices within short range at very high speeds while consuming little power [Siwiak et. al, 2001]. Furthermore, it has the capacity to handle the very wide bandwidths required to

transport multiple audio and video streams. This new technology operates at a power level that most systems interpret as noise, therefore does not cause interference to the existing systems such as cell phones, cordless phones or broadcast television sets.

UWB is a low power technology that supports high data rate communication, which covers area within a short distance (less than 10 m) for personal connectivity. Hence, UWB technology is the complementary of IEEE 802.11 WLAN (Wireless Local Area Network) that frees the users from wired world and promotes wireless freedom. In other words, UWB technology provides the convenience of data transmission at very high data rate between electronic devices such as digital camera, printer, video camera and computer simultaneously without any cable or physical connection.

Due to the potential applications and market of UWB technology in short distance wireless communication, there is a need to study on this attractive technology. Hence, the main effort in this thesis will focus on the design of 3.1 to 4.9 GHz CMOS power amplifier for UWB transceiver system using Silterra 0.18 μ m CMOS technology. The targeted UWB transceiver system applies direct conversion architecture and implements MB-OFDM approach. In short, this power amplifier is designed particularly for IEEE 802.15.3a standard.

1.2 Objective

The main objective of this project is to design a CMOS power amplifier for UWB transceiver system, which applies MB-OFDM (Multi-band Orthogonal Frequency Division Multiplexing) approach and operates in mode 1 of UWB spectrum (3.1 to 4.9 GHz). The CMOS power amplifier will be designed in Silterra 0.18 μ m CMOS Technology and targets for IEEE 802.15.3a. IEEE 802.15.3a is the standard for UWB application in Wireless Personal Area Network (WPAN) [Barr et. al, 2003]. The ultimate design will be sent to Silterra for fabrication.

The second objective of this project is to enhance personal hand on skill in tools and instruments handling as well as measurement skills. Hence, MAX2242EVKIT which is a hardware of power amplifier is bought particularly for measurement. The

performance of the power amplifier will be measured using high end equipments, which are available in the laboratory and the obtained measurement results will be compared to the power amplifier's characteristics listed in the data sheet.

1.3 Design Flow

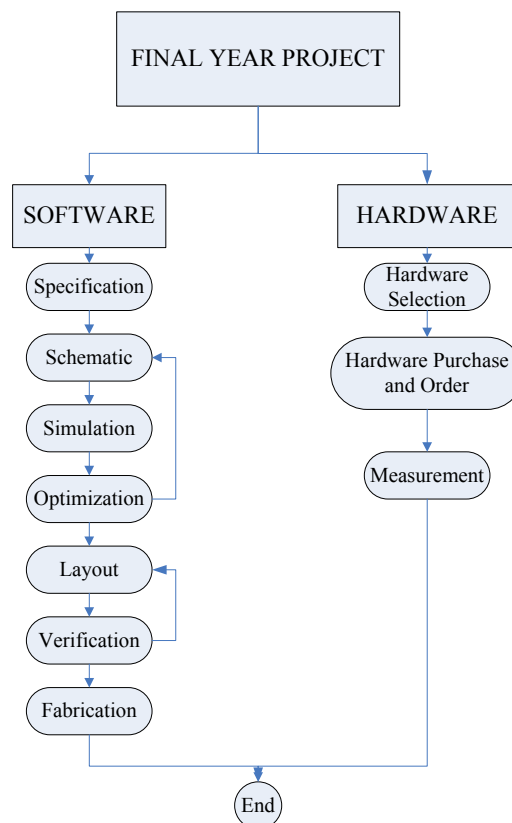


Figure 1 Design flow of the project.

The design flow of the entire project can be illustrated in Figure 1. The project is divided into two parts, software and hardware, respectively. The only tool needed in software part is CADENCE with Silterra CMOS 0.18 μ m CMOS Technology library while hardware part requires measurement tools and hardware kit. The software part can be started independently compare to hardware part because the tools needed in software part are provided. As for hardware part, it involves hardware selection and purchase, which is time consuming. Hence, software and hardware part are carried out in parallel.

Software part involves several standard stages, which include Specification, Schematic Entry, Simulations, Optimization, Layout Design, Verification, Parasitic Extraction and Fabrication. Specification stage emphasizes on information collection and studies on UWB technology. The main objective is to find the specifications for CMOS power amplifier design that is suitable for UWB transceiver system. The next stage is Schematic Entry. The main effort is to find the most effective and efficient topology that tackles the desired specifications. The resulted schematic will be constructed and simulated with CADENCE in Simulation stage. The simulation results are then compared to the specifications and then optimized. Only if the simulations results are conformed to the specifications, the design can proceed to Layout Design or else the design will need to be replaced or altered by repeating the same procedures until the simulation results conform to the specifications. In Layout Design, the main focus is to construct a layout of the designed power amplifier with a minimum area to reduce the cost of fabrication. Next, the constructed layout will proceed to Verification, which includes Design Rule Check (DRC) and Layout Versus Schematic (LVS). DRC checks if the layout obeys a set of rules that guarantees proper transistor and interconnect fabrication despite various tolerances in each step of processing while LVS checks the mismatch between the schematic and the layout. Finally, the power amplifier will be sent to Silterra for fabrication.

Differ from software part, hardware part begins with hardware selection. The major concern is to choose a hardware which is suitable for measurement. It is important to make sure that the equipment or tools required to measure the performance of the hardware are available in the laboratory. After the hardware is determined, the purchase and order of the hardware need to be done as soon as possible. The measurement results are recorded, presented and then compared to the specification. The measurement is complete if measurement results approximate the specifications.

1.4 Project Overview

This thesis consists of 9 chapters which includes Introduction, Ultra-Wideband

technology, Power Amplifier, Power Amplifier for MB-OFDM, Design and Analysis Of Power Amplifier For UWB Application, Result and Discussion, Layout, Measurement and Conclusion.

Chapter 1 briefs through the general characteristics and advantages of UWB technology. This chapter also touches on the objectives and describes the design flow of the entire project.

Chapter 2 presents the theory and fundamental of UWB technology in more details. Several topics, which include the background of UWB technology, the standard for UWB applications, different approaches to exploit UWB spectrum and the advantages of UWB technology are mentioned.

Chapter 3 covers the basic types of conventional power amplifier and the performance merits to evaluate the performance of a power amplifier.

Chapter 4 is the core of the project which explains the initial stage of power amplifier design. The chapter begins with the specifications of the power amplifier and discusses certain characteristics of UWB power amplifier that differ from ordinary power amplifier. Several topologies suitable to tackle each characteristic of UWB PA are discussed and the chapter ends with the overall schematic of the UWB PA.

Chapter 5 shows the design steps, which include simulation, circuit analysis and calculation to determine the dimension for each transistor and passive element.

Chapter 6 includes the simulation results of the power amplifier. There are three version of power amplifier, which has been designed. Hence, the simulation results compare the performance of these three power amplifier. It shows the real implementation of the design in two different versions, which are SIL18RF and ASITIC inductor. SIL18RF version consists of inductors obtained from Silterra 0.18 μ m CMOS Technology library while ASITIC version implements inductors designed using ASITIC software. Their performance are discussed and compared to the ideal simulation results.

Chapter 7 shows the layout design of two different implementations of power amplifiers. It shows the dimension of SIL18RF power amplifier and explains the replacement of the inductors with ASITIC inductors. This chapter ends with ASITIC

inductor design and LVS report of the design.

Chapter 8 shows the tools setup constructed to evaluate MAX2242EVKIT. It shows the tools and connection used to measure the hardware. The measurement result is compared to the specifications listed in the data sheet. A PCB (Printed Circuit Board) designed to evaluate SIL18RF fabricated chip is also mentioned

Chapter 9 concludes the performance of the UWB power amplifier and compares its performance with several designs done by experts in the industries. This chapter ends with suggestions that can be implemented to improve the UWB power amplifier design in future.

CHAPTER 2

ULTRA-WIDEBAND (UWB) TECHNOLOGY

Ultra-Wideband (UWB) Technology is a leading wireless personal area networks (WPAN) technology. It is a promising technology that allows UWB signal to coexist with other radio services with minimal interference while provides high data rates, secure communication and better material penetration [Welborn, 2003].

In this chapter, the overview of UWB background is presented. The understanding of UWB signal and the emission power level of UWB signal make it much different from conventional technology. This chapter ends with the UWB standard, which consists of Multi-band Orthogonal Frequency Division Multiplexing (MB-OFDM) and Direct Sequence Code Division Multiple Access (DS-CDMA).

2.1 UWB Background

On Feb. 14 2002, the Federal Communications Commission (FCC) has opened up 3.1 GHz to 10.6 GHz spectrum for unlicensed use of the Ultra-wideband (UWB) technology. Having such a wide and free spectrum at one's disposal is especially alluring for the industry as well as the academia. However, the power levels of the UWB signal in this spectrum must be low enough to avoid interference with the already existing technologies. The FCC has specified the power emission levels suitable for co-existing with other technologies in the UWB allocated band [Fontana, 2004]. The FCC defines UWB as a signal with either a fractional bandwidth of 20 % of the center frequency or 500 MHz (when the center frequency is above 6 GHz). The formula proposed by the FCC commission for calculating the fractional bandwidth is shown in Eq 2.1. The spectrum mask for both indoor and outdoor emissions is shown in Fig. 2.1.

$$B_{rel} = \frac{f_h - f_l}{f_{avg}} = 2 \frac{f_h - f_l}{f_h + f_l} \approx \frac{W}{f_c} \geq 0.25 \quad (2.1)$$

Where f_h is denoted as the upper edge frequency, f_l is the lower edge frequency, f_{avg} is the average frequency, and W is the absolute bandwidth of interested frequency. Table

2.1 shows a comparison among the categories of signal with respect to relative bandwidth.

Table 2.1 A Comparison among Standards with Respect to Relative Bandwidth.

Standard	Relative bandwidth
Narrow band	≤ 0.01
Wideband	$0.01 \leq \dots \leq 0.25$
Ultra-Wideband, UWB	≥ 0.25

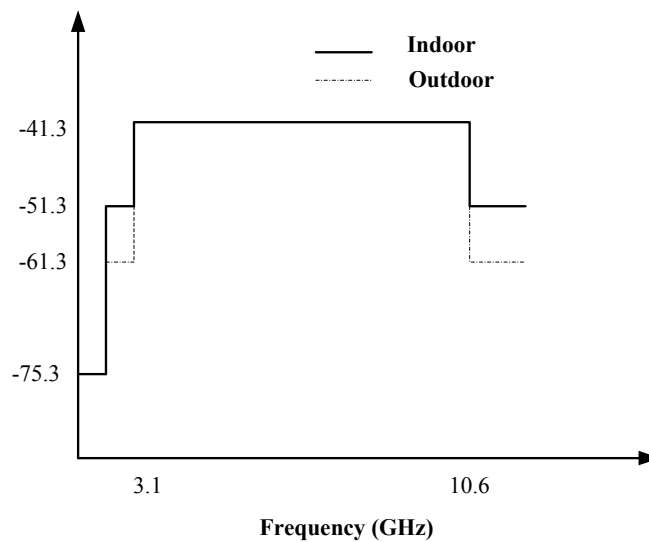


Figure 2.1 Acceptable power levels for indoor and outdoor emissions.

The FCC spectral mask (the operating restrictions for UWB in the United States) specifies 7.5 GHz of usable spectrum bandwidth between 3.1 GHz and 10.6 GHz for communications devices. The FCC also protects existing users operating within this spectrum by limiting the UWB’s signal transmit power. The UWB devices’ power spectral density levels are limited to - 41.3 dBm/MHz. The primary difference between indoor and outdoor operations is the higher degree of attenuation required for the out-of-band region for outdoor operations. This further protects GPS (Global Positioning System) receivers, centered at 1.6 GHz.

2.2 UWB Standards

Currently there are two proposals namely Multi-band Orthogonal Frequency Division Multiplexing (MB-OFDM) and Direct Sequence Code Division Multiple Access (DS-CDMA) for UWB applications. However there is still no a single standard particularly for UWB applications. MB-OFDM proposal is led by Intel while DS-CDMA by FREESCALE. However, MB-OFDM [Batra, 2003] has gained more support compare to DS-CDMA but it is still not enough to finalize MB-OFDM as the standard for UWB applications.

2.3 Direct Sequence Code Division Multiple Access (DS-CDMA)

DS-CDMA (Direct Sequence Code Division Multiple Access) uses traditional impulse UWB with M-ary Bi-Orthogonal Keying and a CDMA encoding scheme for multiplexing and channelization to exploit the entire UWB spectrum. DS-CDMA is a powerful multiple access technique in the presence of narrow band interferer. However, the ability to overcome interference lies in advanced receiver architecture. Besides, it is also bandwidth efficient for multi user wireless.

DS-CDMA transmitter is a low cost, low power application. It incorporates with various levels of Digital-Signal-Processor (DSP) to increase the performance, and thus increase the cost and power accordingly in a transmitter. Hence, low power consumption and compact size requirements limit the processing power available for DS-CDMA receivers [Ryan, 2005].

2.4 MB-OFDM

OFDM is another spread spectrum technique that distributes data over a large number of carriers that are spaced apart at precise frequencies. Within the transmitter for OFDM the data stream to be sent is divided into the sub-carriers. In OFDM, the receiver must have timing, frequency and sampling clock synchronization with the transmitter to ensure the correct data is received [Ryan, 2005].

As for MB-OFDM (MBOA) Proposal (September 2004), it indicates that the

UWB system would provide data capabilities of 110 Mbps, 200 Mbps and 480 Mbps. This UWB system applies MB-OFDM approach. It divides the total bandwidth into 13 sub-bands consists of 528 MHz bandwidth and apply frequency hopping technique. Therefore, this proposal need not use the entire bandwidth for communication. The band plan for MB-OFDM is shown in Figure 2.2. There are 4 band groups with three frequency bands and one band group with 2 frequency bands. System that operates in the lowest three frequency bands are to be known as Mode 1 operations.

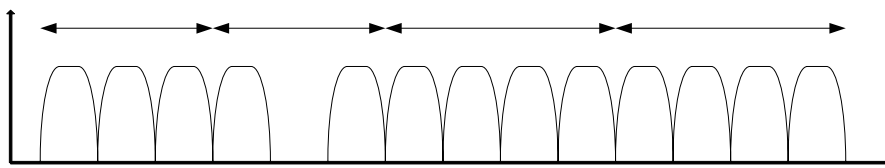


Figure 2.2 Band plan for MB-OFDM.

There are some advantages [Ryan, 2005] obtained from MBOA proposals. First, it is a simpler integration to different worldwide regulatory environments. Besides, minimum interference is achieved in multi-path environment. This aids in reducing the loss of data during transmitting and receiving in a transceiver. Moreover, MBOA is a peaceful coexistence with flexible spectral coverage, which is applicable to UWB technology.

2.5 UWB Advantages

UWB technology offers many advantages over narrowband technology where certain applications are involved. One of the major advantages of UWB is the improved channel capacity. The channel is the RF spectrum within, which the information is transferred and the capacity of the channel is given by Shannon's capacity theorem. Shannon's capacity theorem shows capacity increasing as a function of BW (bandwidth) faster than as a function of SNR (signal to noise ratio).

$$C = BW \log_2(1 + SNR) \quad (2.2)$$

where C is the Channel Capacity (bit/s), BW is the channel bandwidth in Hertz and SNR is signal to the noise ratio.

Shannon's equation shows that increasing channel capacity requires linear increases in bandwidth while similar channel capacity increases would require exponential increases in power. Hence, UWB technology is capable of transmitting very high data rates using very low power.

Another advantage of UWB is simpler architecture compare to narrowband radio. Narrowband radio uses high quality oscillator and tuned circuits to modulate and de-modulate information. UWB transmitter, however, can directly modulate a baseband signal eliminating components and reducing requirements on tuned circuitry. UWB, receiver, on the other hand, may require architectures that are more complex and may take advantage of digital signal processing techniques. Reducing the need for high quality passive based circuits and implementing sophisticated digital processing technique through integration with the same cost CMOS processes used for microprocessors will enable radio solutions that scale in cost/performance with digital technology.

The third advantage of UWB is its robustness to fading and interference. Fading effect is a reduction in the amplitude of the original signal when random multipath reflections are received out of phase. UWB with wideband nature reduces the effect of random time varying amplitude fluctuations. Short pulses will prevent the destructive interference from multipath that cause fade margin in link budgets. However, multipath components can be resolved and used to improve signal reception.

CHAPTER 3

POWER AMPLIFIER

Power amplifier (PA) is a last block used in a transmitter, and mostly recognized as power hungry stage. PA is used to boost up the power level of a signal in order to transmit in a required distance over a wireless medium.

In this chapter, an overview of power amplifier (PA) is presented. The understanding of specifications of PA is also included in this chapter. These include operating frequency, output power, efficiency, power gain, gain flatness, 1 dB compression point, and existing classes of power amplifier.

3.1 Overview of Power Amplifier (PA)

Power amplifier is a key block in a RF transmitter. It is usually the last block in the transmitter, which is the most power hungry stage. Power amplifier boosts the power level of a signal to a certain power level so that the signal can propagate the required distance over a wireless medium. Typically, a power amplifier feeds signal from up-conversion mixer and amplifies the signal to a certain power level, which is determined by the application it is designed for. The output power is delivered to an antenna, which acts like a 50 Ω load.

In UWB system, the power level from the UWB transmitter should be small enough to prevent interference with the existing communication systems. FCC has specified the output level for UWB system to be less than -41.25 dBm/ MHz, which is approximately five times lower than power level of Bluetooth technology. As a result, UWB systems need not require large transistors for power amplifier circuit. This indirectly reduces the power consumption of the transmitter. However, the challenge of UWB power amplifier is to achieve high gain and good impedance matching over the entire frequency range.

3.2 Specification of UWB PA

A few important terms and specification of a power amplifier are discussed in this section. They are operating frequency, output power, efficiency, power gain, gain flatness, 1 dB compression point, and existing classes of power amplifier.

3.2.1 Operating Frequency

In a typical narrowband application, the power amplifier is designed for a particular frequency. However, the frequency range for UWB system is in the order of several GHz. There are two proposals namely MB-OFDM and DS-SS which have options to cover the lower band of UWB spectrum which is from 3.1 GHz to 5 GHz. Therefore, in this power amplifier design, it targets 3.1 GHz to 5 GHz.

3.2.2 Output Power

For a 2 GHz bandwidth and average power level less than -41.25 dBm / MHz, UWB transmitter required to deliver -8 dBm or 160 μ W output power level [Jose, 2004].

3.2.3 Efficiency

Efficiency is a measure of how many percent of the supply power is translated to output power. It is given as

$$\eta = \frac{\text{Power delivered to the load}}{\text{Power drawn from the source}} \quad (3.1)$$

Ideally, we want efficiency of 100% which means the power amplifier only consume the power need to be transmitted. Practically, 100% of efficiency is impossible to achieve. The best way to improve power efficiency is to use technique which the voltage and current does not occurs simultaneously. Switching amplifier is an example that applies this technique and it can achieve efficiency up to 80%. However, the efficiency trade off with linearity. Therefore, both of them need to be compromised for better efficiency.

To compare power amplifiers with different input power levels, PAE namely

power added efficiency is used.

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} \quad (3.2)$$

where P_{out} is the output power of power amplifier, P_{in} is the input power provided, and P_{dc} is the power consumption of power amplifier.

However, in UWB applications, the output power level is very low. Therefore, PAE is not used as a performance metric for UWB power amplifier. Instead, high gain and low power are the appropriate metric for UWB power amplifier.

3.2.4 Power gain

Power gain is the ratio of output power delivered to the load to the input power available from the source. The power gain will equal to the voltage gain of the amplifier if the input and output impedance are the same.

3.2.5 Gain Flatness

Gain flatness is a measured of uniformity of the gain across a wide frequency range of interest. It is commonly used for wideband systems that can influence pulse distortion in impulse-based UWB. The gain is desired to be in a tolerance of ± 0.5 dB.

3.2.6 1-dB Compression Point

1-dB compression is the input power at which the linear gain of the amplifier has compressed by 1 dB, which is illustrated in Figure 3.1. This metric is used to measure linearity of a power amplifier.

For constant envelope modulation scheme (FSK), linearity is not so important compare to non-constant envelope modulation scheme (CDMA). It is because FSK modulates the signal into the phase of the carrier signal oppose to CDMA, which the amplitude of the signal also carry information. For MB-OFDM, linearity is not as important compare to impulse-based UWB.

3.2.7 Power Consumption

In typical transmitter, power amplifier consumes most amount of the power

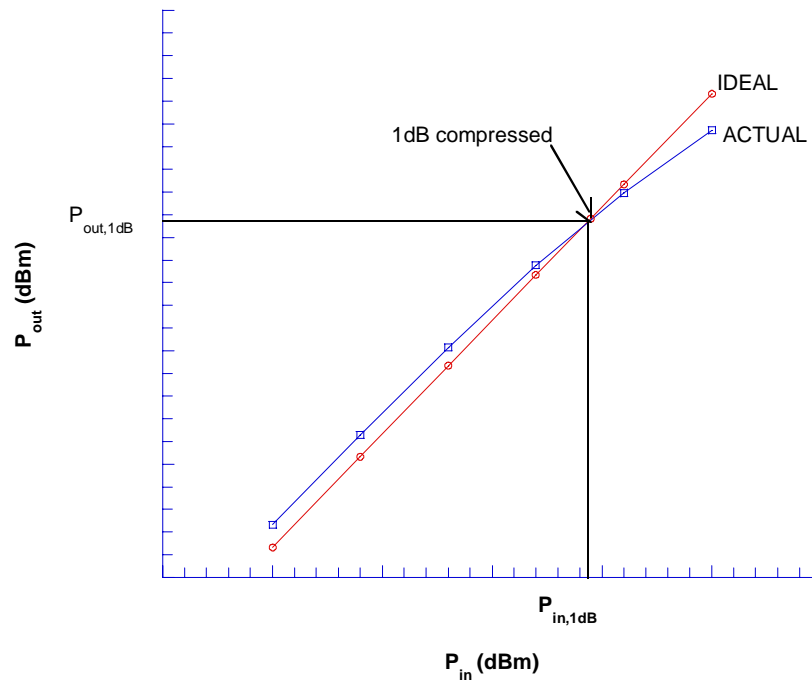


Figure 3.1 1 dB compression point.

from a supply or battery. In portable devices, power consumption must be kept as low as possible so that it has longer battery life. Since the output power level for UWB is very low, the power consumption can be kept as low as possible, which can be achieved by using smaller transistor.

3.3 Classes of PA

Two major kinds of power amplifier are widely used. They are linear amplifier and switching amplifier. In linear amplifier, its output is linearly proportional to its input. Class A, B [Asbeck and Fallesen, 2000] and C are some common types of linear amplifier [Narayanaswami, 1998]. The average output impedance is relatively high. As for switching amplifier like class E and F, the amplifier is driven with large amplitude of signal turning the transistor ON and OFF.

3.4 Loadline

Linear amplifier operates at constant gain is based on load-line theory illustrated in Figure 3.2 (a). The maximum power that can be delivered to the load depends on the maximum current of the transistor and supply voltage. When the transistor load is a large inductor, the maximum voltage swing possible at the drain is 2 times the supply voltage. The loadline is plotted from

$$R_{opt} = \frac{2V_{max}}{I_{max}} \quad (3.3)$$

where the optimum resistance of a load, R_{opt} is obtained by the relationship of maximum power supply, V_{max} to a load, which is usually equal to V_{DD} while $I_{max}=2V_{DD}/R_L$, indicating the maximum load current obtained.

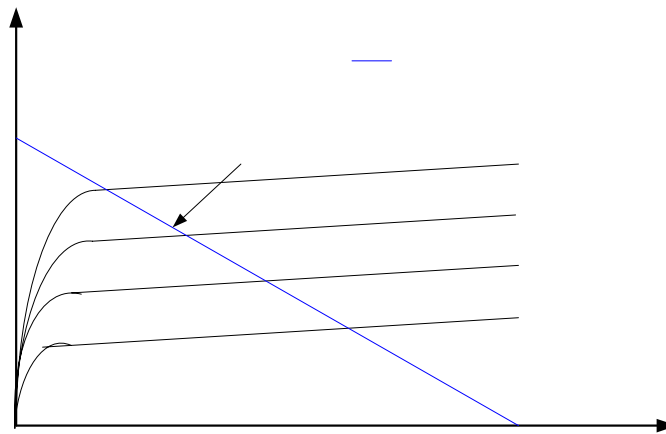


Figure 3.2 (a) Loadline [Cripps, 2000].

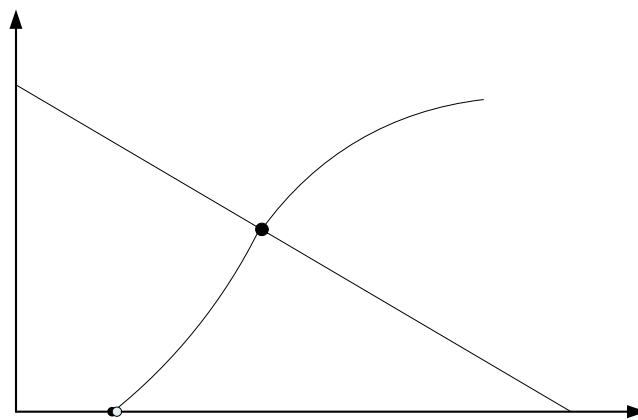


Figure 3.2(b) Q-point of linear power amplifier.

The summary of power amplifier classes is shown in Table 3.1.

Table 3.1: Summary of Power Amplifier's Classes [Cripps, 2000].

Class	Modes	Conduction Angle (%)	Output Power	Maximum Efficiency (%)	Gain	Linearity
A	Current Source	100	Moderate	25	Large	Good
B		50	Moderate	78.5	Moderate	Moderate
C		<50	Small	100	Small	Poor
D	Switch	50	Large	100	Small	Poor
E		50	Large	100	Small	Poor
F		50	Large	100	Small	Poor

CHAPTER 4

POWER AMPLIFIER DESIGN FOR MB-OFDM

Multi-Band Orthogonal Division Multiplexing (MB-OFDM) technique was proposed by a group of companies which include Intel, Texas Instrument etc. However, only mode 1 (3.16 GHz to 4.75 GHz) of UWB frequencies is being considered for the initial transceiver deployment. The remaining of the frequencies is reserved for future use.

In this chapter, the power amplifier design for MB-OFDM is presented. The specifications of the power amplifier design are shown at the beginning of this chapter. It followed by the design considerations as well as architecture and topology as the overall schematic approach.

4.1 Design Specifications

The power amplifier design specifications for UWB MB-OFDM application is shown in Table 4.1. The specification of the power amplifier is obtained from [Jose, 2004], which has been calculated from the link budget of their UWB transceiver design.

When compared to typical power amplifier design, the major differences between UWB power amplifier and typical power amplifier are operation range of frequency and output power level. UWB power amplifier has approximately 2 GHz bandwidth while typical power amplifier has few MHz of bandwidth. Compare to typical power amplifier, which has output level greater than 25 dBm, UWB power amplifier only requires output power level less than 0 dBm which is very low. Therefore, with such low output power, UWB power amplifier's DC power consumption can be kept lower than 40 mW opposed to typical power amplifier with higher output power level, which may need hundreds of mili-Watts.

The major challenge of [Aiello, 2003] UWB power amplifier is the wideband input matching (given by S_{11}) and output matching (given by S_{22}) in the desired range of frequency while delivering output power level greater than -8 dBm with a gain greater

than 15 dB with in band gain flatness within ± 1 dB.

Table 4.1 Specifications of UWB MB-OFDM Power Amplifier Design [Jose, 2004].

Categories	Specifications
Supply Voltage	1.8 V
Frequency	3.168 - 4.75 GHz
Input, P_{1dB}	-22 dBm
Output, P_{1dB}	0.0 dBm
Maximum Output	> -8 dBm
Gain Flatness	± 1 dB
Power Gain	> 15 dB
Voltage Gain	> 15 dB
Efficiency	-
Input Reflection Coefficient, S_{11}	< -10 dB
Isolation, S_{12}	< -30 dB
Output Reflection Coefficient, S_{22}	< -10 dB
DC Power Consumption	< 40 mW
Input Impedance (Differential)	100 Ω
Output Impedance	50 Ω

4.2 Power Amplifier Architecture

As up conversion mixer is the preceding stage of the power amplifier in a transceiver system, power amplifier feeds the output of the mixer and amplifies the signal before sending to the antenna for propagation. Since differential topology such as Gilbert Cell is commonly used as the architecture of an up conversion mixer to take advantage of the differential topology such as noise immunity and isolation, a differential to single-ended conversion circuitry is needed to convert the signal from differential to single-ended before amplification. The block diagram of the overall design is illustrated in Figure 4.1.

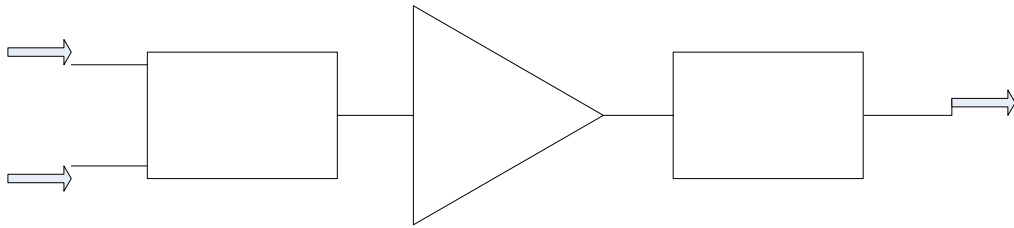


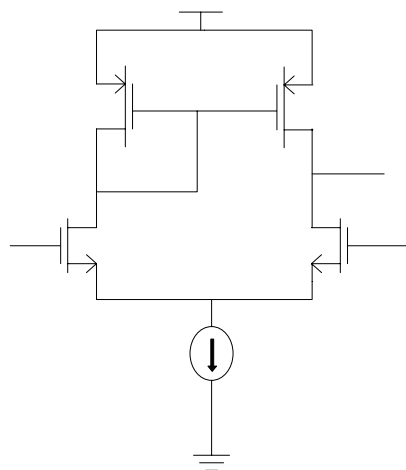
Figure 4.1 Block diagram of overall schematic.

4.3 Differential-to-single-ended Converter [Jose, 2004]

Differential amplifier with active current mirror load [Razavi, 2001] topology is used as it is a common topology for differential to single-ended conversion. The architecture of the differential-to-single-ended is shown in Figure 4.2.

$$\frac{V_{out}}{V_{in}} = g_{m2,3} (r_{o2,3} // r_{o1,4}) \quad (4.1)$$

where g_{m1} and g_{m0} is the transconductance of M_1 and M_0 , respectively, r_{o1} , r_{o2} , r_{o3} and r_{o4} are the output resistance corresponding to M_1 , M_2 , M_3 and M_4 , respectively.



From mixer

Figure 4.2 Differential-to-single-ended converter [Razavi, 2001].

Although this architecture can achieve very high gain, it is used here as unity gain

converter. Equation (4.1) gives the gain of the converter.

4.4 Wideband Input Matching Technique

Typical narrowband applications use LC based networks [Ismail and Abidi, 2004] to achieve matching at a particular frequency by exploiting the fact that the impedance of the network is purely resistive at the resonant frequency. In fact, this concept can be extended for wideband matching conditions [Ismail and Abidi, 2004]. This technique is the combination of source degeneration common source amplifier with n-th order Chebyshev filter. This technique can be illustrated in Figure 4.3.

The input impedance looking into the gate is given as

$$Z_{in}(s) = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \quad (4.2)$$

where L_s is the source degeneration inductance, C_{gs} and g_m are the gate-to-source capacitance and transconductance of transistor, respectively.

From (4.2), it shows that transistor with transconductance, g_m can provide resistance

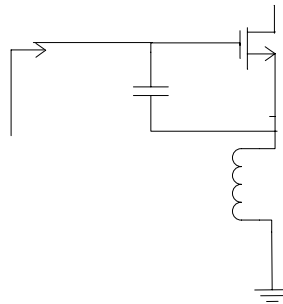


Figure 4.3 Common source amplifier with source degeneration.

of $\frac{g_m L_s}{C_{gs}}$ (typically 50 Ω) at resonant frequency which is determined by L_s and C_{gs} value.

The source degeneration common source amplifier is used to provide 50 Ω at the gate of the transistor at mid-band frequency. The generated resistance will act as the

load of the Chebyshev bandpass filter, which is tied to the gate of the transistor. However, such technique requires LC networks that will eventually consume significant die area.

Another technique is the resistive shunt termination topology [Lee, 2002], which can be shown in Figure 4.4

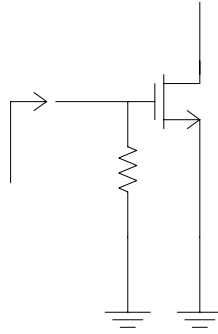


Figure 4.4 Resistive shunt termination topology [Lee, 2002].

This technique is the simplest and primitive way of providing broadband matching by just connecting a resistor of $50\ \Omega$ shunting the gate of the transistor. However, it is not an efficient technique as a significant power is wasted through the resistor. This technique also introduces a lot of noise, which its noise figure is given by

$$NF = 2 + \frac{P_{na,i}}{KTBG_a} \quad (4.3)$$

where G_a is power gain of the amplifier, K is Boltzman constant (1.38×10^{-23} J/K), B is the bandwidth, T is typical temperature in unit Kelvin and $P_{na,i}$ is the internal noise power. Since noise figure is not that critical for power amplifier, resistive shunt termination technique is chosen as the input matching topology.

4.5 Output Matching Technique

T-type matching circuit, which is illustrated in Figure 4.5, has been chosen as the output matching circuit of the power amplifier as it is widely used as input, inter-stage, and output matching circuits in high power amplifier. It can also incorporate active device lead and bond wire inductances within matching circuit. Furthermore, it

can provide significant level of harmonic suppression.

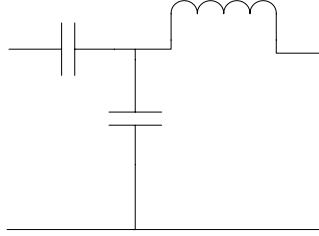


Figure 4.5 T-type matching circuit.

The t-type matching circuit equation is shown as [Grebennikov, 2004]

$$\begin{aligned}
 \omega C_1 &= 1/(R_1 Q_1) \\
 \omega L_o &= R_2 Q_2 \\
 \omega C_2 &= (Q_2 - Q_1)/[R_2(1 + Q_2^2)] \\
 Q_1 &= \sqrt{\frac{R_2}{R_1}(1 + Q_2^2)} - 1 \\
 Q_2^2 &> \frac{R_1}{R_2} - 1
 \end{aligned} \tag{4.4}$$

where ω is the circuit's operating frequency in radian/second, C_1 and C_2 are the capacitances of the capacitors, R_1 is the equivalent impedance to be matched to R_2 , which is the load impedance and $Q_{1,2}$ is the quality factor equal for series and parallel circuits.

4.6 Wideband Gain and Flatness

There are several ways to obtain wideband gain. However, the simplest and cheapest way is to connect a very large inductor to the drain of the transistor to resonate out the effective drain capacitance. To understand why and how this inductor should give bandwidth extension, let us consider a common source amplifier with resistive load shown in Figure 4.6

We know that the gain of the amplifier at low frequency is given by $g_m R$ as the

effective drain capacitance act as an open circuit at low frequency. When frequency increases, the impedance looking into the drain of the transistor decreases as the impedance of the capacitor dismisses (introduce pole). Thus, the gain of the amplifier eventually falls off as the capacitor shunting the current to ground. Therefore, inductor which has impedance that increases with frequency (introduce zero) is added to offset

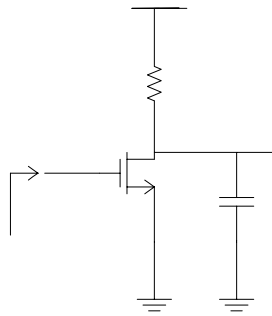


Figure 4.6 Common source amplifier with resistive load.

the decreasing impedance of the capacitance, leaving roughly more constant impedance over a broader frequency range than that of the original RC network. This topology is called inductive shunt peaking, which is shown in Figure 4.7. The output impedance looking into the drain of the transistor is given as

$$Z(s) = (sL + R) // \frac{1}{sC} \quad (4.5)$$

$$Z(s) = \frac{R[s(\omega L/R)^2 + 1]}{s^2 LC + sRC + 1}$$

Note that with constant impedance over a broad frequency range inferred that the gain of the amplifier will also be constant or flat as the transconductance, g_m of the transistor is constant with frequency and is shown as

$$g_m = k_n C_{ox} (V_{gs} - V_{th}) \quad (4.6)$$

The effect of the added inductor can also be explained in time domain by considering the step response. The inductor delays the current flow through the branch containing the resistor, thus more current is available to charge up the capacitor. As a result, the rise time is reduced therefore the bandwidth is increases. To the extent of