DESIGN OF DIGITAL IMAGING SYSTEM USING DIGITAL SIGNAL PROCESSOR (DSP)

Oleh

YEOH SIEW LEE

Disertasi ini dikemukakan kepada

UNIVERSITI SAINS MALAYSIA

Sebagai memenuhi sebahagian daripada syarat keperluan

untuk ijazah dengan kepujian

SARJANA MUDA KEJURUTERAAN (KEJURUTERAAN ELEKTRONIK)

Pusat Pengajian Kejuruteraan

Elektrik Dan Elektronik

Universiti Sains Malaysia **Mei 2006**

ABSTRACT

DESIGN OF DIGITAL IMAGING SYSTEM USING DIGITAL SIGNAL PROCESSOR (DSP)

The objective of this project is to present the design and analysis of a camera module system which this system will be able to capture still images from camera, process these digital images and then display through the computer screen. The digital imaging microcontroller system using digital signal processor (DSP) has been designed and developed. This microcontroller can be distributed into four parts. The main part was contributed by the DSP chipset which act as a centre processing unit (CPU) to control all the processing of images data flow. The second part will be the voltage regulator part to step down the 5V to 3.3V and 1.8V for DSP source power purposes and also to step down to 2.8V for the camera source power purposes. The third part make up of all the logic devices as to store and process the images data. The final part will be treated as transmit and receive control system for the serial communication in between microcontroller system and computer. In addition, this project also analyzes the application of digital image processing using digital signal processor starter kit (DSK). Implementation of the design and analysis of this project will be reported in details. Finally, further analysis and the real time data to image conversion form cannot be executed but the results regarding the processing of the digital image data during the analysis will be discussed in this project.

ABSTRAK

REKABENTUK SISTEM IMEJ BERBENTUK DIGIT DENGAN PEMPROSESAN ISYARAT DIGIT

Objektif bagi projek ini adalah untuk mempersembahkan rekabentuk dan analisis bagi suatu sistem modul kamera yang berupaya untuk menangkap gambar statik, memproses data gambar dalam bentuk digit dan kemudian data tersebut akan dipaparkan pada skrin komputer. Dengan penyelidikan sedemikian, sistem mikropengawal pemproses isyarat digit (*Digital Signal Processor*, DSP) telah direkabentuk. Sistem mikropengawal terdiri daripada empat bahagian. Bahagian pertama terdiri daripada cip DSP yang berperanan sebagai unit pusat pemprosesan (*Centre Processing Unit*, CPU) untuk mengawal semua aliran isyarat supaya isyarat tersebut diproses. Bahagian kedua merupakan penyelarasan voltan 5V kepada 3.3V dan 1.8V untuk kegunaan bekalan kuasa cip DSP serta 2.8V untuk kegunaan bekalan kuasa ADCM CMOS kamera. Bahagian ketiga terdiri daripada semua cip-cip logic yang tujuannya adalah untuk penyimpanan dan peruntukkan data gambar manakala bahagian terakhir merupakan sistem kawalan penghantaran dan penerimaan data gambar secara sesiri dengan komputer. Di samping itu, kajian untuk mengaplikasikan teknik imej pemprosesan bagi *digital signal stater kit* (DSK) juga diselidiki. Dalam projek ini, segala rekabentuk dan kajian pembangunan sistem mikropengawal DSP TMS320VC33 dan penyelidikan sistem DSK TMS320VC5510 akan dilaporkan. Walaubagaimanapun, analisa secara mendalam bagi data gambar tidak dapat dijalankan dan hanya keputusan yang menunjukkan isyarat data imej dan imej selepas diproses dalam sistem DSP dan DSK akan dibincangkan.

ACKNOWLEDGEMENT

I would like to express a thousand of appreciation to everyone who had made my undergraduate studies succeeded. Without them, my studies will never succeed. Also, I gained a lot of experiences from them, not only in academic but also some good experience that a student will never learned directly from their study.

Our deputy dean, Professor Madya Dr. Mohd Zaid Abdullah, is the first person that I wish to express my special appreciation for being my respectable supervisor. Under his guidance and help, a lot of information that I could not understand previously is now become certain. After his guidance and suggestion, I am able to solve many problems while doing my design testing. Besides, Dr. Zaid always helping me and counsel me when I felt tensed and depressed. Without his guidance, encouragement and support, I will not be able to complete this project.

Second, I would like to express my deepest gratitude to my second examiner Dr. Shahrel A.Suandi. With his examination of my thesis, many of the mistakes have been corrected.

My appreciation also goes to Professor Farid Ghani for providing me some useful information related to digital signal processing (DSP) method.

Special thanks to Pn. Zaini who shared her knowledge to me with patience. Thanks for her proper explanation on everything about the system microcontroller 8051 and also her dedication of finding the related information of digital signal processing (DSP) method for me, my design process become much easier and smoother with her explanation and guidance.

Besides, my special thanks also go to Mr. William Koay and Mr. Halim for guiding me on my project and a lot of design and testing problems have been solved. Throughout my project, Mr. William Koay gave his full encouragement and helped me to look for more information in library and internet. With his suggestions, I found out a lot of useful information from the sources suggested by him. Mr. Halim shared a lot of knowledge in programming to me with patience and benefit me a lots to complete my program.

Special thanks to Mr. Nor Rizuan Mat Noor for sharing a lots of knowledge on how to operate the digital signal starter kit (DSK) with patience. He also shared with me about his experiences and difficulties when deal with the DSK. My project would not be succeeded without his helped and guidance.

I would also like to express my sincere gratitude to technicians Mr. Amir Hamzah (DSP Lab), Mr. Nor Azhar Zabidin (Mechatronic Lab), Mr. Amir bin Hamid (Mechatronic Lab), En. Naim (Electronic Lab) and Mr. Mohd Nurul Azrol (PCB Lab). They were all willing to share their time to assist and help me in my task. I appreciated their efforts of helping me fabricated the printed circuit board (PCB), searched related components for me and taught me on how to operate some of the equipments in the lab.

When I am facing any difficulties of using the digital signal processing (DSP) chipset, Mr. Chai Yu Leong is always there to help me. He taught me on how to implement the knowledge from microcontroller 8051 to digital signal processing effectively especially writing the assembly languages program.

Last but not least, I would like to thank everyone that encourage and accompany me gone through the whole design and testing process, especially the course mates where we do a lot of soldering and testing in the lab together.

CONTENT

LIST OF TABLES PAGE

LIST OF FIGURES PAGE

CHAPTER 1 – INTRODUCTION

1.1 Background of Digital Image Processing

In the broadcast sense, image processing is any form of information processing for which both the input and output are images, such as photographs in still images form or frames of video in movement form.

Most image processing techniques involve treating the image as a two-dimensional function, f(x,y), where x and y are special coordinates, and the amplitude of f function at any pair of coordinates (x,y) is called the intensity or gray level of the image at that point. The term gray level is used often to refer to the intensity of monochrome images. Color images are formed by a combination of individual 2-D images. In the RGB color system, a color image consists of three (red, green, and blue) individual component images. For this reason, many of the standard signal processing techniques developed for monochrome images can be extended to color images by processing the three component images individually.

For the function f (x,y) in the image processing field, when x,y and the amplitude values of f are all finite, discrete quantities, we call the image a digital image. The field of digital image processing refers to processing digital images by means of a digital computer. Note that a digital image is composed of a finite number of elements, each of which has a particular location and value. These elements are referred to as picture elements, image elements, pels, and pixels. Pixel is the term most widely used to denote the elements of a digital image [1].

Few decades ago, image processing was done largely in the analog domain, chiefly by optical devices. These optical methods are still essential to applications such as holography because they are inherently parallel. However, due to the significant increase in computer speed, these techniques are increasingly being replaced by digital image processing methods.

Digital image processing techniques are generally more versatile, reliable, and accurate. They have the additional benefit of being easier to implement than their analog counterparts. Specialized hardware is still used for digital image processing, computer architectures based on pipelining have been the most commercially successful. There are also many massively parallel architectures that have been developed for the purpose. Today, hardware solutions are commonly used in video processing systems. However, commercial image processing tasks are more commonly done by software running on conventional personal computers [2].

There are so many applications field using image processing technique nowadays such as photography and printing, satellite image processing, medical image processing, microscope image processing, car barrier detection as well as face or feature detection and identification and so on. Thus, the recapitulation for this project is mainly based on commercial digital image processing techniques applied in digital image processes.

1.2 Objective Of The Project

With the fast computers and signal processors available in this century, this digital image processing project is the most common form of image processing, it involves the common CMOS camera, computer and commercial marketable Digital Signal Processor (DSP). These devices are generally used because they are not only the most versatile method, but also the cheapest.

Digital image processing enables the reversible, virtually noise-free modification of an image in the form of a matrix of integers instead of the classical darkroom manipulations or filtration of time-dependent voltages necessary for analog images and video signals. Besides, it also allows the use of much more complex algorithms for image processing, and hence can offer both more sophisticated performance at simple tasks, and the implementation of methods which would be impossible by analog means. Consequently, this project tends to design and develop an embedded system which can communicate with a CMOS camera based on the digital image processing techniques. This embedded system must be able to control the whole activities of the camera such as data image acquisition and digital processing of the data images. In addition to that, this digital image processing based project needed to be accomplished by special software program that manipulate the images in many ways.

Although the further image processing analysis could not be implemented in this project, but the techniques and studies of this project can be found as a reference or guideline for the next researcher.

Error! Bookmark not defined.

1.3 Scope Of Project

In this project, the scopes of project consist of some implementation as stated below:

1.3.1 Design an embedded hardware system to communicate with a CMOS camera.

1.3.2 Digital images data acquisition and processing using the embedded hardware system.

1.3.3 Software program written to manipulate the signal in embedded hardware system.

1.3.4 Develop the application of an available hardware platform using digital image processing techniques.

1.3.5 Produce the overall documentation based on the analysis methods and results of the image processing project as shown in figure 1.1.

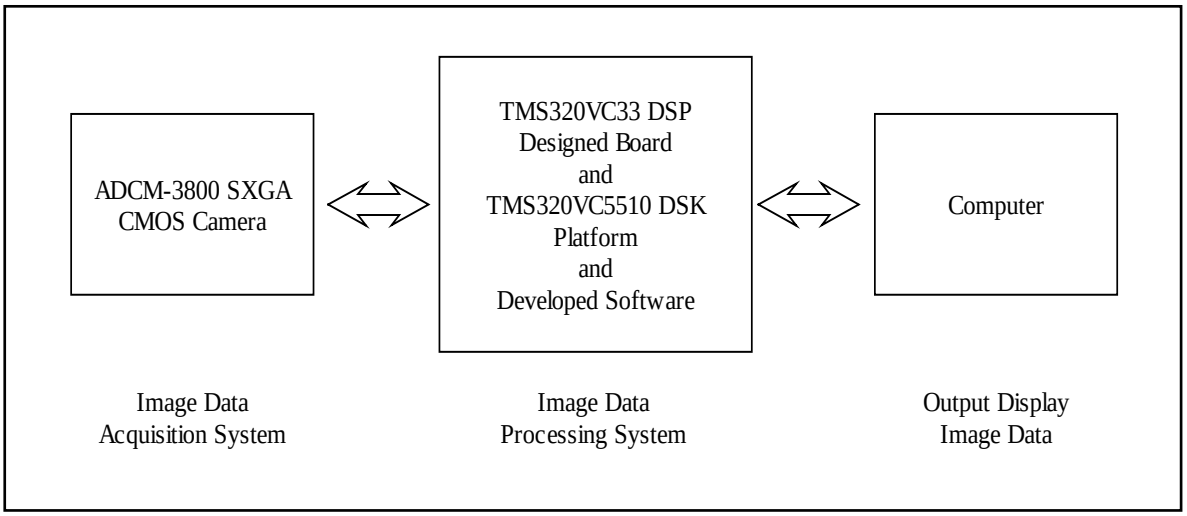


Figure 1.1 : General block diagram of image processing project

1.4 Thesis Literature

In Chapter 1, the introduction of this thesis is discussed. This chapter will discuss the history background and potential for image processing field and also the overview research of this project.

In Chapter 2, the topology of ADCM-3800 SXGA CMOS camera and digital signal processor (DSP) system are discussed. This chapter will discuss the building of a complete image processing camera module system and also the operation of the camera. Then, the discussion will be proceeding into the study of the digital signal processor (DSP) system as well as the functionality of the DSP.

In Chapter 3, the details about the usage of related components, design techniques for TMS320VC33 digital signal processor (DSP) and also the developed software to manipulate signals in the designated image processing embedded hardware are discussed.

In Chapter 4, the application on digital image processing using TMS320VC5510 digital signal starter kit (DSK) is discussed. All the image processing procedures and techniques used to apply in the DSK will be discussed further in this chapter.

In Chapter 5, the methods used to test and analyze the designated hardware and software system is discussed. All the results gained from the experiments will be shown in this chapter.

In Chapter 6, the discussion and conclusion for the overall analysis and experiments that have done in this project will be included. Some future improvements and techniques are also discussed in this chapter.

CHAPTER 2 – TOPOLOGY OF ADCM-3800 SXGA CMOS CAMERA AND DIGITAL SIGNAL PROCESSOR (DSP) SYSTEM

In general, the design of digital image processing using digital signal processor (DSP) is divided into two main module, which are ADCM-3800 CMOS camera system (module 1) and digital signal processor (DSP) TMS320VC33 system (module 2).

System module 1 is operated to control and capture the still images from ADCM 3800 CMOS camera in digital form, the digital still images data is then stored in RAM 6264. System module 2 is used to process the digital still images data from RAM 6264 and then display the images data to PC using DSP TMS320VC33 microcontroller. This chapter will focus on the main core portion of the module 1 and 2.

2.1 Study of CMOS Camera

CCD sensors rely on specialized fabrication that requires dedicated and it is costly in manufacturing processes. In contrast, CMOS image sensors can be made at standard manufacturing facilities that produce 90% of all semiconductor chips, from powerful microprocessors to RAM and ROM memory chips. This standardization results in economies of scale and leads to ongoing process-line improvements. CMOS processes, moreover, enable very large scale integration (VLSI), and this is used by some “active-pixel” architecture to incorporate all necessary camera functions onto one chip. Such integration creates a compact camera system that is more reliable and obviates the need for peripheral support chip packaging and assembly, further reducing cost.

In addition, to convert the photons to electrons and transferring them, the CMOS sensor might also perform image processing, edge detection, noise reduction, and conversion of analog to digital. The sensor and digital camera designers can make the various CMOS functions become programmable and providing a very flexible device. CMOS is designed with functional integration onto a single chip if compared with CCD. CMOS also reduces the number of external components needed. By using an integrated CMOS sensor, it allows the digital camera to devote less space to other chips, such as

digital signal processors (DSPs) and ADCs. In addition, CMOS devices consume less power than CCDs, thus thermal noise can be reduced.

For ADCM-3800 SXGA CMOS camera module contains an image sensor as the image acquisition unit and an image processor/image pipeline as the image processing unit.

2.1.1 Image Acquisition Unit

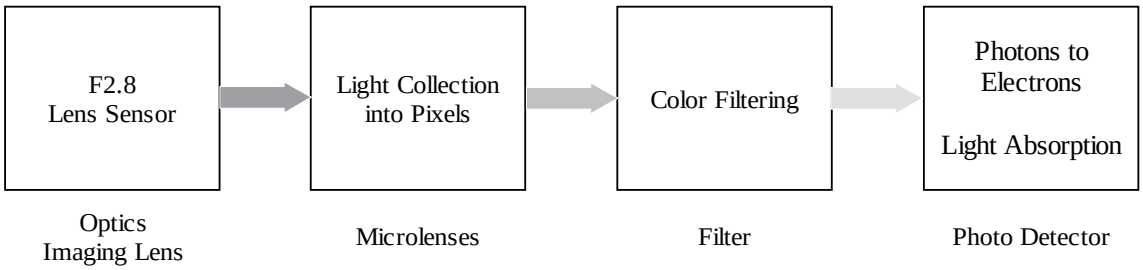


Figure 2.1 : Flow Diagram of image acquisition unit

Initially, the image acquisition unit of ADCM-3800 CMOS camera used a high quality F/2.8 triplet lens to capture image as input.

Then the image will go through a sensor, which consists of a 1280 x 1024 pixel array and can be windowed to any size between 1280 x 1024 and 24 x 24. The array can be mirrored in the horizontal and vertical directions. All image sensors are grayscale device that record the intensity of light from full black to white, with the appropriate intervening gray. To add colour to a digital camera image, a layer of colour filters is bonded to the silicon using a photolithography process to apply the colour dyes. Image sensors that have micro lenses will put the colour between the micro lens and the photo-detector. With scanners that use trilinear CCDs (three adjacent linear CCDs using different colors, typically red, green, and blue) or high-end digital cameras that use three area array image sensors, it's a very simple issue of coating each of the three sensors with a separate color. (Note that some multi-sensor digital cameras use combinations of colors in their filters, rather than the three separate primaries). But for single sensor device, colour filter arrays (CFAs) are used.

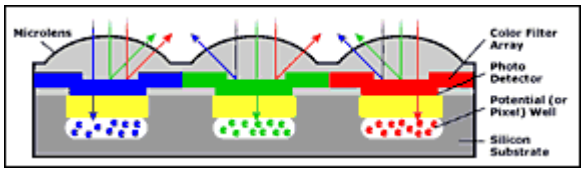


Figure 2.2 : Operation of micro lens and colour filtering process

CFAs assign a separate primary colour to each pixel by placing a filter of that colour over the pixel. As photons pass through the filter to reach the pixel, only wavelengths of that primary colour will pass through. All other wavelengths will be absorbed. Primary colours are a small set of colors identified by science as being the building blocks for all other colours. Therefore, in the RGB color model, combining varying amounts of red, green and blue will create all the other colours in the spectrum.

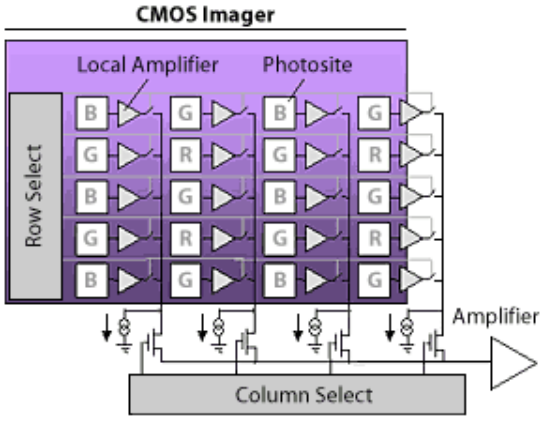


Figure 2.3 : Pixels and amplifier address in parallel circuitry

The charge readout from the CMOS sensor is done by using parallel circuitry, which allows the signal from single pixels or columns of pixels to be directly addressed. This direct random access ability allows a CMOS sensor to intelligently choose to readout select groups of pixel charges (rather than the entire sensor array). This is called window-of-interest or windowing readout.

In addition, to amplify within the pixel site, amplifying circuitry may be placed along the CMOS signal chain. This provides different, multiple gain stages throughout the sensor. Amplifiers can apply global gain to increase sensitivity in low light situations. Or selective gain can be applied to a specific colour to assist in white balance algorithms or artistic effects.

Then, the most popular CFA method, Bayer pattern was applied in this digital camera image sensor. Using a checkerboard pattern with alternating rows of filters, the Bayer pattern has twice as many green pixels as red or blue. And they are arranged in alternating rows, which are red wedged between green, and blue wedged between green. When a Bayer pattern sensor's charge is read out, the colours are recorded line by line. One line would be BGBGBG, followed by a line of GRGRGR and so forth. This is known as sequential RGB. [3]

2.1.2 Image Processing Unit

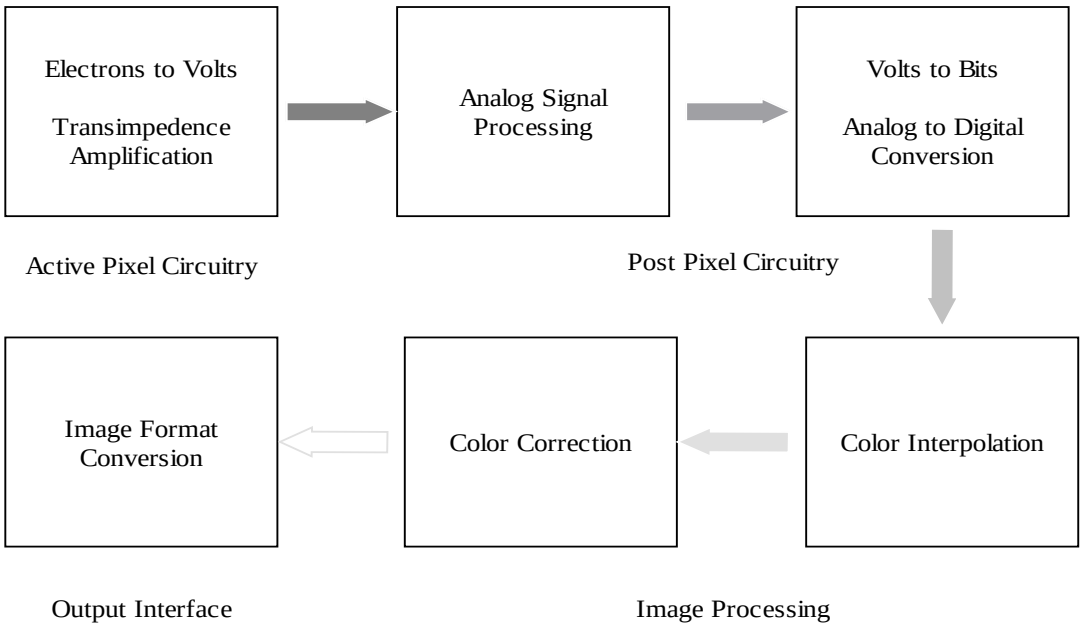
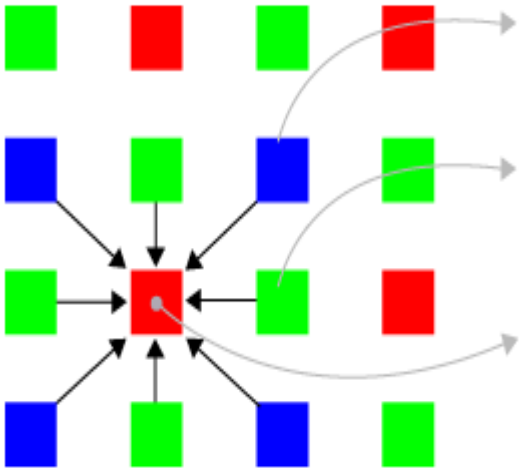


Figure 2.4 : Flow of image acquisition unit

During the post pixel circuitry process, the A/D converter converts the analog pixel voltages to 10 bits digital values and also an anti-vignetting process operate to correct for light fallout in the corners of the picture using variable gain.

After the A/D conversion process, colour interpolation is needed to averages out the colour values of appropriate neighboring pixels to guess, in effect, each pixel’s unknown (filtered out) colour data. For example, if one of the green pixels on a GRGR sequence line of the Bayer pattern is being read out, the process of colour interpolation guesses that pixel’s blue value by looking at the blue above and below it and taking the

average of those blues. For the red guess, the process looks at the reds to the left and right of the green pixel and averages those.



Have blue, need green and red

G= average of 4 neighboring greens

R= average of 4 neighboring reds

Have green, need blue and red

B= average of 2 neighboring blues

R= average of 2 neighboring reds

Have red, need green and blue

G= average of 4 neighboring greens

B= average of 4 neighboring blues

Figure 2.5 : Colour interpolation process

As long as the colour in the image changes slowly in the spatial dimension relative to the filter pattern, colour interpolation works well. However, for edges of objects, or fine details, colour may be interpolated incorrectly. Thus, the colour correction process will reduce the effects of the colour mismatch and improves the colour fidelity.

Finally, there will be an output interface port to handshake with external devices so that can convert the RGB output format to YCbCr or vice versa through programming.

2.2 Study of Digital Signal Processor (DSP)

Digital signal processing technique is concerned with the representation of signals in digital form, and with the processing of these signals with the different information that they carry. Although DSP began to flourish in the 1960's, some of the important and powerful processing techniques that are used today may be traced back to numerical algorithms that were proposed and studied centuries ago. Since the early 1970's, when the first DSP chips were introduced, the field of digital signal processing has evolved dramatically. With a rapid increase in the speed of DSP processors, along with a corresponding increase in their sophistication and computational power, digital signal processing has become an integral part of many commercial products and applications, and is becoming a common place term.

Digital Signal Processors (DSP) take real-world signals like voice, audio, video, temperature, pressure, or position that has been digitized and then mathematically manipulates them. A DSP is designed for performing mathematical functions like "add", "Subtract", "multiply" and "divide" very quickly.

Signals need to be processed to ensure that the information that they contained can be displayed, analyzed, or converted to other useful type of signal. In the real-world, analog products detect signals such as sound, light, temperature or pressure and manipulate them. Converters such as an Analog-to-Digital converter then take the real-world signal and turn it into the digital format of 1's and 0's. From here, the DSP takes over by capturing the digitized information and processing it. It then feeds the digitized information back for use in the real world. It does this in one of two ways, either digitally or in an analog format by going through a Digital-to-Analog converter. All of this occurs at very high speeds.

DSP's information can be used by computer to control things such as security, telephone, home theater systems, and video compression and even in image processing application. Signals may be compressed so that they can be transmitted quickly and more efficiently from one place to another (e.g. teleconferencing can transmit speech and video via telephone lines). Signals may also be enhanced or manipulated to improve their quality or provide information that is not sensed by humans (e.g. echo cancellation for cell phones or computer-enhanced medical images). Although real-world signals can

be processed in their analog form, but the processing of signals digitally will provides the advantages of high speed and accuracy.

A DSP can be used in a wide variety of applications due to DSP is programmable. One can create his own software or the software that provided by the related DSP support manufacturer to design a DSP solution for an application.

2.2.1 Building description of digital signal processor (DSP) TMS320VC33

Figure 2.6 : DSP TMS320VC33 PGE 150 SMD Chip

The TMS320VC33 DSP is a 32-bit, floating-point processor manufactured in 0.18-µm four-level-metal CMOS (Timeline) technology and is packaged in 144 pins low profile quad flat package (LQFP) (PGE Suffix). The TMS320VC33 is part of the TMS320C3x generation of DSPs from Texas Instruments. High level language support is easily implemented through a registered based architecture, large address space, powerful addressing modes, flexible instruction set, and well supported floating point arithmetic. A high performance and ease of use processor are the results of the features as shown below [2].

High-Performance Floating-Point Digital Signal Processor (DSP) features :

- 13-ns Instruction Cycle Time
- 150 Million Floating-Point Operations Per Second (MFLOPS)
- 75 Million Instructions Per Second (MIPS)
- 34K 32-Bit (1.13-Mbit) On-Chip Words of Dual-Access Static Random-Access Memory
- (SRAM) configured in 2 16K Plus 2 x1K Blocks to Improve Internal Performance
- x5 Phase-Locked Loop (PLL) Clock Generator
- 16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations
- Four Internally Decoded Page Strobes to Simplify Interface to I/O and Memory Devices
- Boot-Program Loader
- 32-Bit Instruction Word, 24-Bit Addresses
- Eight Extended-Precision Registers
- One Serial Port & two 32-Bit Timers
- Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Parallel Arithmetic/Logic Unit (ALU) and Multiplier Execution in a Single Cycle
- Interlocked Instructions for Multiprocessing Support
- 1.8-V (Core) and 3.3-V (I/O) Supply Voltages

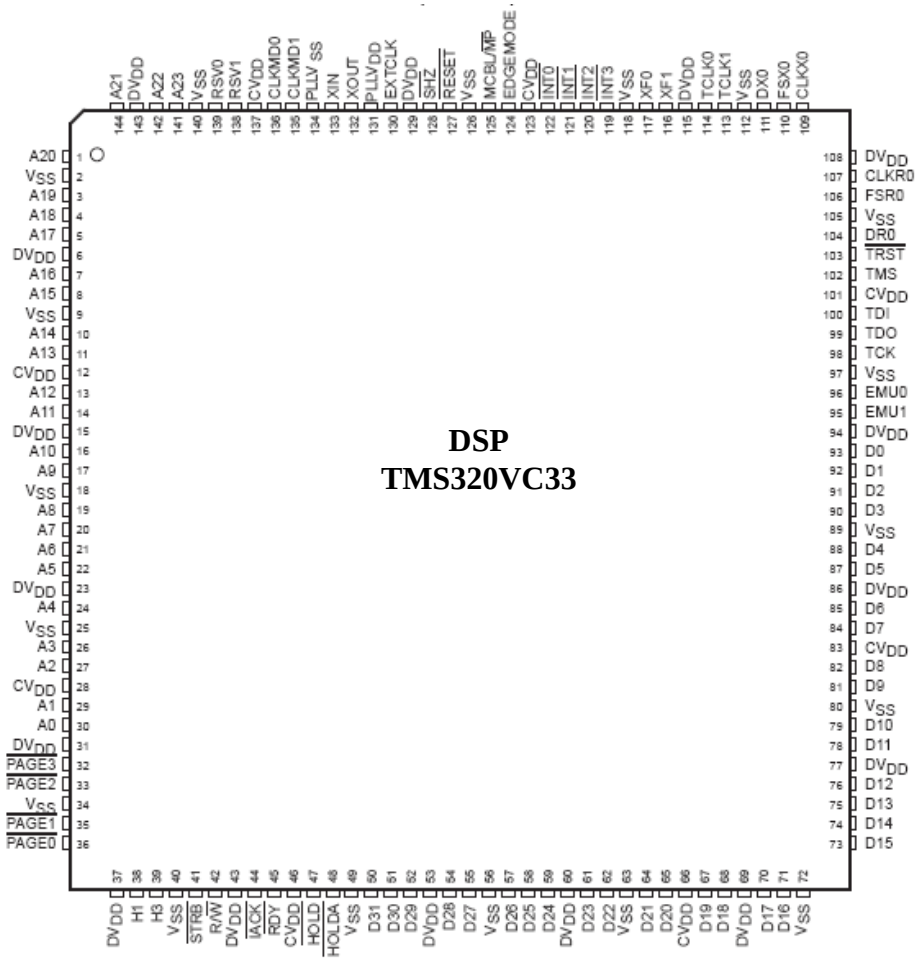


Figure 2.7 : DSP TMS320VC33 PGE 150 package I/O pin configurations

Legend:

- DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU, V_{SS} is the ground for both the I/O pins and the core CPU.
- $PLLV_{DD}$ and $PLLV_{SS}$ are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

Table 2.1 : Terminal Assignments (Alphabetical)

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
A0	30	D0	93		31	R/$\overline{W}$	42
A1	29	D1	92		37	$\overline{RDY}$	45
A2	27	D2	91		43	$\overline{RESET}$	127
A3	26	D3	90		53	RSV0	139
A4	24	D4	88		60	RSV1	138
A5	22	D5	87		69	$\overline{SHZ}$	128
A6	21	D6	85	DV_{DD}	77	$\overline{STRB}$	41
A7	20	D7	84		86	TCK	98
A8	19	D8	82		94	TCLK0	114
A9	17	D9	81		108	TCLK1	113
A10	16	D10	79		115	TDI	100
A11	14	D11	78		129	TDO	99
A12	13	D12	76		143	TMS	102
A13	11	D13	75	DX0	111	$\overline{TRST}$	103
A14	10	D14	74	EDGEMODE	124		2
A15	8	D15	73	EMU0	96		9
A16	7	D16	71	EMU1	95		18
A17	5	D17	70	EXTCLK	130		25
A18	4	D18	68	FSR0	106		34
A19	3	D19	67	FSX0	110		40
A20	1	D20	65	H1	38		49
A21	144	D21	64	H3	39		56
A22	142	D22	62	$\overline{HOLD}$	47		63
A23	141	D23	61	$\overline{HOLDA}$	48	V_{SS}	72
CLKMD0	136	D24	59	$\overline{IACK}$	44		80
CLKMD1	135	D25	58	$\overline{INT0}$	122		89
CLKR0	107	D26	57	$\overline{INT1}$	121		97
CLKX0	109	D27	55	$\overline{INT2}$	120		105
	12	D28	54	$\overline{INT3}$	119		112
	28	D29	52	MCBL/$\overline{MP}$	125		118
	46	D30	51	$\overline{PAGE0}$	36		126
	66	D31	50	$\overline{PAGE1}$	35		140
CV_{DD}	83	DR0	104	$\overline{PAGE2}$	33	XIN	133
	101		6	$\overline{PAGE3}$	32	XOUT	132
	123	DV_{DD}	15	$PLLV_{DD}$‡	131	XF0	117
	137		23	$PLLV_{SS}$‡	134	XF1	116

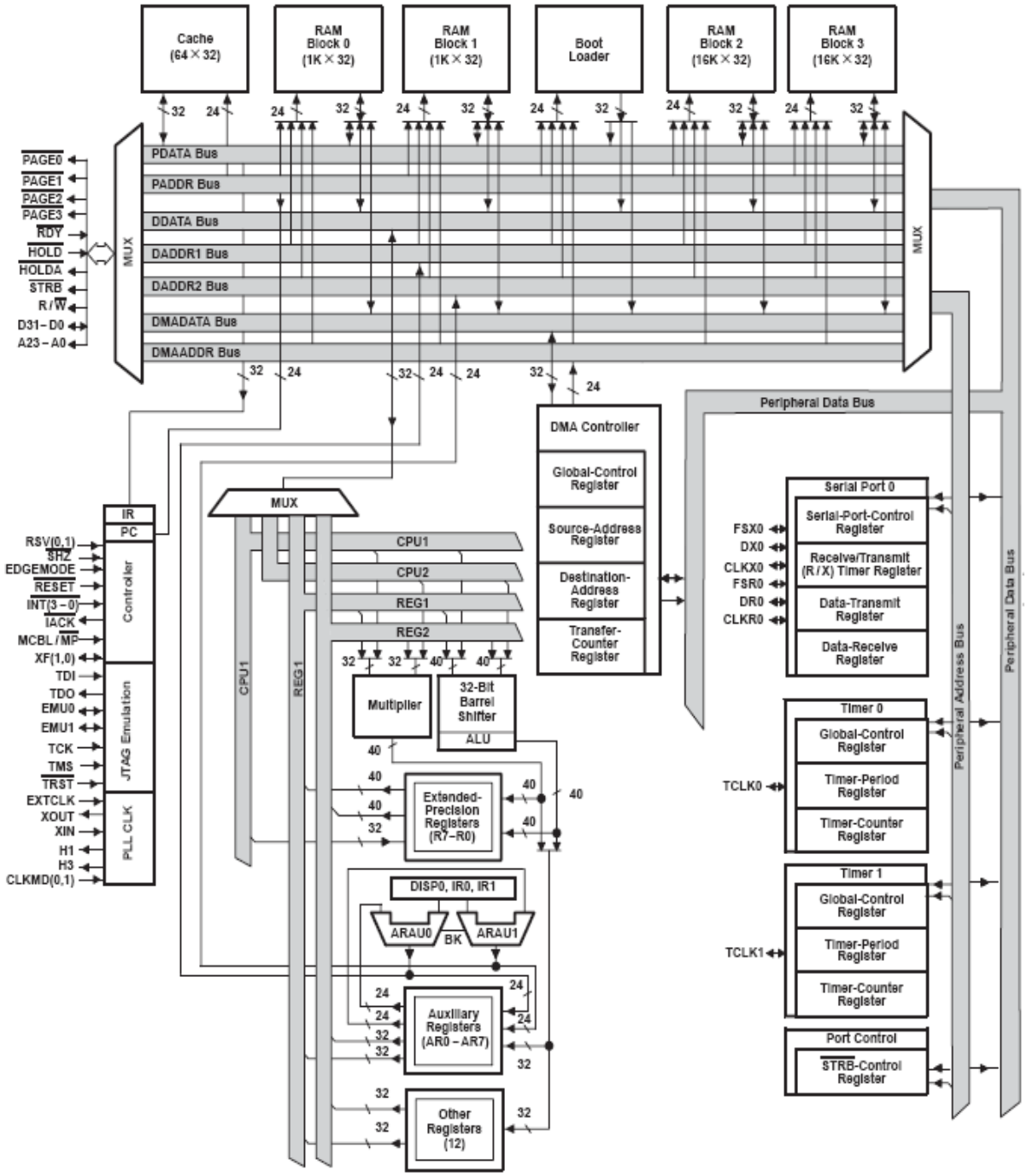


Figure 2.8 : DSP TMS320VC33 Function Block Diagram

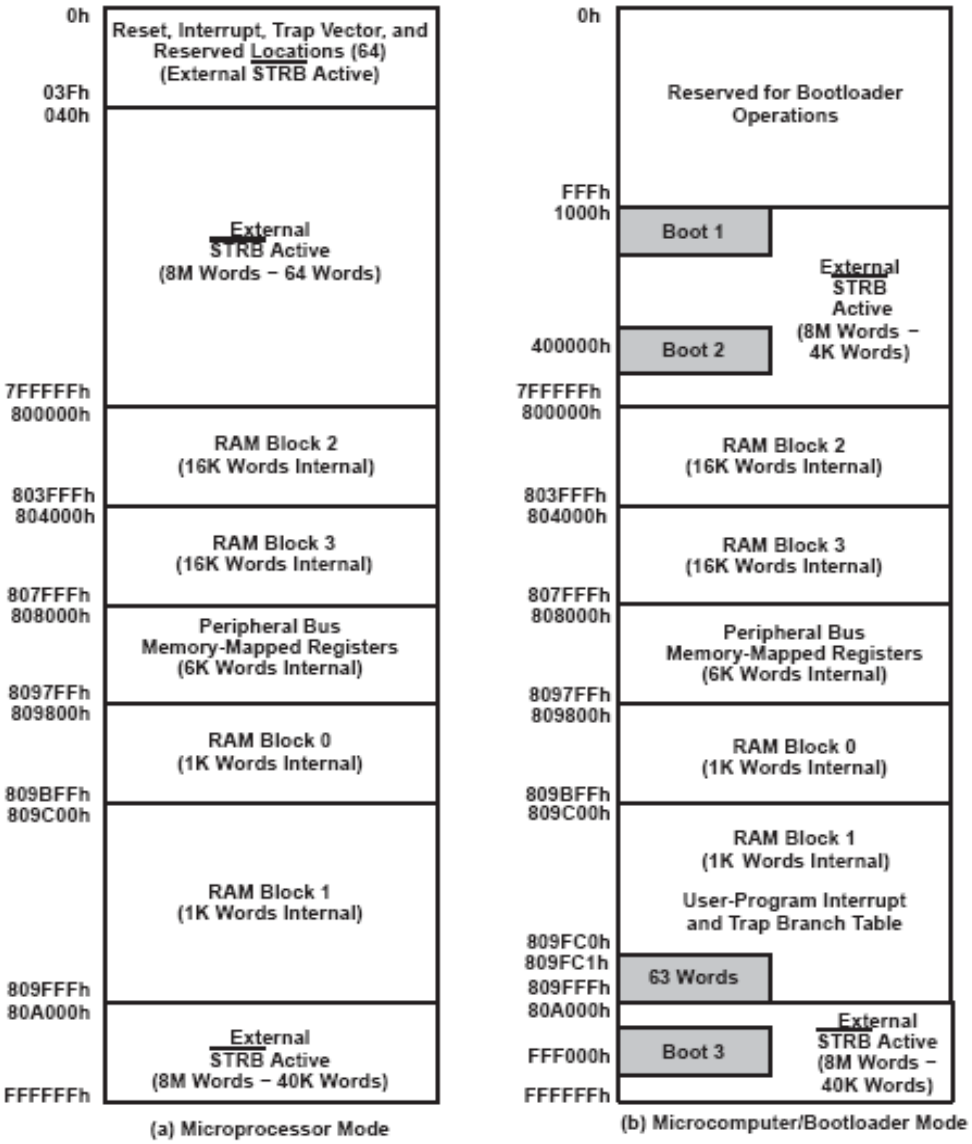


Figure 2.9 : DSP TMS320VC33 Memory Map

CHAPTER 3 – DESIGN OF DIGITAL IMAGE PROCESSING SYSTEM

3.1 Digital Image Processing System Block Diagram

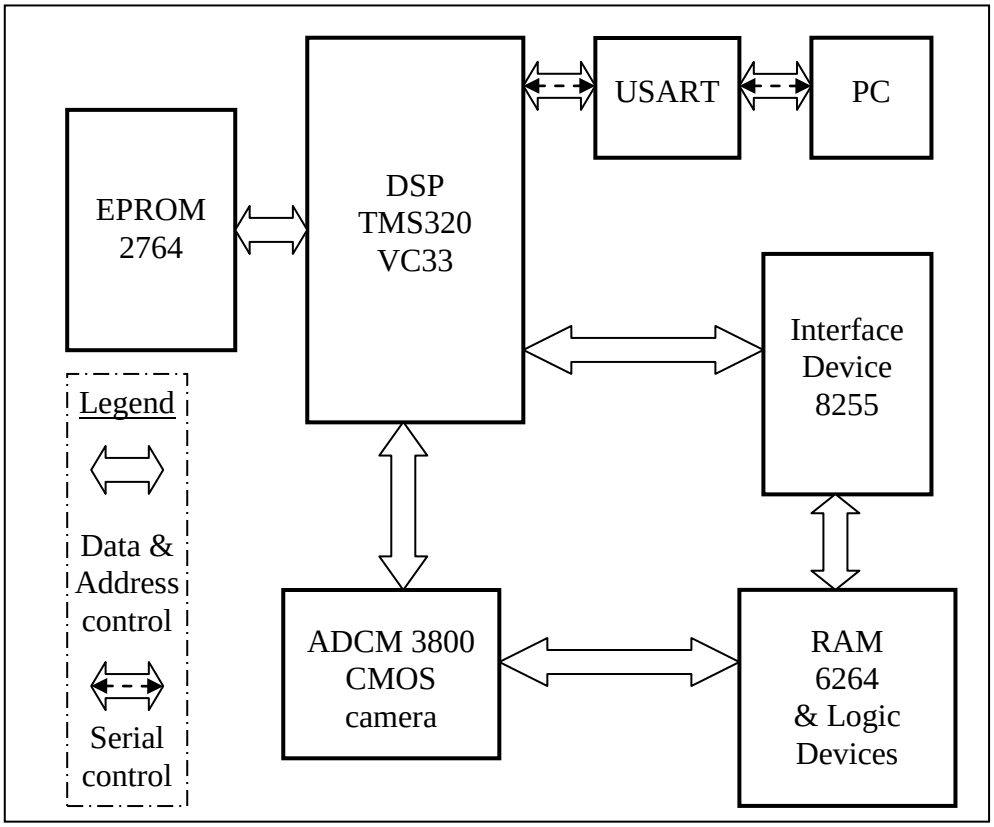


Figure 3.1 : Digital image processing system Block Diagram

3.2 System Flow Chart

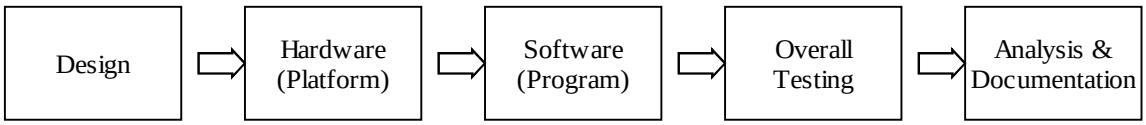


Figure 3.2 : General design flow of digital image processing system

3.3 Design Equipment

3.3.1 List Of Components

The following table shows the list of components which are required to complete the hardware system of digital image processing.

Error! Bookmark not defined.

Table 3.1 : List of components used in project

No	Component List	Quantity
1	ADCM-3800 CMOS camera module	1
2	DSP TMS320VC33	1
3	EPROM (M27C64A)	4
4	IC External Interface (8255)	1
5	IC Usart (MSM82C51A)	1
6	IC Driver Interface (MAX232)	1
7	RAM (6264)	1
8	Voltage Shifter (74HC4050)	1
9	Counter (74HC4020)	1
10	Counter (74HC393)	1
11	3-to-8 Decoder/Mux (74LS138)	1
12	Buffer (74LS244)	2
13	Baud Rate Generator (HD4702)	1
14	AND gate (74LS08)	1
15	NOT gate/Inverter (74LS14)	4
16	Voltage Regulator (LM317)	3
17	Relay 5.0V	2
18	Crystal Oscillator (4.9152MHz)	1
19	Crystal (15.000MHz)	1
20	Crystal (2.4576MHz)	1
21	On/Off Switch	1
22	8 pins DIP Switch	1
23	Connector	7
24	LED	1
25	Resistor	15
26	Electronic & Ceramic Capacitor	13
27	Printed Circuit Board (PCB)	3
28	Veraboard	1
29	RS232 Connector (Male & Female)	2
30	RS232 Cable	1
31	Wire wrap Tool	1
32	Interfacing Row	2
33	Spacer & PCB Stand	26

3.3.2 Components Functionality

3.3.3.i) ADCM-3800 SXGA CMOS Camera

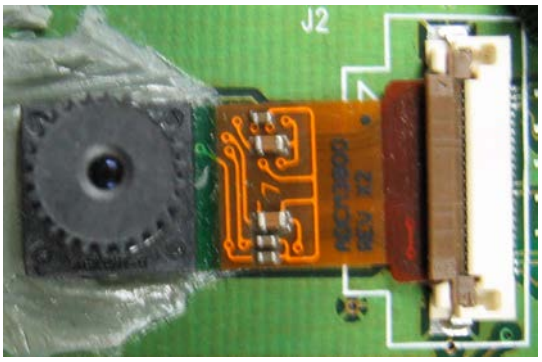


Figure 3.3 : ADCM 3800 SXGA CMOS Camera

The ADCM- 3800 camera module contains a single integrated circuit which builds in an image sensor and an image processor. The image sensor has a rectangular pixel array of 1280 x 1024 pixels and its function is to convert the input either still image or video image into digital data form. This CMOS camera can perform few types of output format, which are gray scale (serial or parallel), YCbCr (4:4:4), YCbYCr (4:2:2A), RGB (444C), RGB (332) and so on, all in either video or still image form.

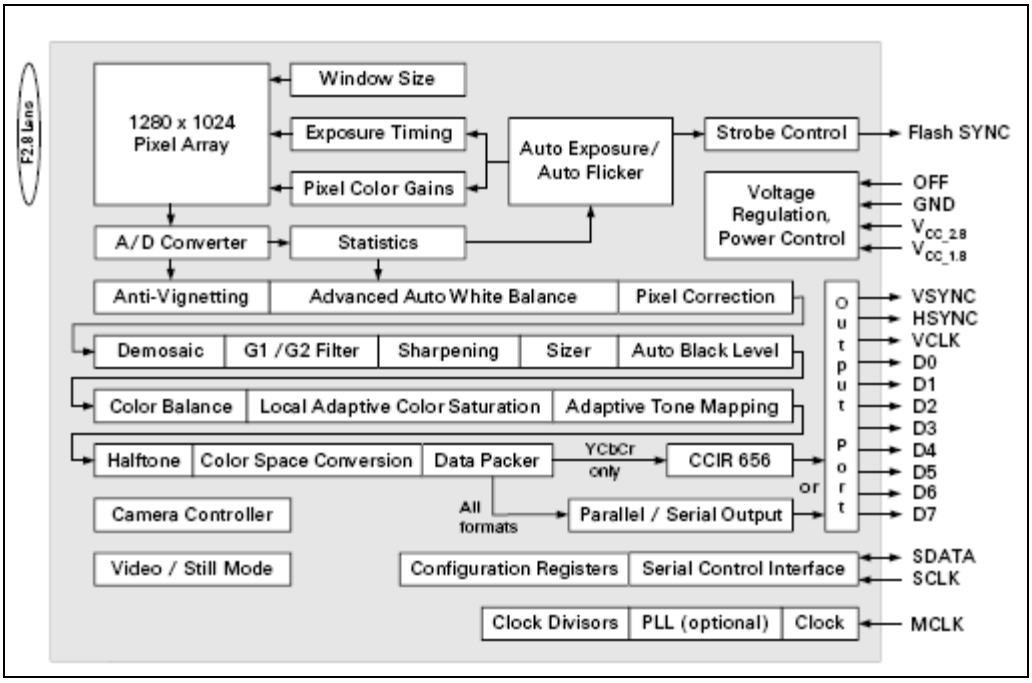


Figure 3.4 : ADCM 3800 SXGA CMOS camera block diagram

Table 3.2 : ADCM 3800 CMOS camera terminal function

Pin No	Terminal Name	Description/Function
1 & 18	GND	Ground signal (0v)
17	Vcc	Power source (+2.8v)
2	M_CLK	Input clock
3	VSYNC	Vertical synchronization/end of frame. Show start/end an image.
12	VCLK	Video clock/data ready. Signal show existing data in output.
13	HSYNC	Horizontal synchronization/end of line. Show line in process.
14	ON/OFF	On/Off the operation of camera
15	SCL	Serial control clock
16	SDA	Serial input and output data control
4 - 11	DATA0-DATA7	Output image data . If serial input/output data, ONLY pin11 used.

Table 3.3 : Major control register need to control the operation of the camera

Register Name	Address	Description	Default
ID	0 x 0000	Chip ID	0 x 0068
CONTROL	0 x 0002	Camera control	0 x 0001
STATUS	0 x 0004	Camera status	0 x 0004
CLK-PER	0 x 0006	External clock frequency	0 x 0514
SIZE	0 x 0008	Image size and orientation	0 x 0b84
OUTPUT_FORMAT	0 x 000a	Output format	0 x 0909
OUTPUT_WID_S	0 x 0024	User-defined picture output width, still	0 x 0280
OUTPUT_HGT_S	0 x 0026	User-defined picture output height, still	0 x 0280
CLK_PIXEL	0 x 080e	Number of sensor clock per pixel	0 x 0100

The table below shows the connection of ADCM 3800 CMOS camera to peripheral devices. The Input pins camera must connect through a buffer 74LS244 or voltage shifter 74HC4050 to step down or regulate the high voltage signal from directly enter the camera. The camera will be spoiled with high voltage signals. Thus, the camera must operate in typical voltage 2.8v.

Table 3.4 : Connection ADCM-3800 SXGA CMOS Camera to peripheral devices

No	CMOS Camera	Connect to	Devices
1	ON/OFF	→	3Y voltage shifter HC4050
2	HSYNC	→	Pin 2 AND gate
3	DATA7	→	Pin 2A4 buffer 74LS244
4	DATA6	→	Pin 2A3 buffer 74LS244
5	DATA5	→	Pin 2A2 buffer 74LS244
6	DATA4	→	Pin 2A1 buffer 74LS244
7	DATA3	→	Pin 1A4 buffer 74LS244
8	DATA2	→	Pin 1A3 buffer 74LS244
9	DATA1	→	Pin 1A2 buffer 74LS244
10	DATA0	→	Pin 1A1 buffer 74LS244
11	VSYNC	→	Pin 1 AND gate
12	M_CLK	→	4Y voltage shifter HC4050
13	VCLK	→	Pin 12 AND gate
14	SCL	→	2Y voltage shifter HC4050 and Vdd
15	SDA	→	1Y voltage shifter HC4050, PC4 8255 and Vdd

3.3.3.ii) Digital Signal Processor (DSP) : TMS320VC33

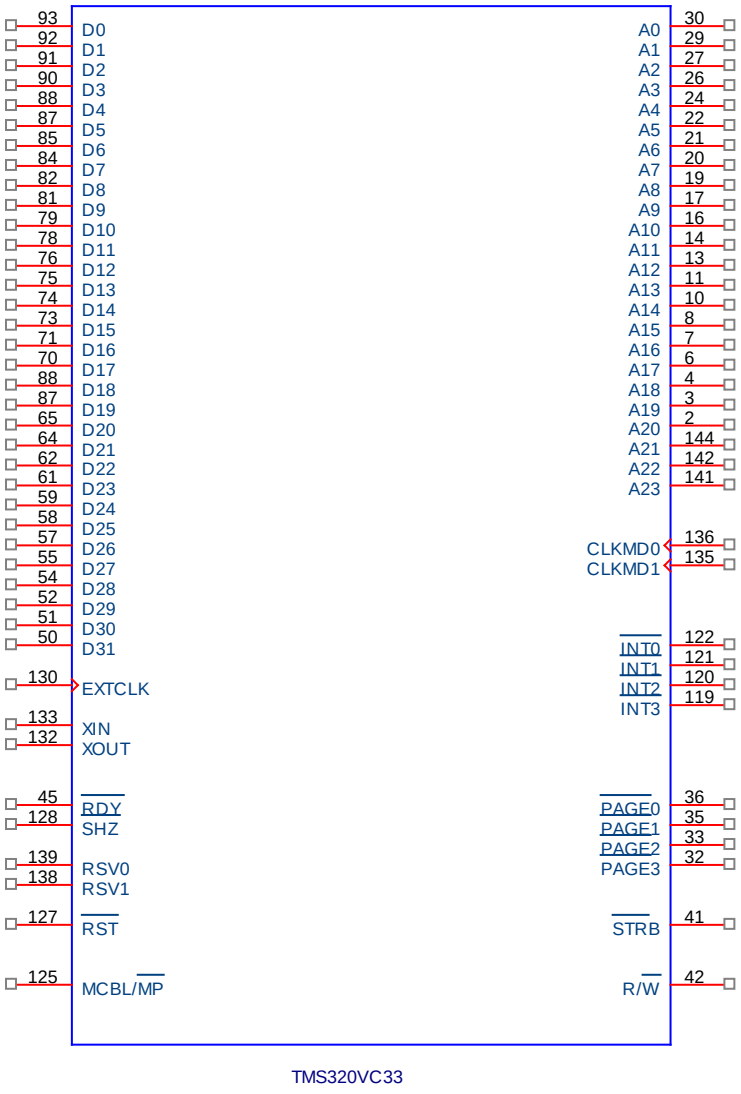
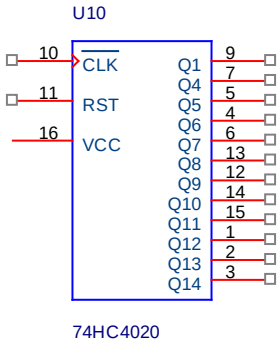


Table 3.5 : TMS320VC33 terminal functions

No	Terminal Name	Description/Function
1	D31 – D0	32 bit data port
2	A23 – A0	24 bit address port
3	R/$\overline{W}$	Read/Write data enable to access the processor
4	$\overline{STRB}$	Strobe, for all external accesses
5	$\overline{PAGE0}$ - $\overline{PAGE3}$	Page strobes, connected to external memory
6	$\overline{RESET}$	Active low to perform reset condition

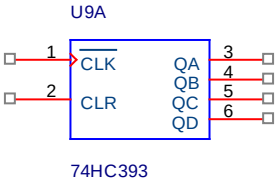
7	$\overline{INT0}$ - $\overline{INT3}$	External interrupts
8	$\overline{SHZ}$	High to avoid device memory and register contents corrupted
9	CV_{DD}	Dedicated 1.8v power supply for core CPU
10	DV_{DD}	Dedicated 3.3v power supply for the I/O pins
11	Vss	Ground
12	EXTCLK	External clock to processor
13	XIN	Clock in to ground because EXTCLK is used
14	XOUT	Clock out should left unconnected because EXTCLK is used
15	CLKMD0,CLKMD1	Clock mode select pins
16	RSV0 , RSV1	Reserved. Use individual pull up to DV_{DD}

3.3.3.iii) Counter : 74HC4020



- This chip also functions as a counter to count and store the digital image data from camera into A4 to A12 RAM 6264 address memory.

3.3.3.iv) Counter : 74HC393



- This chip functions as a counter to count and store the digital image data from camera into A0 to A3 RAM 6264 addresses memory.