CHARACTERIZATION OF ADC

Oleh

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ABSTRACT

This report consists of functional description, design of test circuit board, built up the PCB test circuit, also the measurement and characterization for ADC0804LCN analog to digital converter IC chip. This project is mainly to characterize the analog to digital converter IC. IC ADC0804LCN 8-bit national semiconductor is used as specimen IC to define several characteristics. To measure the characteristics of the IC, firstly have to design and built a test circuit board to make the IC operate. After that, implement several methods to characterize the IC. Linearity, clocking frequency, time conversion and relation between input voltage (Vin) and voltage reference over two (Vref/2) are the characteristics that measured in this project. This type of experiment that had been conduct can be used to measure characteristic of the IC such as linearity, clock frequency, time conversion and relation between input voltage and voltage reference over two.

ACKNOWLEDGEMENT

First of all I would like to thanks Allah the almighty for giving me strength to finish up my final year project successfully even though I have to encounter a lot of problems during the process of finishing this project.

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Finally I hope that this project will bring some benefits whether for myself and hopely to everybody that has involve.

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CHAPTER 1: INTRODUCTION

This chapter consists of the objective and introduction about this project. ADC characterization use ADC0804LCN as specimen IC for implements several test to characterize the IC. This IC chip is CMOS 8 bit successive approximation analog digital converter use the differential potentiometric ladder similar to 256R products.

Objective of this project mainly to define the characteristics of the specimen IC ADC0804LCN by design the test circuit board which suitable with the specification of the IC and another component in the circuit.

CHAPTER 2: FUNCTIONAL DESCRIPTION OF ADC0804LCN

2.0 Introduction to ADC0804LCN IC Chip

The ADC0804LCN is CMOS 8-bit A/D converter use a differential potentiometric ladder. Differential analog voltage inputs allow increasing the offsetting zero input voltage value. The voltage reference can be adjusted to allow encoding any smaller input voltage range due to the full 8 bits. Below is the ADC0804LCN schematic IC chip diagram.

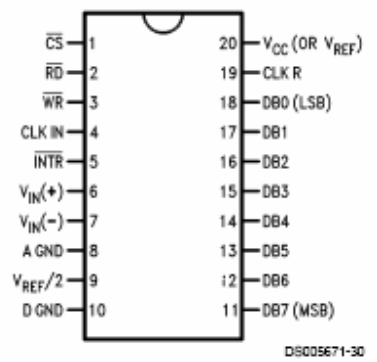

Figure 2.1: ADC0408LCN schematic [4]

To operate this chip, have four main pin should gives priority. Firstly is pin 1, that is chip select (CS), then pin 2 and 3 that are pin read (RD) and write (WR), and interrupt (INTR) that locate at pin 5. To start the conversion, make CS=0 and send a low to high pulse to pin WR, while INTR and RD pin in high condition. If the INTR pin is trigger to low that will end the conversion. After the INTR has become low, pin CS set to zero (CS=0), and one high to low pulse or trigger high is send to RD pin to get the data out of the ADC0804LCN. The timing for this process is shown graphically in figure 2.2:

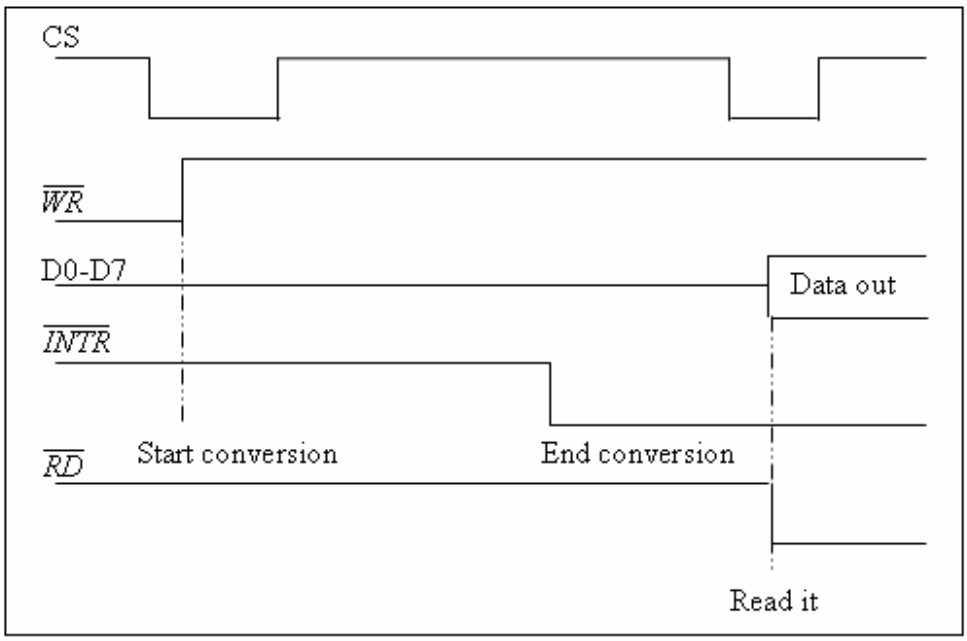

Figure 2.2: Read and Write timing for ADC0804LCN.

The clock in (CLK IN) pin 4 is an input pin connected to an external clock source when an external clock is used for timing. ADC0804LCN has an internal clock generator or self-clocking. To use the internal clock generator of this IC, the CLK IN and CLK R pins are connected to a capacitor and a resistor.

$V_{IN}(+)$ and $V_{IN}(-)$ are pin for analog input voltage range, analog input voltage will feed in through $V_{IN}(+)$ with voltage range 0V to 5V direct current. This two analog input pin are tied up with two on chip diodes (internal chip), which will forward conduct for analog input voltages, one diode drop below ground or one diode drop greater than the $V_{CC.}$

ADC0804 have two type of ground (GND), which is analog ground (A GND) and digital ground (D GND). Pin 8 is conduct for analog ground, which connects to analog ground V_{IN} supply. While pin 10 is for digital ground connected to the ground of the V_{CC} pin. The reason that should have two ground pins is to isolate the analog V_{IN} signal from transient voltages caused by digital switching of the output D0-D7. Another reason is, internally the chip have digital and analog blocks, so both of this blocks must grounds separately. In the real world of data acquisition, both the analog and digital grounds are handled separately

Vcc or VREF pin 20, typically supplied with 5.12 volt. While Pin 9 is $V_{REF}/2$ pin, this pin is an input voltage used for the reference voltage typically supplied with 2.56 volt. That will cause the analog input voltage V_{IN} for ADC0804LCN is in the range of 0 to 5 volts. For others applications of voltage input range, the value of V_{CC} or V_{REF} and $V_{REF}/2$ have to calibrate to get the desired voltage input range. The relation between V_{REF} and $V_{REF}/2$ will discuss in section 5.3.

Digital 8 bits data output for ADC0804LCN is through pin 11 until pin 18. The least significant bit (LSB) is conduct by pin 18, and most significant bit is conduct by pin 11. These are the tri-state buffered and the converted data is accessed only when CS=0 and RD is forced low. The minimum voltage output when logic “1” is energize is 2.4V dc with I_O=−360 µA, V_{CC}=4.75 VDC. When I_O=−10 µA with the same V_{CC}, the minimum voltage output logic “1” is 4.5V dc.

Figure 2.3 is the functional diagram of ADC0804. Input WR shift from high to low that causes the internal SAR latches and shift register stages are reset. The ADC0804 chip will remain in a reset condition, as long as the CS and WR input remain low. After at least one of these inputs makes low to high transition, the internal clocks again provide a reset signal for the start F/F and conversion will start from 1 to 8 clock period.

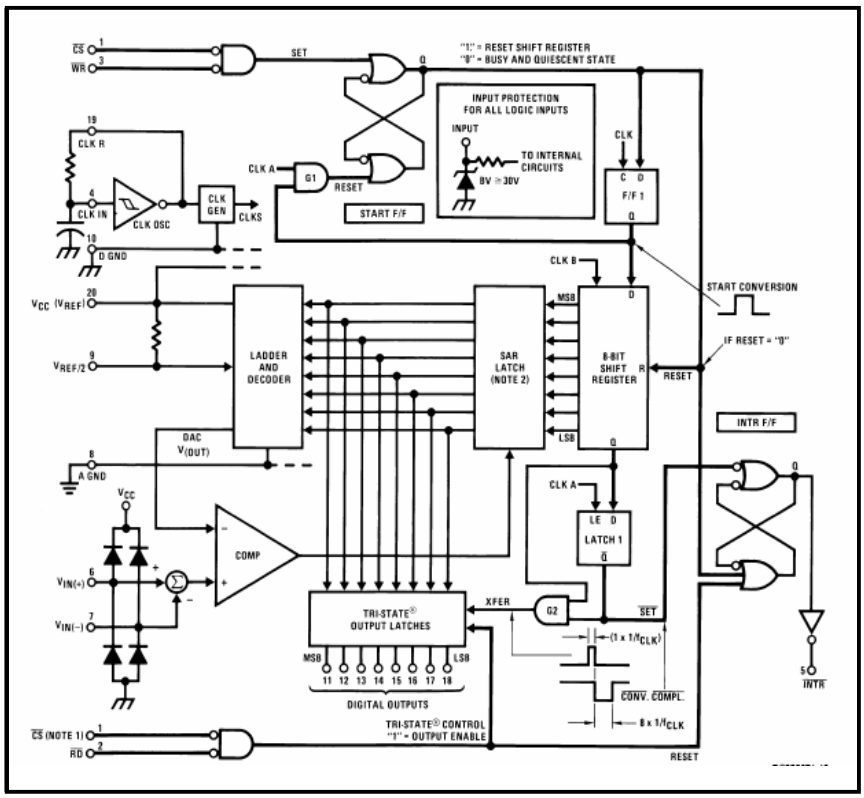

Figure 2.3: Functional diagram of ADC0804LCN [4]

After “1” is clocked through the 8 bit shift register (complete the SAR search) it appears as the input to the D type latch, LATCH 1 (also set the INTR F/F). The output (Q=1) from the shift register also appear as the input for AND gate G2, causes the new digital word to transfer to the TRI-STATE output latches. When data is to be read, the combination of both CS and RD being low will cause the INTR F/F to be reset and the TRI-STATE output will be enabled to provide the 8 bit digital outputs. CS and RD remain low, the data output remain enable and the INTR output will still signal the end conversion (high to low transition).

The device can be operated in the free-running mode by connecting INTR pin to the WR input pin with CS is feed with logic zero (CS = 0). An external pulse required to power up the cycle through the WR. The START F/F is set by the high to low transition of the INTR signal and this resets the SHIFT REGISTER which causes input to the D-type latch, LATCH 1, to go low. The Q output of LATCH 1 will go high, as long as the latch enable input still have clock signal, and continuously allows the INTR F/F to be reset.

When data from the input signal is to be read, the CS and RD being low and this will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Analog Input Noise

Noise and undesired digital clock get through the analog input pins (pins 6 and 7) can cause system error. The source resistance for these inputs should be below 5kΩ. Larger values of source resistance can cause undesired system noise. Input bypass capacitors connect from the analog input to ground will eliminate system noise, but can effects the analog scale errors as these capacitor will average the transient input switching currents. The scale error depends on both, the use of an input bypass capacitor and a large source resistance. This error can be solving by doing a full scale adjustment of the chip with the input bypass capacitor and source resistance.

Another method can be implementing to eliminate the noise and undesired clock to disturb the analog input signal is, by implement the filtering circuit between the analog supply and analog input voltage of the ADC circuit. Filter circuit can be built by using op-amp, for example ic chip LM358. For example by uses the Chebyshev implementation for steeper roll-off unity-gain, 2nd order low pass filter. The noise filtering analog input signal circuit is shown in figure 2.4 below. This figure adapted from [4].

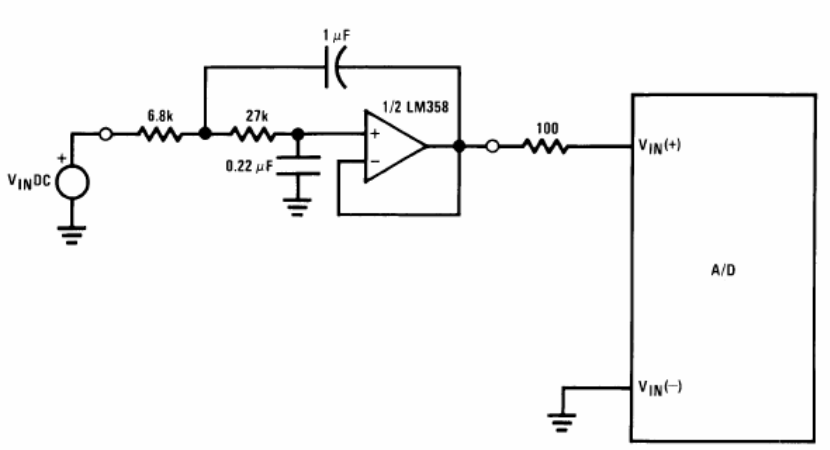

Figure 2.4: Noise Filtering analog input signal circuit [4]

2.2 Reference Voltage Span Adjust.

These ADC chip have been designed to hold a 5V dc, 2.5V dc or an adjusted voltage reference. The reference voltage for the IC is either half of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply or a less than 2.5V dc can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ is 2, that making the full-scale differential input voltage twice the voltage at pin 9.

2.3 Errors and Reference Voltage Adjustment

- Zero error

  The converter can be made to output 0000 0000 8 bits digital code for this minimum input voltage by biasing the ADC chip VIN(-) input at this VIN(MIN) value. The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the VIN (−) input and applying a small magnitude positive voltage to the VIN (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal 1⁄2 LSB value (1⁄2 LSB = 9.8 mV for VREF/2=2.500 VDC).

- Full scale

  The full-scale adjustment can be made by applying a differential input voltage that is 1 1⁄2 LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the VREF/2 input (pin 9 or the VCC supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.4 Clocking option

Have two options to derive the clock for this ADC chip, either derived from the CPU clock or an external RC circuit to provide self clocking. CLK IN pin 4 uses a Schmitt trigger as shown in figure 2.5 below.

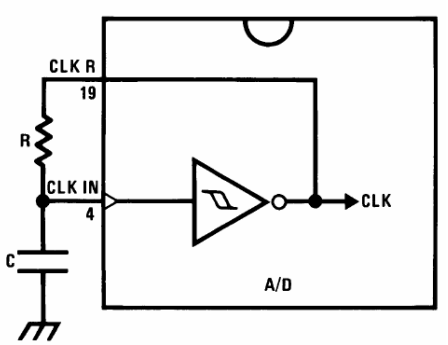

Figure 2.5: Self-clocking the ADC0804 [4]

Besides external RC circuit to provide self clocking for the ADC0804, has one circuit that involve using of pair of LM358 operational amplifier. The name of this circuit is Voltage Control Oscillator. This circuit will provide two type output oscillator wave, there are square wave and triangular wave.

Output wave from this circuit will control by the input voltage Vc. The schematic diagram for Voltage Control Oscillator (VCO) circuit is shown in figure 2.6.

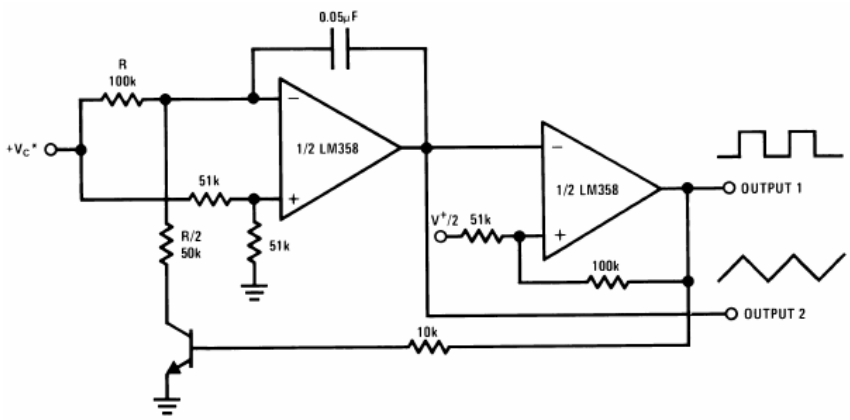

Figure 2.5: The schematic diagram for Voltage Control Oscillator (VCO) crcuit.[6]

Have several expressions to relate the clock frequency f_{CLK} with the resistor R and capacitor C as shown below.

$$f_{CLK} = \frac{1}{1.1(RC)} \tag{2.1}$$

$$T_{CLK} = \frac{(RC)V_{IN}}{V_{REF}} \tag{2.2}$$

2.5 Restart during a Conversion

If the A/D is restarted (CS and WR go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The INTR output simply remains at the “1” level.[4]

2.6 Continuous conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the CS input is grounded and the WR input is tied to the INTR output. This WR and INTR node should be momentarily forced to logic low following a power-up cycle to guarantee operation.[4]

CHAPTER 3: DESIGN TEST CIRCUIT FOR ADC0804LCN

3.0 Introduction of Test Circuit Design.

The test circuit that has been design, consist of several part of circuit that provide different function. This design is combination of basic test circuit for ADC0804LCN including self-clocking circuit connect to CLK IN and CLK R, noise filtering circuit for the analog input, using Chebyshev implementation for steeper roll-off unity gain 2^{nd} order low pass filter. Also involve supply voltage control circuit, such as voltage divider circuit and potentiometer circuit.

3.1 Basic Test circuit for ADC0804LCN

This circuit is the simplest test to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output 8 bit code. The schematic of the test circuit is shown in figure 3.1.

For this test circuit, the supply voltage V_{CC} (pin 20) should be supplied with 5.12V dc and a $V_{REF}/2$ (pin 9) supply with 2.560 V dc. For a full scale adjustment, an analog input voltage 5V dc is applied to the V_{IN} (+) pin (pin 6) with V_{IN} (-) pin (pin 7) connects to analog ground. The value of $V_{REF}/2$ should be adjusted until the digital output 8 bit code is just changing from 1111 1110 to 1111 1111. Then value of $V_{REF}/2$ ready to use for all test with another value of analog input voltage.

Header supply and ground are function to interface the test circuit board with power supply, analog ground and digital ground. The first leg of this header is connecting with voltage supply 7V dc, while the second leg connects with 5.12V dc supply voltage. Another two legs, there are leg number 3 and 4 are connects to analog ground and digital ground.

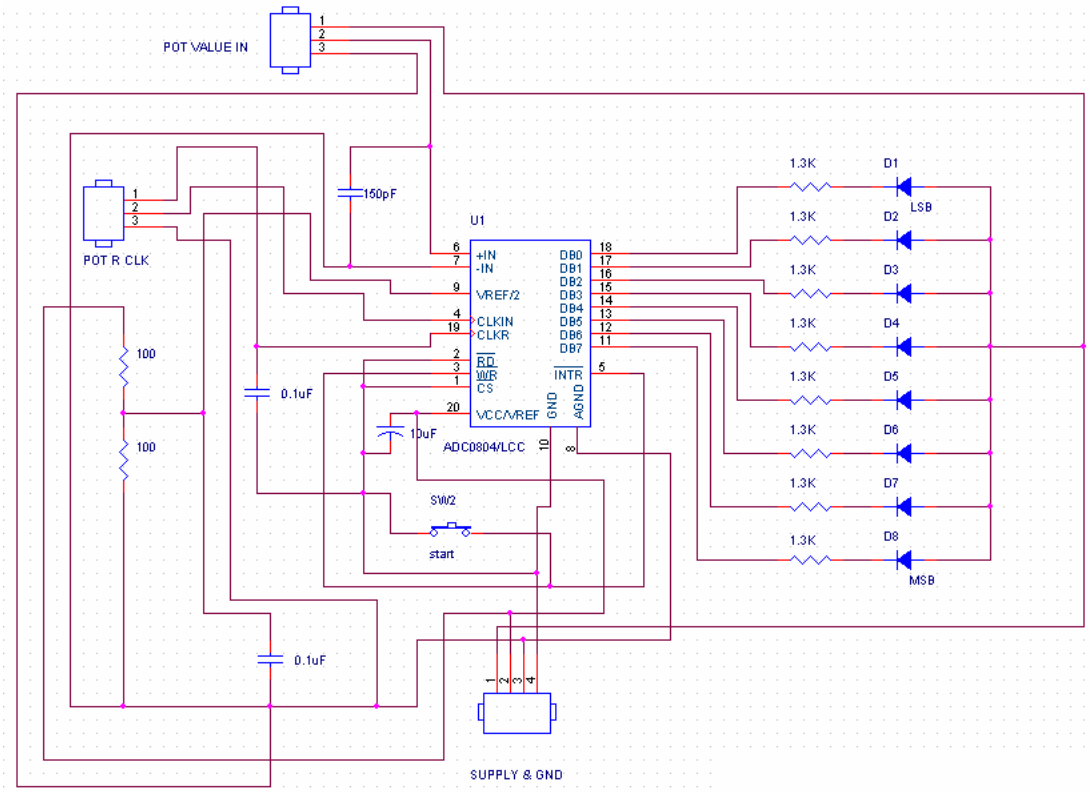

Figure3.1: The schematic of the test circuit.

For this test circuit design, the clock frequency (f_{CLK}) derived from an external RC circuit. This method also called self-clocking method. The resistor for RC circuit is change with potentiometer (POT), these is because to yield different value of clock frequency. The clock frequency can be change by varying the resistance of potentiometer. If the resistance of potentiometer is reducing, the frequency of the clock will increase. That mean the relation between resistance and frequency are reciprocal.

3.2 Noise Filtering Circuit for Analog Input Voltage.

This noise filtering circuit use Chebyshev implementation for steeper roll-off unity gain 2nd order low pass filter. This circuit consists of LM358 operational amplifier function as filter. The schematic for noise filtering circuit is shown in figure 3.2:

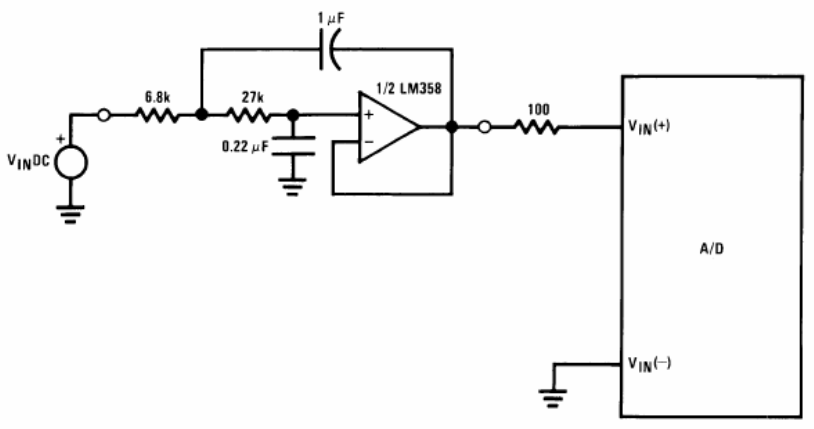

Figure 3.2: Noise Filtering Circuit for Analog Input. [4]

Advantages of Chebyshev type of filter, better attenuation beyond the pass-band than Butterworth filter. Disadvantages of this filter are ripple in pass-band and considerable ringing in step pulse response than Buttherworth type.

3.3 Analog Input Voltage for ADC0804LCN

The analog input voltages for ADC0804LCN are in the range of 0V dc to 5V dc. Theoretically with input 0V dc will give 8 bit digital output of 0000 0000, while full scale 5V dc 1111 1111. To varying the input voltage the suitable method is by using the potentiometer. To execute this method is by connect one of the side leg to 5V dc and another side leg to analog ground and the center leg of potentiometer connect to the analog input voltage V_{IN} pin 6. The schematic diagram of the analog input voltage circuit is shown in figure 3.3.

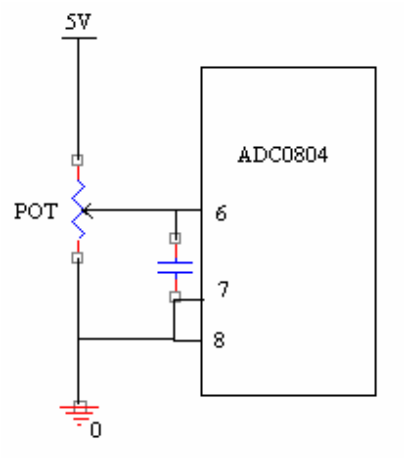

Figure 3.3: Analog Input Voltage Circuit.

Output of center leg potentiometer is the analog input voltage to the ADC0804LCN. The desire input voltage can be obtained by varying the potentiometer. The voltage value cannot over than range 0V and 5V dc.

3.4 Supply and Ground on board.

This part is one of the important parts in this design. In this design circuit, involve several IC chips that required different value of supply and input voltage. For example ADC0804LCN, this IC required 5.12V dc as VCC supply voltage, 2.56V dc as VREF/2 and 5V for maximum voltage to analog input voltage potentiometer. Another IC chips consist are LM358 operational amplifier and 7404 inverter. LM358 required 7V dc as supply voltage to activate this IC, and to give better output as analog input voltage to ADC0804. For 7404 inverter IC chip required 5V dc to become supply voltage to activate this IC.

In this design just involve 2 header to connect with power supply, one header will dispense 7V dc to the test board, and another one header will supply 5.12V dc. To gratify all necessity, several circuits have to build to ensure all the IC chips involve receive correct value of supply voltage.

One of the methods can be implement is voltage divider, this method involve two resistor in series connection. One side of both resistors connects to supply voltage and another side connects to analog ground. The value of both resistors will give the major effect to the output value of this circuit. The output value will come out from the center between resistors. The voltage divider circuit is shown in figure 3.4.

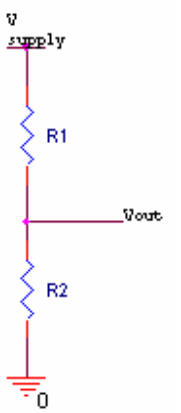

Figure 3.4: Voltage Divider Circuit.

This method actually same as potentiometer methodology, but this method involve passive resistor. To get the desire output voltage, values of resistor have to define nicely because this resistor is passive component, not all value of resistance are exist. To make ease design work, values of both resistors can be define by using of calculation below.

$$V_{out} = IR2 \tag{3.1}$$

$$V_{IN} - V_{out} = IR1 \tag{3.2}$$

Replace (3.1) into (3.2),

$$V_{IN} - IR2 = IR1 \tag{3.3}$$

$$V_{IN} = IR2 + IR1 \tag{3.4}$$

$$V_{IN} = (R2 + R1)I \tag{3.5}$$

$$I = \frac{V_{out}}{R2} \tag{3.6}$$

Replace (3.6) into (3.5),

$$V_{IN} = \frac{(R2 + R1)V_{out}}{R2} \tag{3.7}$$

$$V_{out} = \left(\frac{R2}{(R2 + R1)} \right) V_{IN} \tag{3.8}$$

$$R1 = R2\left(\frac{V_{IN}}{V_{out}} \right) - R2 \tag{3.9}$$

$$R1 = R2\left(\frac{V_{IN}}{V_{out}} - 1 \right) \tag{3.10}$$

To get output 5V dc with input 7V dc the resistor R2 has chosen first with value of 7.5KΩ. After calculation the value of resistor R1 is 3.0KΩ. The schematic circuit for this circuit is shown in figure 3.5.

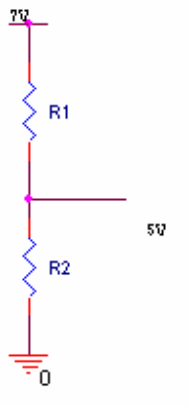

Figure 3.5: Schematic Circuit for Voltage Divider with Input Voltage 7V and Output Voltage 5V dc.

Another voltage divider circuit is involved voltage input of 5.12V and the output voltage half from the input circuit, V_{OUT} is 2.56V dc. For this circuit just select the same value of resistors, to get the desire output. For this design value of resistors that already selected are 100Ω. The schematic circuit for this specification is shown in figure 3.6.

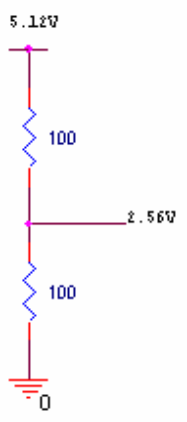

Figure 3.5: Schematic Circuit for Voltage Divider with Input Voltage 5.12V and Output Voltage 2.56V dc.

For this ADC0804LCN design circuit board involved two types of ground, there is analog ground and digital ground. Analog ground has to connect with ground power supply, while digital ground connects to digital input 0 bit.

On the test circuit, all analog ground either from ADC0804 or other IC chip should be ground together, or another term to describe this condition is common ground.

3.5 The Output Display.

On this test board design involve 8 LED to display the 8 bit output from the ADC0804LCN. All LED are protect with 1.3kΩ for each. The least significant bit (LSB) come out from pin 18 ADC0804LCN, while most significant bit (MSB) from pin 11.

If the output circuit connects like in figure 3.6, the output will be invert from the actual output from output pins ADC0804. This is because of the 5V dc supply connect to all anode of LED.

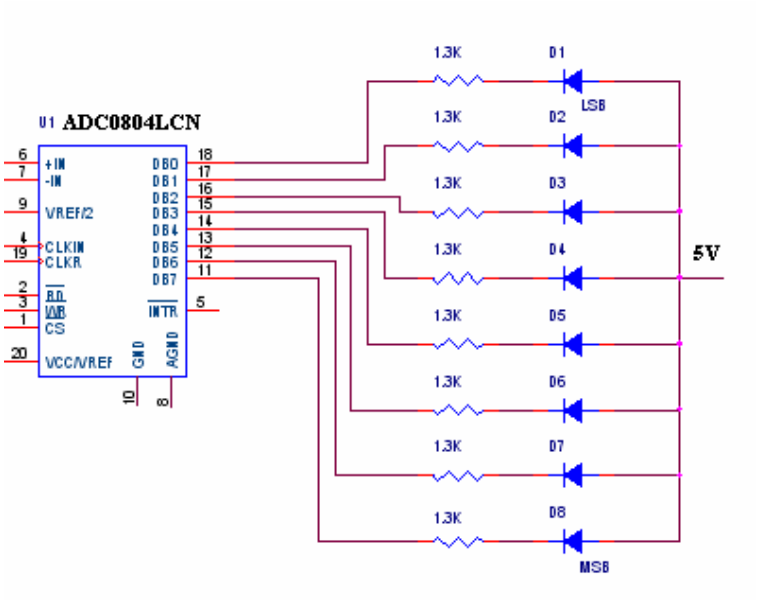

Figure 3.6: The Output Display Schematic Circuit 5V Connect to Anode.

To solve this problem either connects inverter between output ADC0804LCN and LED, or switch all the LED to the invert side and connects the cathodes to analog ground. To see the schematics circuit for both circuits, please refer to figure 3.7 and 3.8.

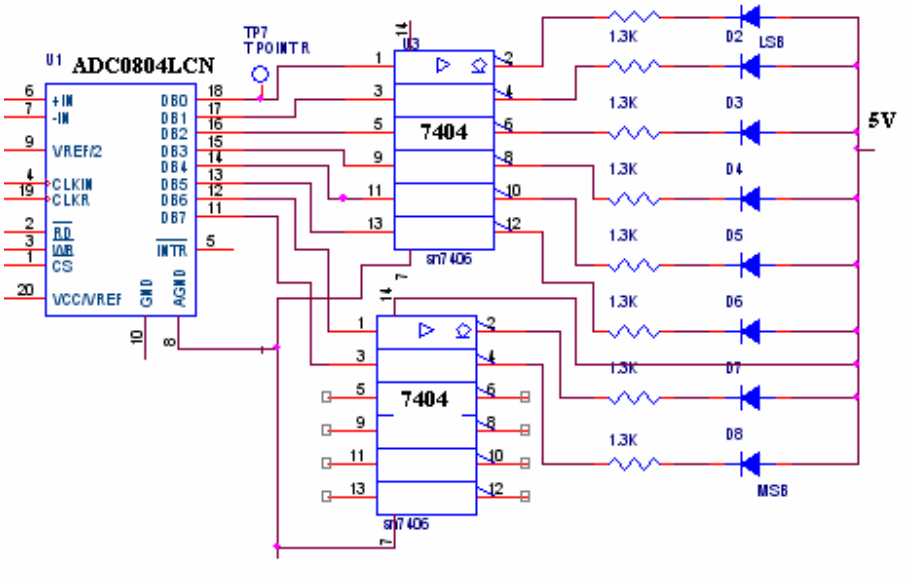

Figure 3.7: The Output Display Schematic Involve Inverter 7404 with supply 5V Connect To Anode.

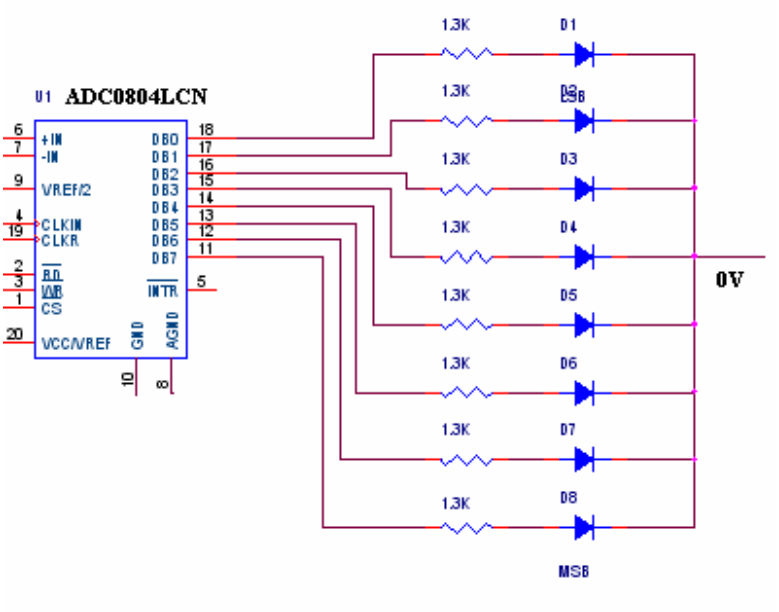

Figure 3.8: The Output Display Schematic Circuit with Cathode Connect To Ground.

Finally when all element circuit designs above are assemble together, that will yield the optimum test circuit board for ADC0804LCN. The schematic diagram for the design of test circuit board for ADC0804LCN IC chip is shown in figure 3.6.

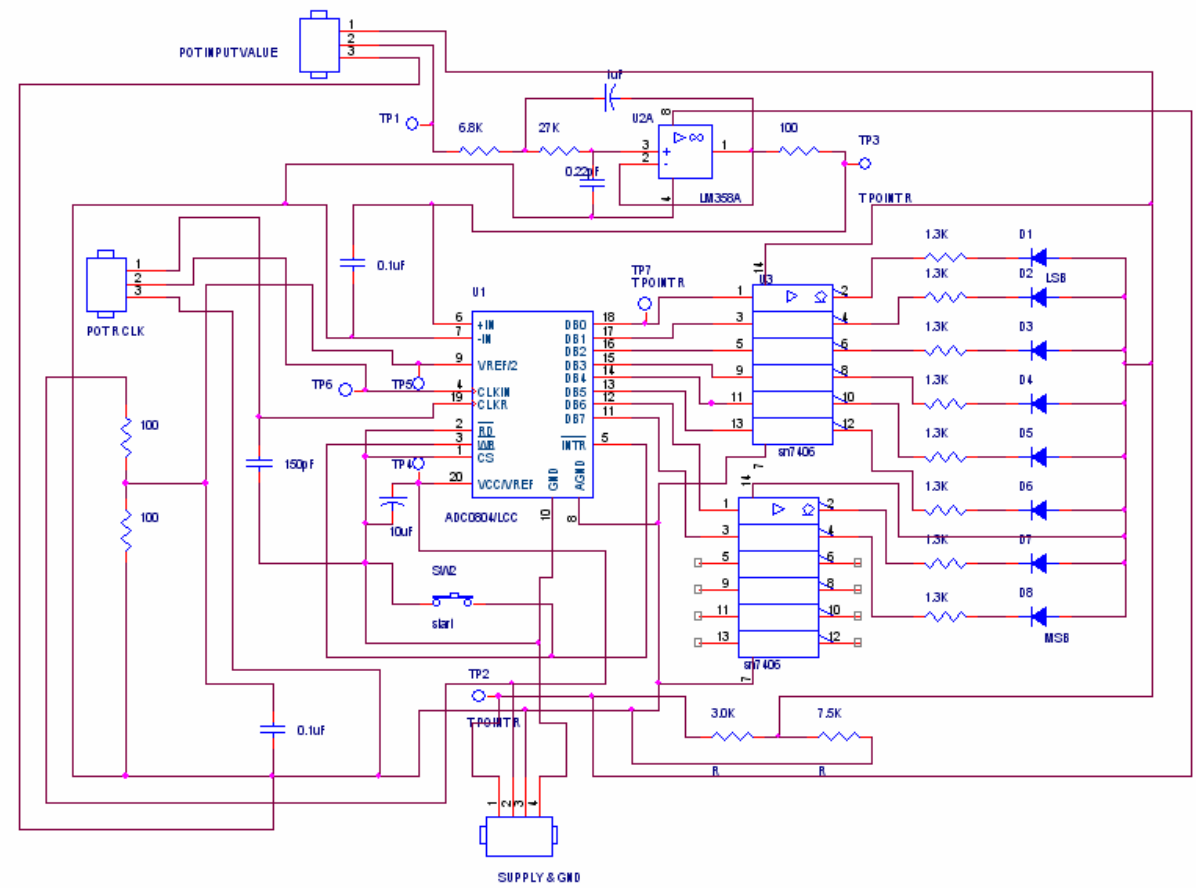

Figure 3.6: Schematic Diagram for the Design of Test Circuit Board for ADC0804LCN IC Chip.

All the circuits are connect using bread board before build properly on PCB, the picture of test circuit on bread board is shown in figure 3.7.

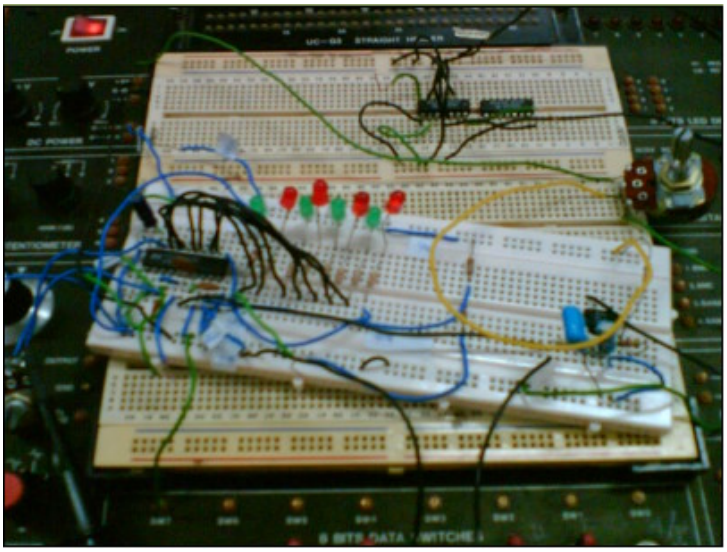

Figure 3.7: Test Circuit on Bread Board.

CHAPTER 4: DRAWING AND BUILT PRINTED CIRCUIT BOARD (PCB) FOR TEST CIRCUIT BOARD.

4.0 Introduction of OrCAD software.

The characterize board of analog to digital converter (ADC) IC chip are designed using OrCAD Family Release 9.2 software that fully owned by Cadence Design System Software. This software useful to design circuit and yield printed circuit board (PCB).

The schematic circuit is drawing using OrCAD Capture CIS. This software complete with variety of electronics component in the software library. That will make users draw the circuits easily.

4.1 Design Principle use OrCAD software.

To start drawing circuit use this software, firstly go to OrCAD Family Release 9.2 and select Capture CIS. Then follow the instruction below:

- Go to menu bar select File → New → Design.
- Go to Place → part (Place Part window will appear). → Go to Add library, select all then open.
- Start draw schematic refer from the design until finish.
- Select power pin visible by double click to each component on the circuit. Then connect all power pin and ground.
- Insert footprint for all component:
  - Go to OrCAD Family Release 9.2 at program file, and then select Layout Plus.
  - Go to menu bar select File → New → Cancel.
  - Go to menu file and select library manager.
  - Select code of footprint that suitable for place component.
- To insert footprint to the component, by double click on one component and select footprint then insert the footprint code into the space provide. The selected footprint for the design ADC test circuit board as shown in the Table 4.1: