UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Kedua

Sidang Akademik 2002/2003

Februari/Mac 2003

JEE 241 – Elektronik Analog I

Masa : 3 Jam

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi **TIGA BELAS (13)** muka surat bercetak dan **ENAM (6)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **LIMA (5)** soalan.

Agihan markah diberikan di sut sebelah kanan soalan berkenaan.

Semua soalan hendaklah dijawab di dalam Bahasa Malaysia.

...2/-

1. (a) Jelaskan apakah kepentingan titik Q di dalam rekabentuk litar penguat menggunakan transistor jenis BJT ataupun FET.

Explain the importance of the Q-point in amplifier circuit design using transistor device such as BJT or FET.

(10%)

(b) Bagi litar di dalam Rajah 1(b), tentukan nilai I_B, I_C, V_E, dan V_{CE}.

For the circuit network in Figure 1(b), determine I_B, I_C, V_E, and V_{CE}.

(30%)

(c) Tentukan nilai V_E dan I_E bagi litar di dalam Rajah 1(c).

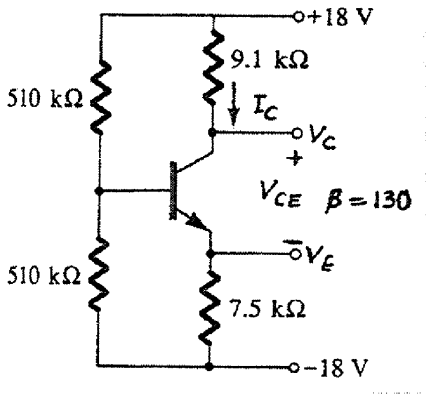
Find the values of V_E and I_E for the circuit in Figure 1(c).

(30%)

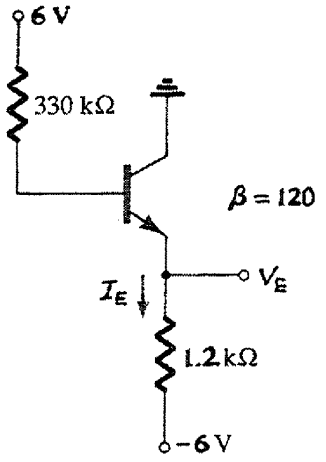
(d) Reka sebuah litar penstabil-pemancar (*emitter-stabilised*) dengan nilai $I_{CQ} = ½ I_{Csat}$, dan $V_{CEQ} = ½ V_{CC}$. Gunakan $V_{CC} = 20V$, $I_{Csat} = 10\ mA$, $\beta = 120$, dan $R_C = 4R_E$. Gunakan nilai yang piawai.

Design an emitter-stabilised network at $I_{CQ} = ½ I_{Csat}$, and $V_{CEQ} = ½ V_{CC}$. Use $V_{CC} = 20V$, $I_{Csat} = 10\ mA$, $\beta = 120$, and $R_C = 4R_E$. Use standard values.

(30%)



Rajah 1(b)
Figure 1(b)



Rajah 1(c)
Figure 1(c)

2. (a) Jelaskan perbezaan operasi peranti FET jenis *Depletion-MOS* dan *Enhancement MOS.*

Describe the difference in the operation of a Depletion MOS and Enhancement MOS for an FET type device.

(30%)

(b) Tentukan nilai V_o bagi litar di dalam Rajah 2(b), sekiranya $y_{os} = 20\ \mu S$.
Determine V_o for the network of Figure 2(b), if $y_{os} = 20\ \mu S$.

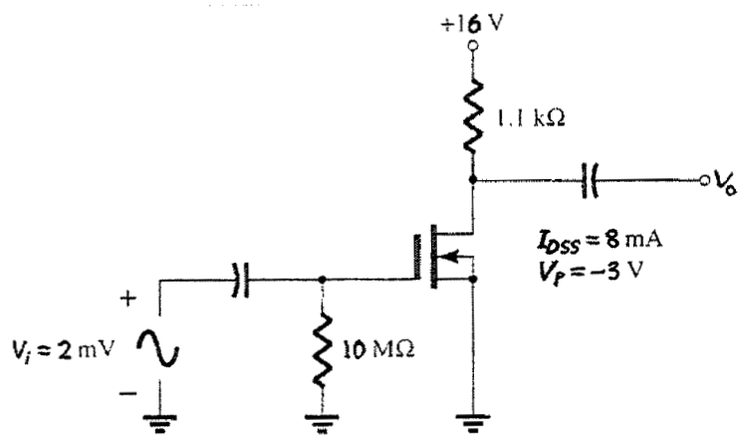
(20%)

(c) Tentukan nilai Z_i, Z_o dan A_v bagi penguat di dalam Rajah 2(c), sekiranya $k = 0.3 \times 10^{-3}$.

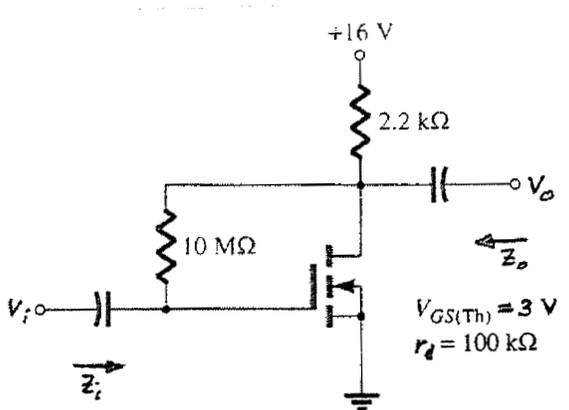
Determine Z_i, Z_o, and A_v for the amplifier of Figure 2(c), if $k = 0.3 \times 10^{-3}$.

(50%)

...4/-



Rajah 2(b)
Figure 2(b)



Rajah 2(c)
Figure 2(c)

3. (a) Huraikan jenis litar padanan yang boleh digunakan di antara bahagian-bahagian litar penguat berbilang peringkat.

Describe the type of coupling circuits that can be used between the stages of a multistage amplifier circuit.

(15%)

(b) Bagi litar sistem berturut seperti di dalam Rajah 3(b), dengan kedua-dua peringkat yang sama, tentukan:

For the cascaded system of Figure 3(b), with two identical stages, determine:

[I] Gandaan voltan terbeban bagi setiap peringkat
The loaded voltage gain of each stage

[ii] Gandaan voltan total bagi sistem, iaitu A_V dan A_{VS}
The total gain of the system, A_V and A_{VS}

[iii] Gandaan arus terbeban bagi setiap peringkat
The loaded current gain of each stage

[iv] Gandaan arus total bagi sistem
The total current gain of the system

[v] Bagaimanakah Z_i terkesan oleh peringkat kedua litar dan R_L
How Z_i is affected by the second stage and R_L

[vi] Bagaimanakah Z_o terkesan oleh peringkat pertama litar dan R_S
How Z_o is affected by the first stage and R_S

[vii] Kaitan fasa antara V_o dan V_i
The phase relationship between V_o and V_i.

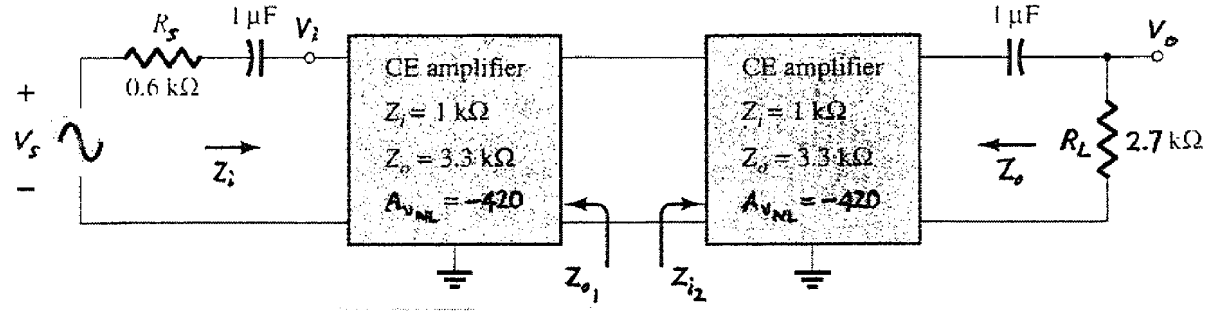
(50%)

(c) Bagi penguat berturut seperti di dalam Rajah 3(c), tentukan nilai voltan pincang arus terus (AT) dan arus pengumpul bagi setiap peringkat.

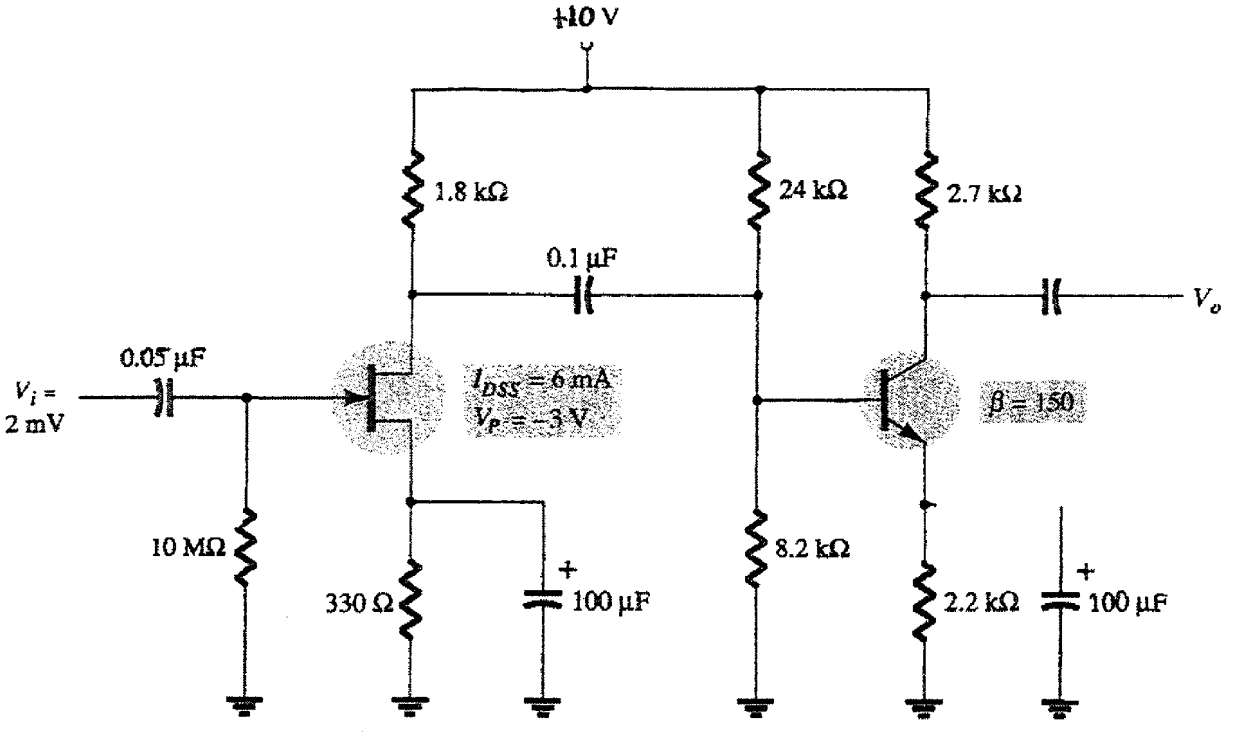
For the cascade amplifier of Figure 3(c), calculate the dc bias voltages and collector current of each stage.

(35%)

...6/-



Rajah 3(b)
Figure 3(b)



Rajah 3(c)
Figure 3(c)

...7/-

4. (a) Terbitkan rumus yang bersesuaian bagi kuasa masukan, kuasa keluaran dan kecekapan bagi litar penguat kuasa jenis kelas B.

Derive the relevant formula for the value of input power, output power and efficiency of a class B power amplifier circuit.

(25%)

(b) Bagi litar penguat-kuasa kelas B dengan V_{CC} = *30V*, dan memacu beban bernilai *16* Ω, tentukan nilai maksima bagi kuasa masukan, kuasa keluaran dan lesapan transistor.

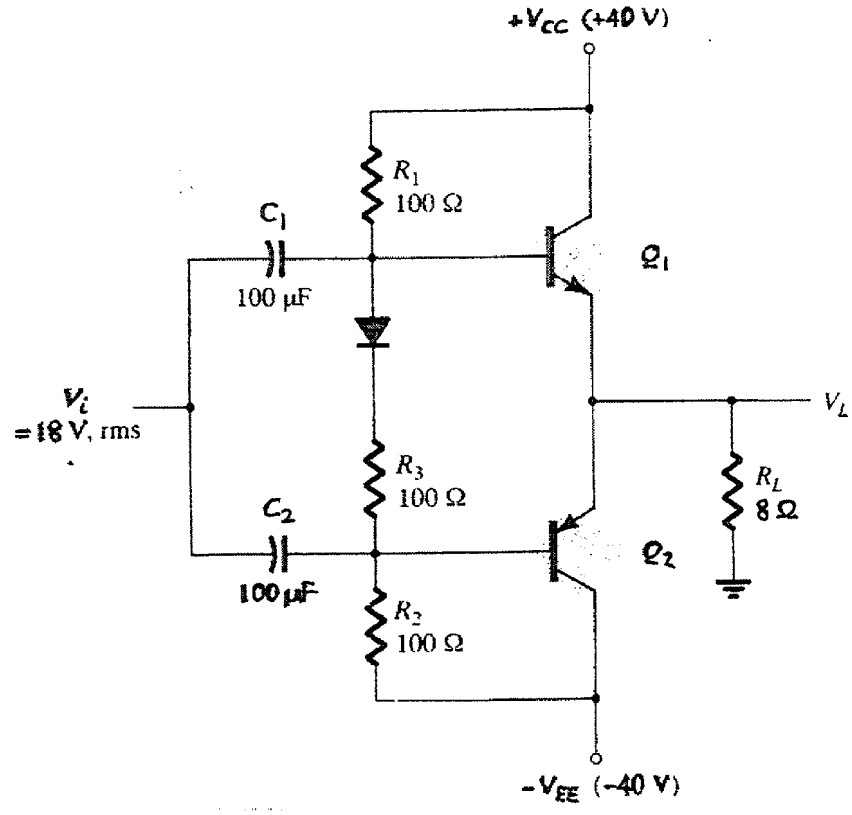
For a class B amplifier using a supply of V_{CC} = *30V, and driving a load of 16* Ω, *determine the maximum input power, output power and transistor dissipation.*

(35%)

(c) Bagi litar penguat-kuasa di dalam Rajah 4(c), tentukan nilai $P_O(ac)$, $P_i(dc)$, $\%\eta$ dan lesapan kuasa oleh kedua-dua transistor.

For the power amplifier of Figure 4(c), calculate $P_O(ac)$, $P_i(dc)$, $\%\eta$ *and power dissipated by both output transistors.*

(40%)



Rajah 4(c)
Figure 4(c)

5. (a) Apakah keperluan analisa frekuensi lakukan di dalam rekabentuk litar penguat?

What is the benefit of conducting the frequency analysis in amplifier circuit design?

(5%)

(b) Tentukan nilai potong frekuensi rendah bagi litar Rajah 5(b), menggunakan parameter-parameter berikut:
Determine the lower cutoff frequency for the network of Figure 5(b), using the following parameters:

$C_G = 0.01\ \mu F$, $C_C = 0.5\ \mu F$, $C_S = 2\ \mu F$, $R_{sig} = 10\ k\Omega$, $R_G = 1\ M\Omega$, $R_D = 4.7\ k\Omega$, $R_S = 1\ k\Omega$, $R_L = 2.2\ k\Omega$, $I_{DSS} = 8\ mA$, $V_p = -4V$, $r_d = \infty\ \Omega$, $V_{DD} = 20\ V$

Lakarkan juga sambutan frekuensi menggunakan plot Bode.
Sketch the frequency response using a Bode plot.

(45%)

(c) Bagi litar di dalam Rajah 5(c),
For the network of Figure 5(c),

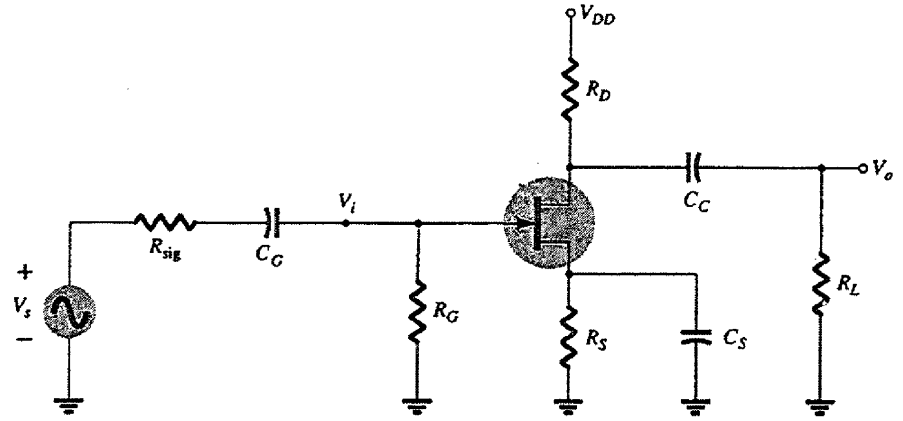
[i] Tentukan nilai f_{Hi} dan f_{Ho}
Determine f_{Hi} and f_{Ho}

[ii] Andaikan bahawa $C_{b'e} = C_{be}$ dan $C_{b'c} = C_{bc}$, tentukan f_β dan f_T
Assuming that $C_{b'e} = C_{be}$ and $C_{b'c} = C_{bc}$, find f_β and f_T

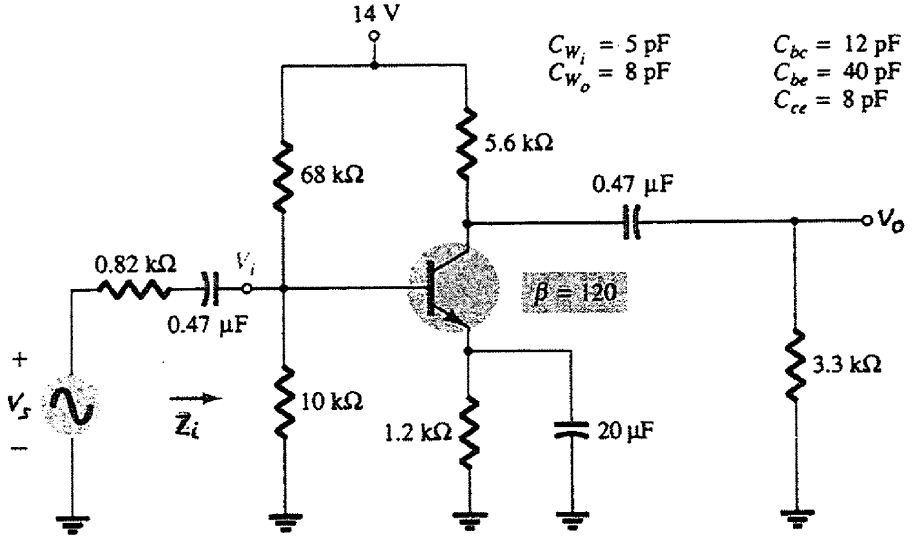
[iii] Lakarkan sambutan frekuensi bagi kawasan frekuensi tinggi dengan menggunakan plot Bode dan tentukan frekuensi potong yang sesuai.

Sketch the frequency response for the high-frequency region using a Bode plot and determine the cutoff frequency.

(50%)



Rajah 5(b)
Figure 5(b)



Rajah 5(c)
Figure 5(c)

6. (a) Bagi litar di dalam Rajah 6(a), tentukan nilai; I_B, I_C, r_e, Z_i, Z_o, A_v dan A_i.

For the network of Figure 6(a), determine; I_B, I_C, r_e, Z_i, Z_o, A_V and A_i.

(30%)

...11/-

(b) Bagi litar konfigurasi tapak sepunya di dalam Rajah 6(b);
For the common-gate configuration of Figure 6(b);

(40%)

[i] Tentukan nilai A_{VNL}, Z_i dan Z_o.
Determine A_{VNL}, Z_i and Z_o.

[ii] Lakar model dua port yang sesuai bagi litar dengan parameter-parameter dari bahagian (i).
Sketch a suitable two-port model with the parameters determined in part (i) in place.

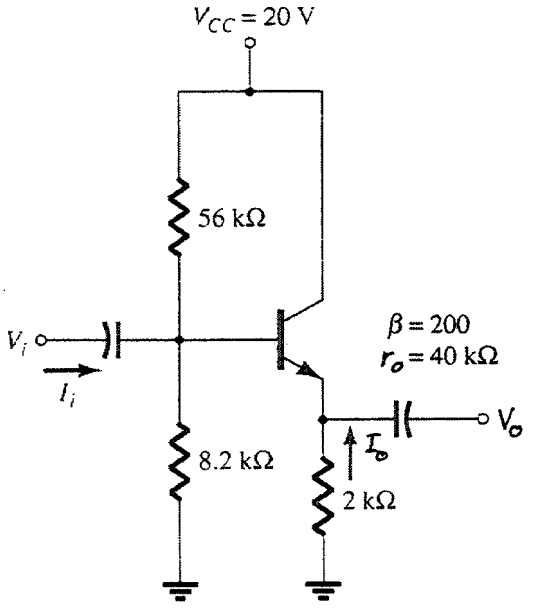
[iii] Tentukan nilai A_V dan A_{VS}
Determine A_V and A_{VS}

[iv] Tukar nilai R_L kepada 2.2 kΩ dan kira nilai A_V dan A_{VS} yang diperolehi. Apakah kesan penukaran nilai R_L kepada gandaan voltan?

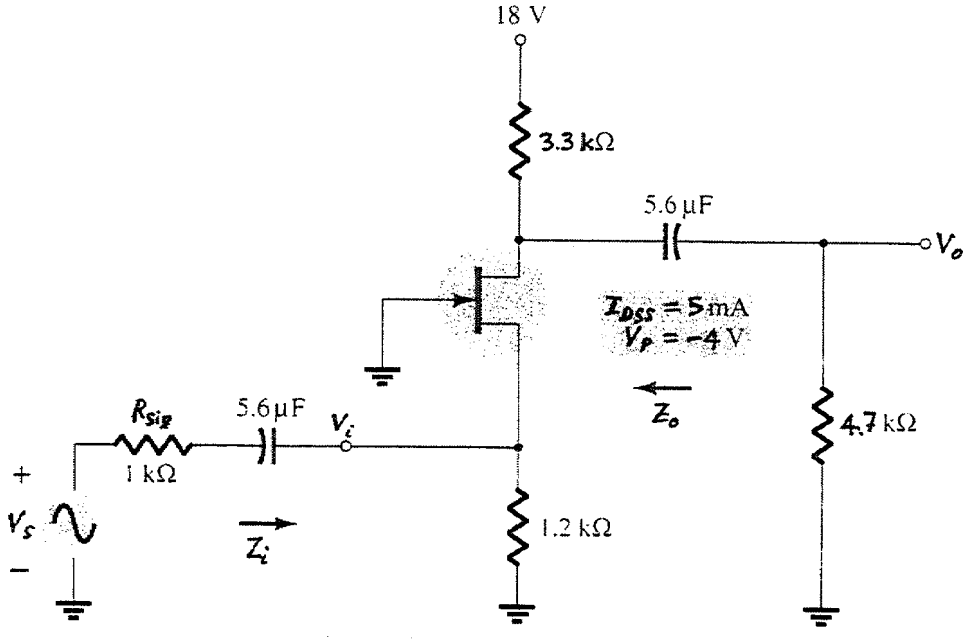
Change R_L to 2.2 kΩ and calculate A_V and A_{VS}. What was the effect of changing R_L on the voltage gains?

(c) Reka sebuah litar pincang tetap seperti Rajah 6(c) dengan nilai gandaan 10.
Design the fixed-bias network of Figure 6(c) to have a gain of 10.

(30%)

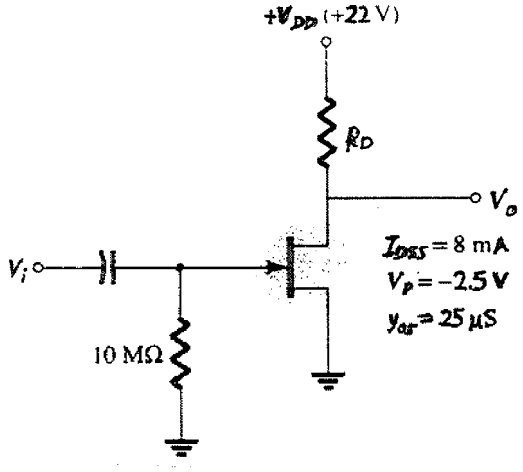


Rajah 6(a)
Figure 6(a)



Rajah 6(b)
Figure 6(b)

...13/-



Rajah 6(c)
Figure 6(c)

- oo0oo -