SCALABLE FABRICATION OF NICKEL MICROPILLARS USING ULTRA-VIOLET PHOTOLITHOGRAPHY PROCESS FOR MICROELECTRONICS APPLICATION

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Declaration

I, Rais Bin Ahmad Taufik, hereby declare that I am the sole author of this thesis and that neither any part of this thesis nor the whole of this thesis has been submitted to any other University or institution for any level of education.

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List of Abbreviations

3D IC	Three Dimensional Integrated Circuit
2.5D IC	Two point Five Dimensional integrated Circuit
2D IC	Two Dimensional Integrated Circuit
TSV	Through Silicon Via
IMC	Intermetallic Compound
Cu	Copper
Pb	Lead
Sn	Tin
Ni	Nickel
IoT	Internet of Things
AI	Artificial Intelligence
IR 4.0	Industry Revolution 4.0
PMOS	p-type metal oxide semiconductor

NMOS	n-type metal oxide semiconductor
JMOS	Joint Metal Oxide Semiconductor
F2F	Face-to-Face
F2B	Face-to-Back
B2B	Back-to-Back
SoC	Systems-on-Chip
CIS	CMOS image sensor
DRIE	Deep Reactive Ion Etching
CMP	Chemical Mechanical Polishing
LIL	laser interference lithography
LIGA	Lthographie, Galvanoformung, Abformung
UV	Ultraviolet
TEM	Transmission Electron Microscopy
SEM	Scanning Electron Microscopy
EDS	Energy Dispersive X-ray Spectroscopy
DC	Direct Current

Abstract

In the world of semiconductors and microelectronics, a trend to vertically stack integrated circuits are highly been used as it can meet the electronic device requirements. This stacking system technology can perform better performance, increase the functionality, reduce power consumption and also reduce in size with smaller footprint. There are some methods and processes need to go through in order to achieve the stacking technology that are called 3D integration technologies which addresses Moore law to fit in more ICs/transistors in a smaller area (chip).

The overall of this project is being conducted is to develop nickel micropillar on copper substrate by conducting UV lithography of thick SU-8 photoresist pair with nickel electroforming method. Both experimental methodology was conducted step by step in order to study the physio-chemical characterization of the nickel micropillar as a solder interlayer between copper and microbumps to reduce intermetallic compounds to enhance the reliability of joints. This research covers the Ni micropillars just beneath the microbumps. The size of the designed micropillar were within 2 to 80 μm with highest thickness can be achieved.

There are experimental methodology that need to conduct in sequence in order to achieve the objectives of this project. The process involved was lithography and nickel electrodeposition. Both this method are the requirement of this project since without the lithography process, there is no SU-8 PDMS mold, without the nickel electrodeposition, there is no growth of nickel form on the copper substrate. Microanalysis of the specimen was conducted by using Scanning Electron Microscopy (SEM) with the Energy Dispersive X-ray Spectroscopy (EDS). All the nickel physical behavior can be analyses through this process.

Abstrak

Di dunia semikonduktor dan mikroelektronik, trend litar bersepadu secara bertindih sangat popular digunakan kerana ia dapat memenuhi keperluan peranti elektronik. Teknologi sistem bertindih ini boleh meningkatkan prestasi kearah yang lebih baik, meningkatkan fungsi, mengurangkan penggunaan kuasa dan juga mengurangkan saiz kearah yang lebih kecil. Terdapat beberapa kaedah dan proses yang perlu dilalui untuk mencapai teknologi bertindih yang dipanggil teknologi integrasi 3D.

Keseluruhan projek ini dijalankan adalah untuk membangunkan micropillar nikel pada substrat tembaga dengan menggunakan kaedah litografi UV keatas permukaan photoresist SU-8 yang tebal dengan kaedah electroforming nikel. Kedua-dua metodologi eksperimen dijalankan secara berturut-turut untuk mengkaji tingkah laku fizikal nikel micropillar. Saiz micropillar yang direka adalah di antara 2 μm hingga 80 μm dengan ketebalan maksimum yang dapat dicapai.

Terdapat metodologi eksperimen yang perlu dijalankan mengikut turutan untuk mencapai matlamat projek ini. Antara proses yang terlibat adalah proses litografi UV dan elektrodeposisi nikel. Kedua-dua kaedah ini adalah keperluan untuk projek ini kerana tanpa proses litografi UV, tidak akan ada acuan PDMS SU-8, tanpa elektrodeposisi nikel, tidak akan ada pertumbuhan micropillar nikel pada substrat tembaga. Mikroanalisis spesimen dijalankan dengan menggunakan Mikroskopi Pengimbasan Elektron (SEM) dengan Spektroskopi X-ray Dispersif Tenaga (EDS). Semua tingkah laku fizikal nikel boleh dianalisis melalui proses ini.

Chapter 1 Introduction

1.1 Introduction

In this high technology world, the pattern of demands on electronics highly increased with the latest development of technology. People now looking forward for smallest technology as it is very easy and convenient to carry around. In order to fulfil all the demand mention, semiconductor industries are all committed to develop a small with multifunctional merchandise to attract consumers and increase its competitiveness. All semiconductor industries now focusses on producing high density of transistor inside the chip with small size of node to improve the performance of IC chip.

Three Dimensional Integrated Circuit is a stacking of silicon dies onto a 2D package and vertically interconnect those through-silicon-vias (TSV). It behaves as a single device in order to achieve high performance improvements with a small form factor by increasing I/O density and shortening interconnect distance. In fact, 3D IC is one of a host of 3D integration schemes that introduced z-direction in order to achieve electrical performance benefits.

3D ICs promise in many significant benefits such as smaller footprint that function to produce tiny devices with powerful behavior, reduce the fabrication cost as decreasing the size of dies, shorter interconnect in term of average wire length is being reduced, can reduce power consumption used by keeping a signal on a chip.

Through Silicon Via (TSV) act as the heart of 3D IC integration as it provides the opportunity for the shortest chip-to-chip interconnects. If TSV is being compared with other interconnection technologies like wire bonding, TSV benefits a lot as it can perform a better

electrical performance, its generate lower power consumption, has a wider data width and bandwidth, consist of high density and lighter in weight with smaller form factor.

TSV is then connected to chips layer with the help of an interface material known as microbumps. As it is depicted in the Figure 1-1, the arrangement of TSV, microbumps and how they are connected are shown. The Synchrotron radiation topography image also shows a bared metal only interface of the materials which helps to understand actual arrangement of these components.

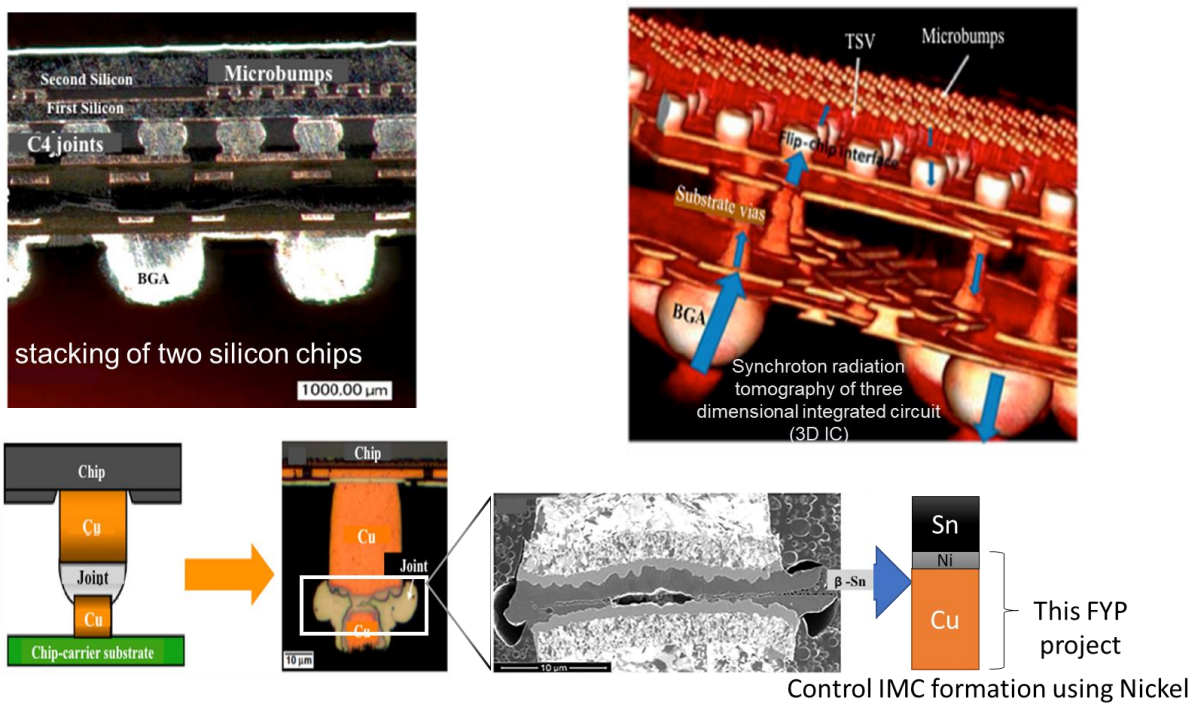

Figure 1-1: Illustration of 3D-IC, TSV, and microbumps in a typical silicon board with several chips

Due to the nature of solder joints when exposed to Cu, an intermetallic material (IMC) layer is developing at the interface. This intermetallic layer can brittle and lead to infant failure of microelectronic usage. The IMC formation is usually accelerated due to electromigration and thermomigration which are in effect when the chip is in used, or when a neighbor chip is

producing heat and due to heat conduction the heat will be pass on to the other chip through TSV and microbumps. Therefore, in this study a layer of nickel has been introduced to very interface of solder microbumps to decelerate such IMC formation. Hence, it will increase the reliability of the 3D-IC.

1.2 Project Background

In the era of global industry transformation to the fourth generation of industry which has been brought into attention of Malaysia economic development plan is embracing industry 4.0 element into effect. Through this, rise of broadband and mobile connectivity, Internet of Things (IoT), robotics and Artificial Intelligence (AI), Labs and companies produce machines or software with increasing human-like capabilities. The most important part of embracing IR 4.0 is to have reliable electronic devices which dimensional size are continuously become smaller from 2D into 3D stacking chips but still possesses reliability issues. Nowadays, in the era of progressive grow of electronic technology, the advanced circuit packaging called three-dimensional integrated circuits (3D ICs) has increased the capability to assemble many miniaturization chips in one single substrate. Despite on the advanced packaging of 3D ICs, the shrinking in size of it causes inevitable formation of intermetallic compounds (IMCs) in smaller solder joint called microbumps. The IMCs formation within the microbump has been associated by the thermomigration and electromigration affects that usually occurred in normal flip chip solder in two-dimensional integrated circuits (2D ICs). This requires to study the formation of asymmetrical IMCs by means of thermomigration and electromigration in microbumps by investigating the selection of metallurgical configuration as to reduce the IMCs formation.

1.3 Problem Statement

The existing of three dimensional integrated circuits (3D ICs) are currently being developed to improve the 2D designs by providing smaller chips areas and higher performance and lower power consumption. However, it causes inevitable formation of intermetallic compounds in smaller solder joint called microbumps. Microbump have attracted lots of attention as it can form the high density interconnection with low cost. The main problem of Cu-Ni IMC based microbump in 3D-ICs is it has low mechanical properties.

1.4 Objectives

- To produce nickel micropillar interlayer on the copper substrate
- To study the physio-chemical characterization of the nickel micropillar

1.5 Scope of Work

In order to achieve this project's objective, the following scope of work need to be done. The scope of work is as follow:

1. Understand how does 3D ICs works
2. Identify the properties of Cu-Ni in Intermetallic Compounds
3. Study the phenomenon of microbump and kirkendall voids
4. Conduct an experiment to identify the physical behavior of nickel micropillar.

Chapter 2 Literature Review

2.1 Three Dimensional Integrated Circuit

In 1962, methods of vertically interconnect circuits were first proposed during the earliest integration circuits. William Shockley and Richard Feynman are some of the most prominent engineers and scientist that are very supportive when vertical integration was proposed. This vertical integration as illustrated in Figure 2-1 were appreciated by industry as early as 1960s. However not all developer followed this 3D integration production as the evolution of planar processes yielded the desired improvements in transistor density, speed, and power in integrated circuits with a commensurate decrease in manufacturing cost.

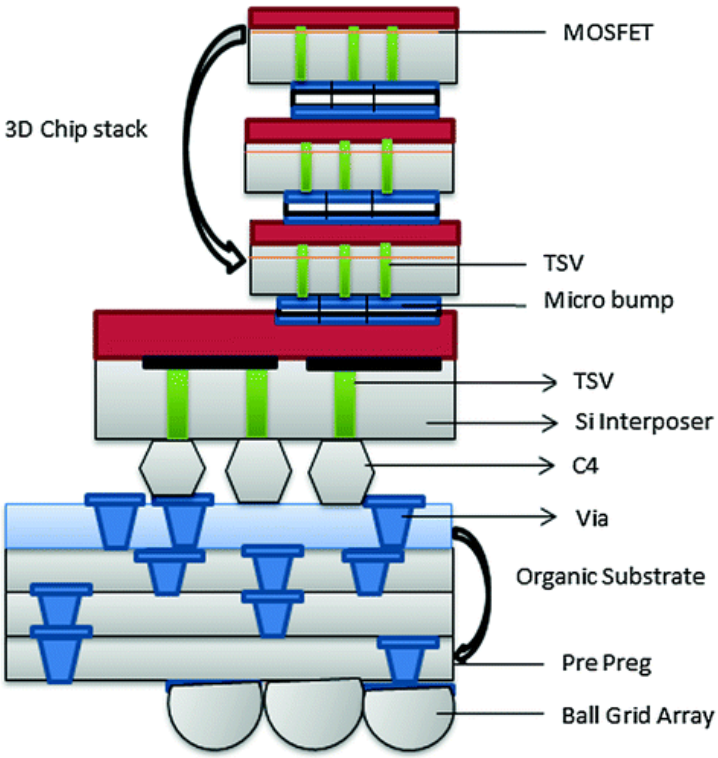

Figure 2-1: Schematic diagram of a 3D-IC with multiple chip stacks [1]

Vertical integral consist 3-D CMOS inverters, where the p-type metal oxide semiconductor (PMOS) and n-type metal oxide semiconductor (NMOS) transistors share the same gate,

greatly reducing the total area of an inverter [2]. Joint Metal Oxide Semiconductor (JMOS) term was used in these structures to describe the joint use of a single gate for both devices. Infrared detectors are some of examples of early uses of 3-D integration where the infrared detectors were manufactured in exotic materials such as mercadmium telluride or indium phosphate, were flipped and bonded to silicon-based detector readout circuits.

Due to the increasing importance of interconnect and the demand for greater functionality on a single substrate, the concept of vertical integration has been revived and has become a prominent topic of research and commercial development since 2000s. 3-D integration has evolved into a design paradigm manifested at many abstraction levels, such as the package, die and wafer. 3-D technology act as a systems integration platform yields significant improvements in transistor density, performance, heterogeneity, form factor, and cost.

3D integrated circuit is the high performance and downsizing technology by the utilization of stacking of silicon wafer or dies vertically by through-Si-Via (TSV) and solder microbumps. The not exact prediction of Moore's law due to physical limitation as well as economic constraints has cause this stacking of chip vertically has been introduced [3]3D integration with TSV can perform a system level integration with smaller package size, higher interconnection density, and better performance [4]. There are several key technologies required to achieve 3D IC integration such as through silicon via (TSV), wafer thinning, and handling as well as wafer/chip bonding.

Three Dimensional circuits can be conceptualized as the bonding of multiple wafers or bare dice. Vertical interconnect are the differences between a SiP and a 3D ICs. Different bonding styles between the planes within a 3D system are also possible Face-to-Face (F2F), Face-to-Back (F2B), and Back-to-Back (B2B) [5].

2.2 Opportunities For three-dimensional integration

The existence of 3-D integration has reduced the length of the longest interconnects across an integrated circuit. 3D IC is very important in electronic device since it act as an amplifier, oscillator, timer, counter, computer memory or microprocessor.

This 3D integrated circuit will improve packing density as it is very small in shape, better noise immunity, reduced power consumption, and faster speed due to reduced wire length/lower wire capacitance. 3D ICs are promising for the heterogeneous integration of different technologies (logic, memory, RF, analog, etc) which would enable better high performance and compact SoCs.

The 3D-IC based systems provides the capability to include disparate technologies, greatly extending the capabilities of modern systems-on-chip (SoC) [6]. The feature of 3D-IC offers unique opportunities for highly heterogeneous and sophiscticated systems [7].

2.3 Microbump

Due to high demand of high performance and high density application of 3D ICs , a fine pitch microbump was developed in order to meet the requirement of low profile, light weight, and high pin counts for 3D IC integration applications [8]. This microbump technology involves the use of solder or gold bumps on the surface of the die to make connections [9]. The mechanical stresses of assembly are much lower than with wire bonding, so pads require only the top or sometimes top two layers, leaving lower layers free for routing or for devices. A layer of microbumps bond each die carrier tier to an epoxy routing tier that brings signal to the edges of the cube. After that, it will laminate the tiers into a single stack and add metallization to the sides to connect the routing tiers. 3D package does not significantly reduce parasitic capacitances because a microbump bonded cube must still route signals to the periphery before sending them back to the destination inside the cube.

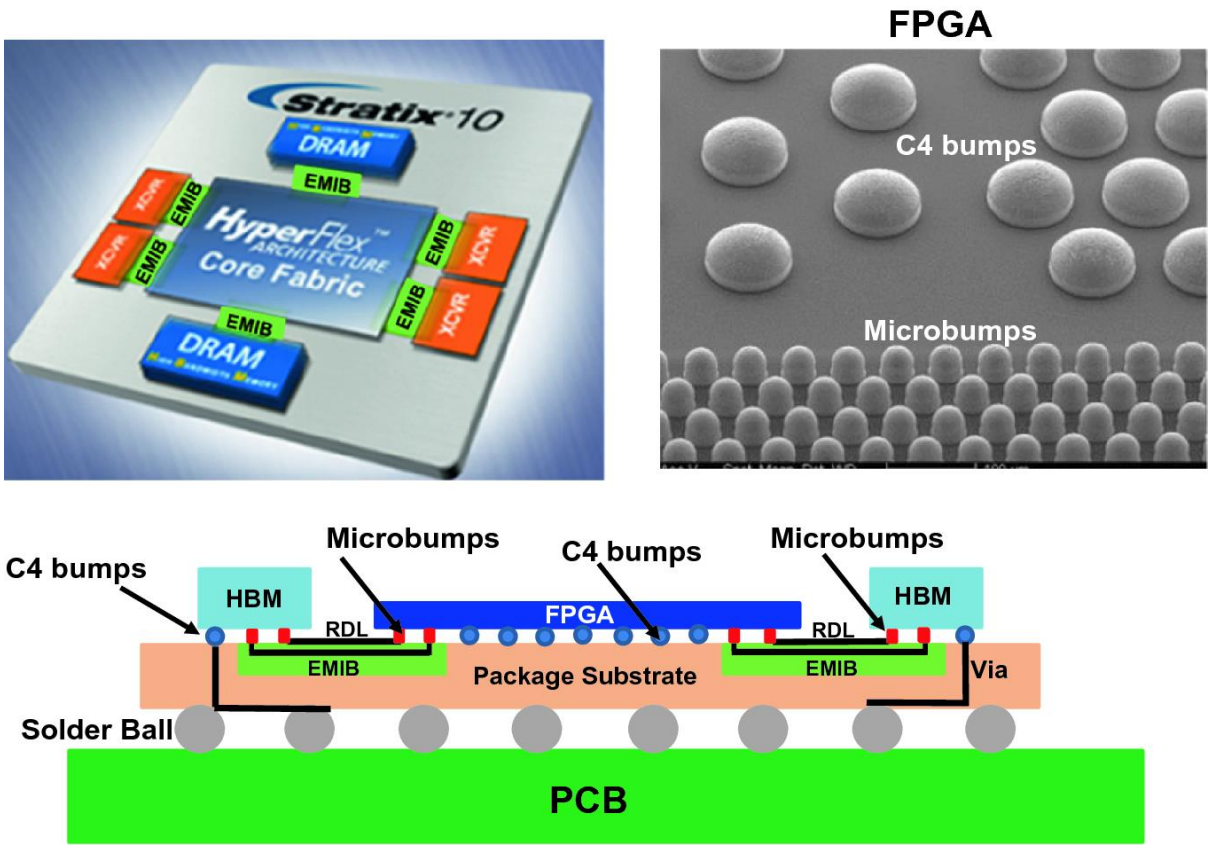

Figure 2-2: Schematic illustration and SEM micrograph image of solder bumps on a chip surface [10]

The intermetallic compounds (IMCs) of Cu6Sn5 usually form during interfacial reactions at the Sn-based solder/Cu interface [11]. The joints are composed mostly of Cu-Sn IMCs because of the small size of microbumps [12]. Figure 2-2 shows the variance type and size of microbumps in manufacturing of 3D IC world. Research found that after multiple or long-time reflows in these microbumps, the IMCs join causing an impingement phenomenon, and the crystals tend to grow in a homogenous direction and the properties of IMCs such as grain structure, toughness and voids may dominate joint reliability in 3D-IC technologies [13]. Crack propagation will occur in this structure through the IMCs under impacts [14]. The wire between tiers can be shorten and performance by reducing parasitics can be improve by using face to face microbump technology

2.4 Through Silicon Via

In order to achieve 3D and 2.5D IC integrations, there are several keys technologies required such as through-silicon via (TSV), wafer thinning and handling as well as wafer/chip bonding. 3D ICs that consist of through-silicon Via had this advantages of higher interconnection density, can improve the performance and at the same time can perform system level integration with smaller package size [15]. TSV considered as the heart of 3D integration because it provides the advantages of shortening interconnection path and thinner package sizes. There are three types of TSV formation during 3D IC process which is when TSV is formed before CMOS processes, the process progression is defines as via first. Then, in via middle flow, backend process only continues after the completion of TSV process and the final scheme is via last where TSV is fabricated from the front side of wafer once going through the CMOS processes. All the TSV schemes choices based on the final application requirement in the semiconductor industry itself.

MEMS, mobile phone, CMOS image sensor (CIS), bioapplications devices and memory products are some product example using this TSV technology. With the relatively high fabrication cost, TSV implementation in 3D IC and advanced packaging application is not generally implemented yet [16] [17]. TSV fabrication is the key technology to permit communications between various strata of the 3D integrated system. There are various important process of TSV such as via formation by deep reactive ion etching (DRIE), lining with dielectric layer, barrier and seed layers, via filling, chemical mechanical polishing (CMP) and Cu revealing process.

2.5 Intermetallic Compounds

In Three Dimensional Integrated Circuit, Cu-Sn IMCs bonding was used as interconnection material. Micro bumps and through-silicon-via (TSVs) vertical interconnect structures are used to stack Si chips in 3D integrated circuits packaging, and the highly reliable interconnect is

achieved by forming intermetallic compounds (IMCs) at the interface [18]. Sn-based solder alloys are reflowing in an isothermal oven and would react with metallization layers to form intermetallic compounds (IMC) during soldering. The quality of interfacial IMCs as illustrated in Figure 2-3 are critical for the reliability of solder joints because of the brittleness and higher electrical resistivity of IMCs [19].

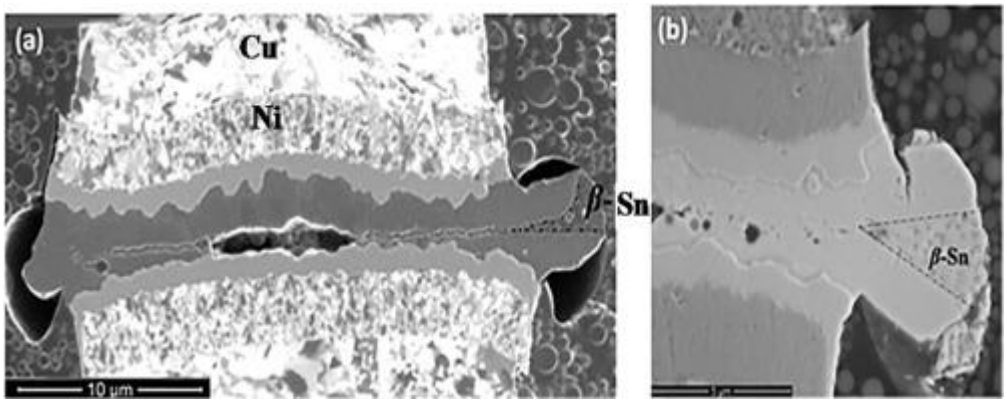

Figure 2-3: IMC growth in a microbump solder joint [20]

The growth of IMCs between the solder and substrate give big impact on the reliability of smaller solder sizes in3D ICs [3]. Copper (Cu) and tin (Sn) based alloy with more than 97wt% Sn metal configuration are the most popular metallurgy of Pb free solder microbumps. This IMCs configuration of soldered microbumps usually involves heating, reflow and solidification. There are some reliable data published on Cu-Sn IMC growth rates below 100°C and this is because of the low growth rates at these temperatures and the difficulty of measuring thin, irregular IMC layers [21]. Cu-Sn IMCs are brittle and if present in large amounts at the solder / substrate interface, they may reduce the lifetime of the joints [22]

2.6 Kirkendall Void

3D IC has reduced the size of electronic components and at the same time the solder joints is being continuously scaled down. It cause the electromigration has a remarkable effect on the initiation and propagation of Kirkendall voids. This voids are generated at the solder/Cu

interface and deteriorate the reliability of the solder joint under impact or shock loads [23]. Electromigration (EM) is considered inevitable on the reliability of the in-chip interconnects in ultra large scale integration device. EM induced Kirkendall voids occurred at the Cu/Cu3Sn compound interface [24]. Kirkendall voids are often found in the inter diffusion zone of numerous diffusion couples as shown in Figure 2-3.

Soldering of Sn- containing alloys and Cu interconnection pads are widely used in microelectronic manufacturing [25]. Cu3Sn and Cu6Sn5 intermetallic compounds (IMCs) was formed during the metallurgical reactions and usually the formation of Cu3Sn layer is thin right after soldering. Microscopic of voids are formed and observed inside the Cu3Sn IMC and at the Cu/Cu3Sn interface after isothermal aging tests. Due to the voiding in Cu3Sn , it cause a significant degradation of solder joint reliability in board-level impact [26] and void-induced brittle failure at the solder/pad interface [27].

Kirkendall voids are voids that arise from the agglomeration of excess vacancies, as a result of the intrinsic diffusivity difference between the two diffusion species like Cu and Sn. However, kirkendall voids does not always occur in Cu-Sn binary diffusion couple. An observation of high voiding level in Cu3Sn on electroplated Cu interconnect pads

2.7 Lithography

Electron Beam Lithography and Ion Beam Lithography are the latest model that promises powerful technologies for prototyping, but both of them has some serious disadvantages which very expensive and slow in time [28]. There are some structuring technologies that had been considered to improve and to overcome the problems like self-assembly [29], nano-imprint lithography [30], two photon polymerization and laser interference lithography (LIL). However, all the advantages are stuck with higher cost lower throughput [31].

Laser Micromachining or LIGA Mems promises a better materials flexibility and 3-Dimensional capability than conventional UV lithography. LIGA is a German acronym for *Lithographie, Galvanoformung, Abformung* which means Lithography, Electroplating, and Molding that describe a fabrication technology used in order to produce high aspect ratio of microstructure [32]. There are two types LIGA fabrication technology which is X-Ray LIGA and UV Liga. X-ray is used in X-Ray LIGA to create high aspect ratio structure while UV LIGA uses ultraviolet light in order to create structures with relatively low aspect ratios [33].

Among all of lithography process, the most widely used photolithography technique today is Ultra Violet (UV) Lithography. UV lithography is the basic tools used in the exposure of microchip as it is the key to the age of micro- and nano-electronics [34]. UV lithography refers to a lithography process that uses ultraviolet light in order to form or project the pattern design on the photoresist through printing. The term UV lithography actually represent the two components of projection optics and lighting. The optimal lighting for the photomask was provided by the illuminator while the light source is a laser which guided through a special system of lenses and mirrors [35].

2.8 Electrodeposition of Nickel

In engineering world, Nickel are widely being used to coat other materials since Nickel has advantages in possesses good mechanical properties such as high hardness, corrosion resistance and magnetism [36]. Research shows that Nickel can protect Copper surface from corrosion to occur. Nickel coating has its own unique advantage since it can greatly broaden its applications such as anti-corrosion and anti- contamination materials.

Over decades, the study about electrodeposition of nickel has been intensely made in relation to its particular mechanical behavior and numerous application in industry [37]. Nickel

sulphate, nickel chloride and boric acid are some Watts electrolyte that widely been used in order to do nickel electrodeposition. Previous study explain that only nickel sulphamate solutions are the only alternative adopted on a substantial scale since the dominant position of Watts solutions in industrial processes has been challenged for many times [38].

Electrodeposition or electroplating is a relatively the easiest and inexpensive way of depositing thin and thick film under the good condition on conductive substrate without damaging the substrate. The typical setup that need to have when conducting a nickel electrodeposition is nickel (II) sulphate, sulphuric acid (H_2SO_4), DC power supply, crocodile clip, nickel plate and things to coat.

2.9 Microstructural analysis

In the early of 1930's and 1940's, the basic principle of the scanning electron microscope (SEM) were introduced by Knoll and continue by Von Ardenne in Germany and by Zworykin, Hillier and others in America [39]. The scanning electron microscope (SEM) is a microscope very well suited to the examination of surface by collecting secondary electrons emitted from the surface of the substrate.

Electron microscopy has been used to study neuronal ultrastructure since decades ago and found that from the first study using transmission electron microscopy (TEM) is used to analyses the synapses in the cerebral cortex [40, 41]. In fact that only electron microscopy is capable of seeing every axon, dendrite, and synaptic connection within a volume of neuropil.

The SEM are becoming a very useful and powerful research tool to analyses all the nanostructure behavior. Over these ten years, SEM technology benefited from considerable direct development investment, but also from apparently coincidental advances in vacuum engineering, nuclear physics, space technology, photography, radar, cryogenics and image

processing among others. By 1975, more than 1000 SEMs were installed in the USA alone, in all sizes from desk-top to the sophistication of stereoscan 180.

Energy Dispersive X-ray Spectroscopy (EDS) is a chemical analysis method than usually be paired with the electron beam based techniques of Scanning Electron Microscopy (SEM). EDS can perform elemental analysis in a very small areas as low as 1 nanometer diameter (STEM) if it combined with high resolution imaging tools like SEM [42]. EDS analysis usually used to determine the elemental composition of individual point, line scans and lateral distribution of elements from the imaged area. EDS is also being used by researchers as it is a qualitative and quantitative X-ray microanalytical technique that provide detailed information on the chemical composition of a sample for elements with atomic number [43].

Chapter 3 Research Methodology

In order to achieve all the objectives of this experiment, research methodology is carried out as it is the technique or method of every process applied. There are several steps need to follow accordingly from the very beginning till the end of the experimental as illustrated in Figure 3-1.

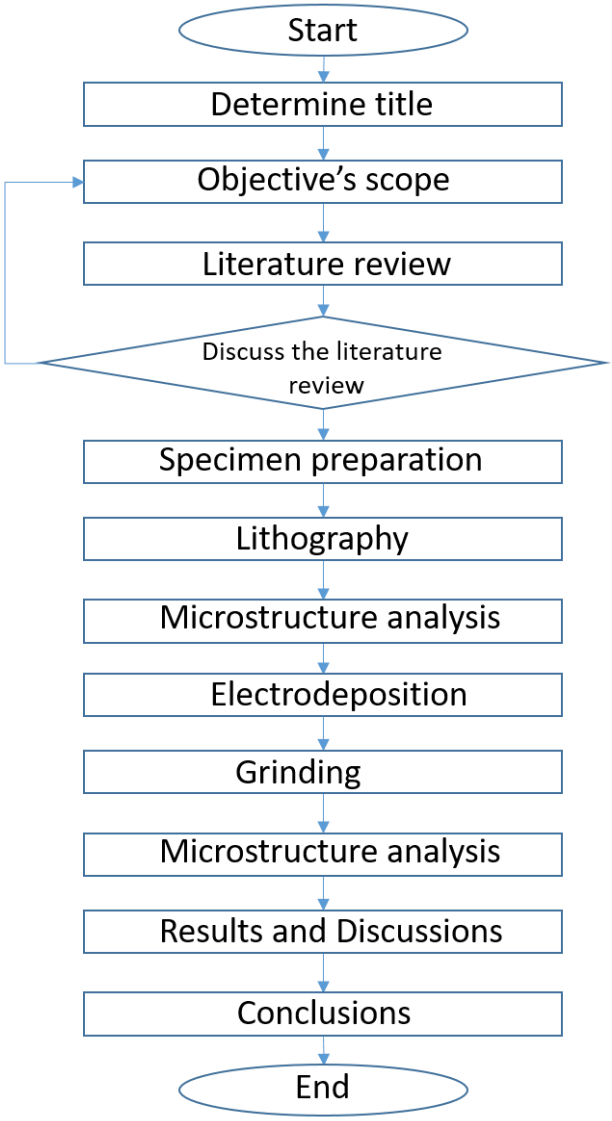

Figure 3-1: Research Methodology Steps

3.1 UV Lithography

Lithography is a process used in microfabrication to transfer geometric patterns to a film or substrate. Figure 3-3 illustrate on how actually the UV lithography is all about, the SU-8 negative photoresist will be expose to UV through emulsion mask and continue with development process to wash away the soluble photoresist There are several steps need to follow in order to transfer the pattern to the substrate. Figure 3-2 shows the 8 steps of UV lithography process.

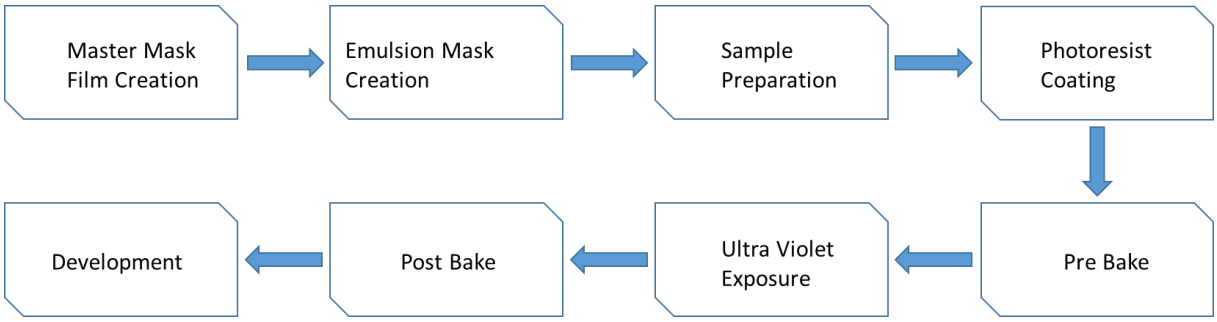

Figure 3-2: UV Lithography Steps

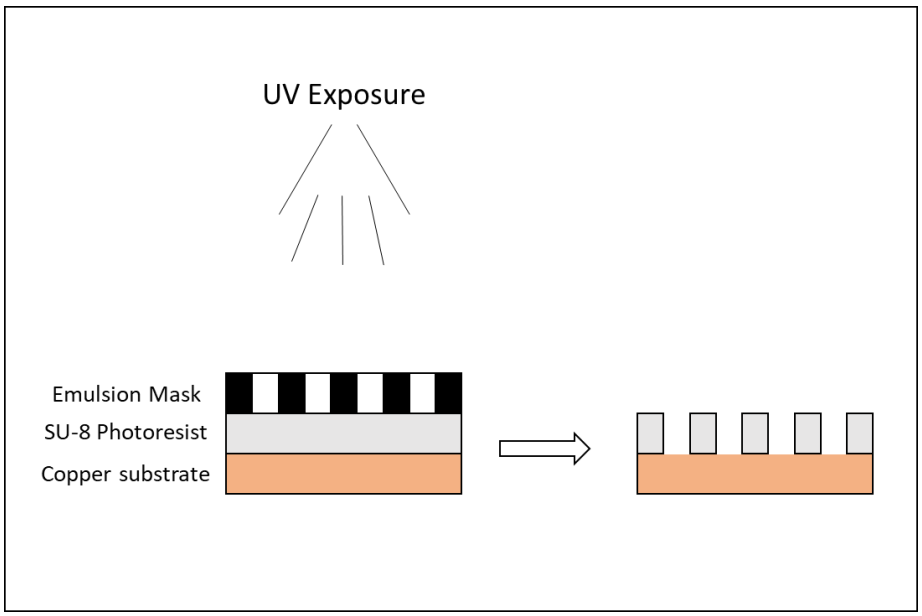

Figure 3-3: Schematic Diagram of UV Lithography process on Copper Substrate

3.1.1 Master Mask Film creation

Master mask film creation is the very first step of conducting this experiment. Software like Adobe Illustrator (AI) and Corel DRAW were used in order to design the complex micro pattern for the master mask film. Once the master mask film pattern completed, the next step to be done is print it on a transparent PET film by using image setter technique. Figure 3-4 shows the pattern of micropillars with different dimension produced by using Adobe Illustrator (AI).

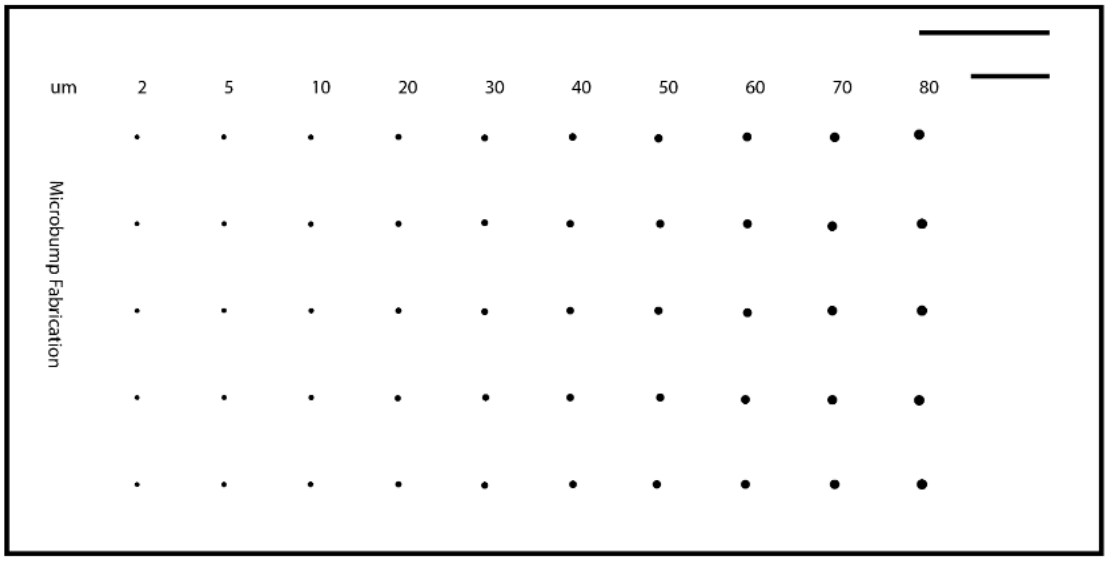

Figure 3-4: Design of Master Mask Film on PET

3.1.2 Emulsion Mask creation

The pattern from the master mask film was transfered to the blank emulsion mask (High Precision Photo Plate manufactured by Konica Minolta, Inc.) in the size ratio of 5:1 by using Simple Mask Fabrication Machine (MM605, Nano-metric Technology Inc.) in a dark condition as the emulsion mask is very sensitive to light. Light was exposed from light box to the master mask film and then project the pattern to the emulsion mask with scaling down the image 5 times than the original sizes for 6 seconds as in Figure 3-5(a). After the exposure process was done, emulsion mask was dipped and stirred into the mixture of CDH-100 and Distilled water

with ratio 1:4 for 2 minutes and then followed by distilled water for 2 minutes and Fixer Agent (CFL-881) from Konica Minolta, Inc. as shown in Figure 3-5(c) for 10 minutes continuously.

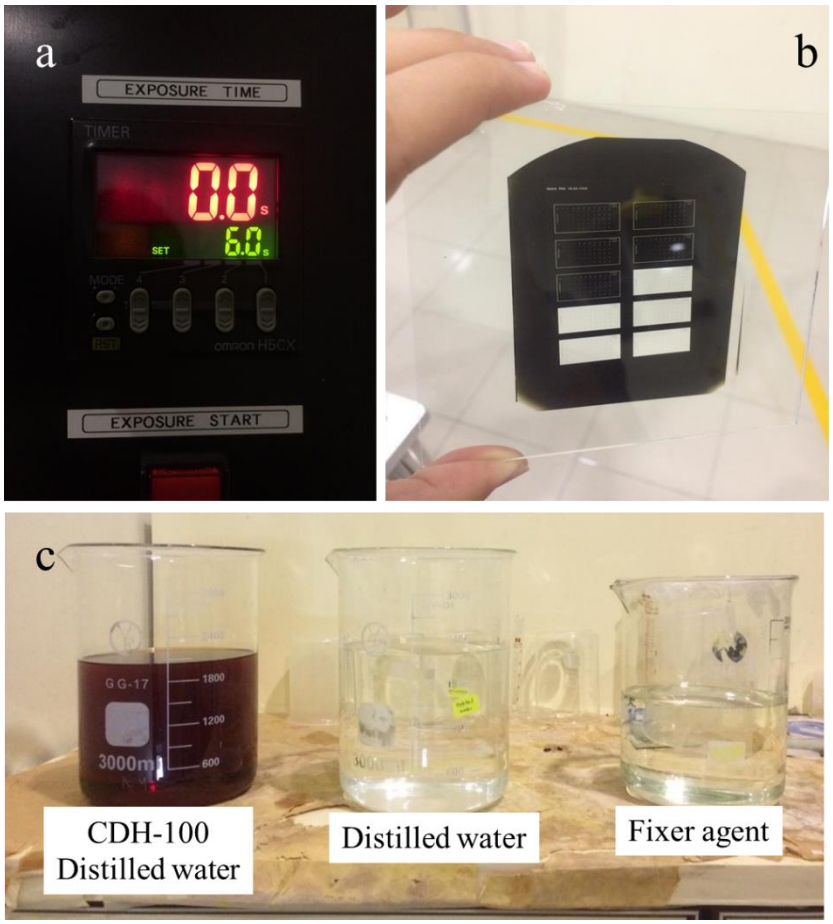

Figure 3-5: Emulsion mask preparation;

(a) Exposure time measurement, (b) finished emulsion mask, (c) chemical solution used after exposure process

3.1.3 Sample Preparation (Substrate cleaning)

Copper substrate was used in this experiment. Before do the substrate cleaning, make sure all the equipment used was very cleaned and dry using air gun. Clean the substrate by soak into acetone (QReC) in a beaker and put it in ultrasonic cleaner for 20 minutes. Continue this process by using methanol (HmbG Chemicals) and isopropyl alcohol, IPA (QReC) for 5

minutes each before being rinsed with distilled water. After that, the substratewas blown to dry it by using hair dryer and was on a hot plate at temperature 95°C for 5 minutes.

3.1.4 Photoresist coating

SU-8 2002 (MicroChem) were then being apply on the surface of the substrate as a photoresist. Syringe was used to dispense the SU-8 2002 to the surface of the copper substrate. Spin coater was not being used in this experiment since to achieve high thickness of pillar.

3.1.5 Substrate Pre Bake

After done with photoresist coating, the copper substrate will then go through with pre bake process. The reason of pre bake was done is to remove all the solvent off the substrate. The substrate were put on the hot plate as shown in Figure 3-6 for around 12 hours to make sure that the Su-8 on the substrate were fully coated.

Figure 3-6: Copper substrate was baked on the hot plate

3.1.6 Ultraviolet exposure

The emulsion mask that had prepare earlier was stack on the surface of the substrate that contain SU-8 2002 photoresist at the one side mask aligner machine LA4100_R1 (Sanei Electric Inc.). The substrate and emulsion mask was aligned and locked by using vacuum lock. Wait about 30 minutes so that the lamp power stable up to 180W shows in Figure 3-7(b). The substrate was exposed to the Ultraviolet light for 60 seconds in the dark condition.

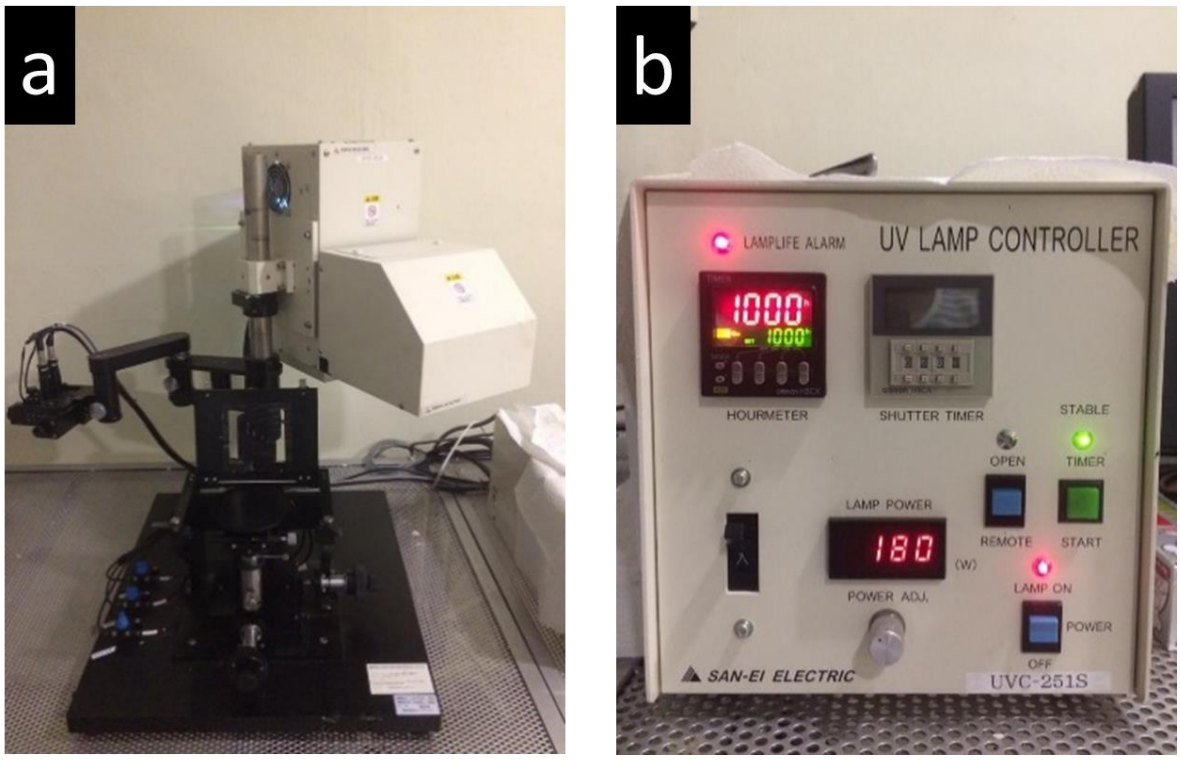

Figure 3-7; (a) one side mask aligner machine LA4100-R1 (Sanei Electric Inc.), (b) UV lamp controller

3.1.7 SU8 Post Bake

In order to reduce the standing wave effect after being exposed to UV radiation, the substrate again was baked on the hot plate at 65°C for 2 minutes and followed by 95°C for 10 minutes, 70°C for 5 minutes, 50°C for 5 minutes and 30°C for 5 minutes.

3.1.8 SU8 Development

Develop is the last step of this process as it function is to remove and wash away the unexposed SU-8 photoresist. The substrate was dipped and stirred into SU-8 Developer (MicroChem) for 20 minutes and was rinsed by using Isopropyl alcohol (IPA) and distilled water for 1 minutes each.

3.2 Microstructure analysis

Microstructural study of the specimens were conducted using Scanning Electron Microscopy (Hitachi S3400N) couple with elemental analysis EDX. The function of this study is to analyze the structure and the dimension of the hole produced by UV Exposure during lithography process. Since the image were very dark and hard to capture using the SEM machine, the specimens was sputter coated using Mini Sputter Coater (SC 7620 - Quorum) for 5 minutes. The actual function of Mini Sputter Coater is for coating specimens prior in tungsten filament SEMs.

3.3 Electrodeposition of Nickel

Electrodeposition or electroplating is the method of coating one metal or plate with another. Usually this method is used for decorative purpose, appearance and protection. In this experiment, Nickel was used to coat the copper that has been gone through the lithography process to produce pillar on it. The schematic diagram of nickel electrodeposition in

Figure 3-8 shows how the nickel is coated on the copper substrate. Figure 3-9 shows all the steps involved for electrodeposition process.

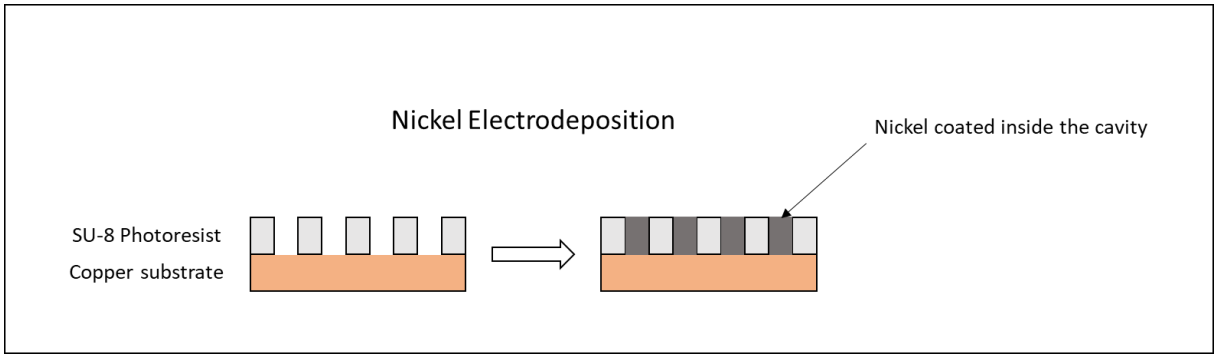

Figure 3-8: Schematic diagram of nickel electrodeposition process on patterned substrate

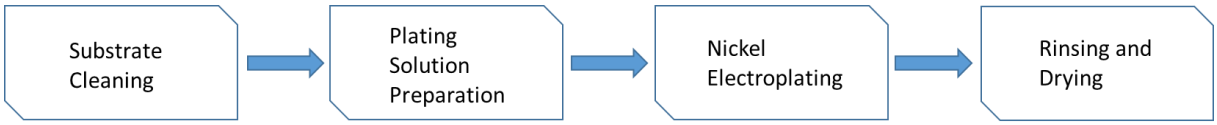

Figure 3-9: Steps of Electrodeposition of Nickel Process

3.3.1 Substrate Cleaning

Before start the experiment, copper substrate was cleaned in a mixture of 30 ml of deionized water and 5 ml of sulphuric acid (H_2SO_4) and was put into ultrasonic bath for 5 minutes. Then, the substrate was blown dry with nitrogen gas by using hairdryer. The function of cleaning is to prevent any contamination on the surface of the copper that will prevent the nickel electroplating coating from properly adhering to the copper substrate.

Safety measures: make sure that Sulphuric acid (H_2SO_4) was added into water not water added into Sulphuric acid as this process can cause exothermic reaction to occur that result water splashed.

3.3.2 Electroplating Solution Preparation

In order to conduct an electrodeposition or electroplating process, it requires a specialized electrolyte solution for the substrate to be immersed into. Nickel (II) Sulphate was used as an electrolyte in this case since Nickel is used to coat the copper substrate. As illustrated in Figure 3-10, the mixture of 60 ml of distilled water, 10 ml of sulphuric acid (H_2SO_4) and 5 grams of Nickel Sulphate ($NiSO_4$) was put into the 150 ml beaker to produce Nickel (II) Sulphate solution, $NiSO_4$ $(H_2O)6$ Aldrich, USA. The solution was put on the hot plate at 65°C and stirred vigorously until the Nickel Sulphate ($NiSO_4$) were totally dissolve in the solution [44].

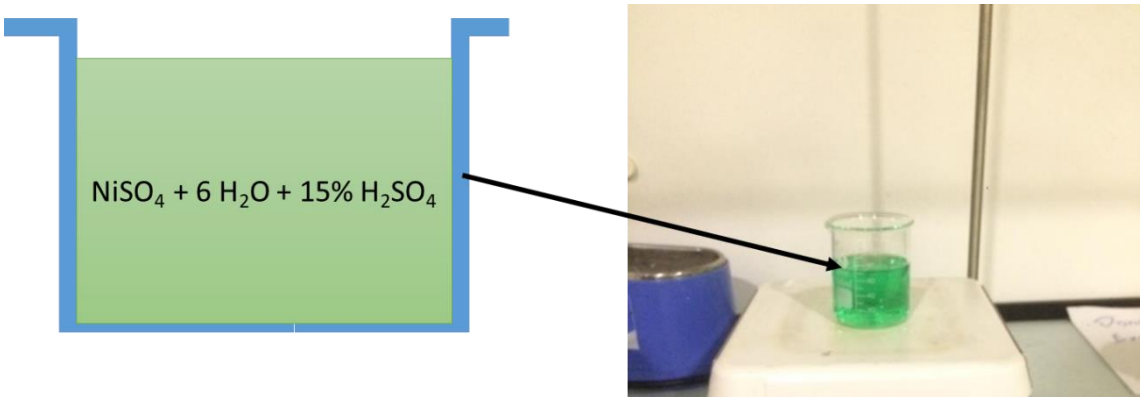

Figure 3-10 Nickel (II) Sulphate solution, $NiSO_4$ $(H_2O)_6$ Aldrich

3.3.3 Nickel Electroplating

Before start the electroplating process, make sure that the back of copper substrate was covered using an insulator to prevent electrolysis happened at the back of copper substrate. Nickel plate was fixed at the anode pole position while copper substrate was at the cathode pole of DC power supply (GPS – 3030D). The voltage was set at 1.1 V and current was set at 1.35 as shows in Figure 3-11(a) during the process. Once ready for plating, both nickel plate and copper substrate were dipped into the Nickel (II) Sulphate electroplating Solution for an hour in closed circuit. During this process, electrolysis happen as illustrated in Figure 3-11(b). Nickel ion

attracts to copper substrate and the copper substrate will be coated with layer of nickel consequently.

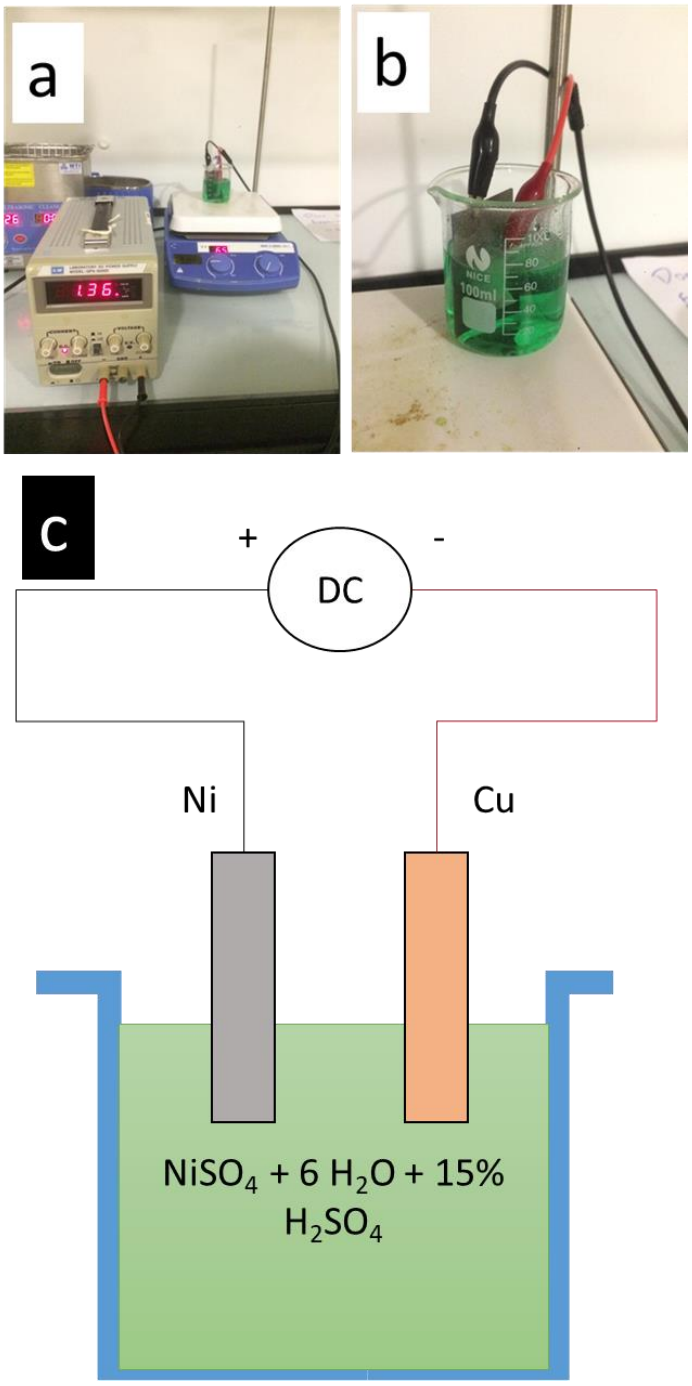

Figure 3-11; (a) Setup for Electrodeposition of Nickel, (b) Electrolysis process, (c) Schematic diagram of Nickel Electrodeposition