INFLUENCE OF COPPER PILLAR BUMP STRUCTURE ON FLIP CHIP PACKAGING DURING REFLOW SOLDERING

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DECLARATION

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

Signature …… (CHONG JIA JUN)

Date ……29 May 2019……

STATEMENT 1

This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by giving explicit references. Bibliography/references are appended.

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ABSTRAK

Pasaran elektronik pengguna adalah salah satu pasaran yang paling pesat berkembang di dunia. Teknologi Serpihan Flip (FC) adalah salah satu teknologi untuk menghubungkan peranti semikonduktor, dan dengan permintaan untuk menyusut jejak pakej elektronik, teknologi FC mesti mengendalikan peningkatan ketumpatan I/O interkoneksi, dan pada masa yang sama perlu menawarkan prestasi yang lebih tinggi serta berbilang fungsi, pada kos yang lebih ekonomik. Selain itu, berikutan sekatan penggunaan pateri plumbum, industri memerlukan cara altenatif dalam sambungan litar, maka FC jenis tiang tembaga (Cu) muncul sebagai cara penyelesaian yang baik. Walau bagaimanapun, FC jenis tiang Cu tidak digunakan secara meluas pada masa kini kerana kebolehpercayaannya tetap menjadi kebimbangan. Oleh itu, pengoptimuman pada teknologi ini mesti dijalankan. Dalam kerja ini, pendekatan pengkomputeran bendalir dinamik (CFD) digunakan untuk memodelkan proses pematerian balikan FC jenis tiang Cu, terutamanya dalam peringkat balikan. Pemodelan Isi Padu Bendalir (VOF) dan Pemodelan Pemeluwapan/Peleburan digunakan untuk tujuan simulasi ini. Model simulasi yang dapat menggambarkan peleburan dan pemejalan pateri dibentangkan dalam kerja ini. Pengaruh diameter tiang Cu pada pematerian balikan juga dikaji. Penemuan kajian menunjukkan bahawa jumlah isi padu pateri adalah faktor utama yang mempengaruhi pematerian balikan. Walau bagaimanapun, penemuan juga menunjukkan bahawa keupayaan model berangka dibentangkan dalam kajian ini terhad kerana tidak dapat menangkap anjakan pepejal semasa simulasi. Cadangan diberikan untuk mengatasi kelemahan model pada masa depan.

INFLUENCE OF COPPER PILLAR BUMP STRUCTURE ON FLIP CHIP PACKAGING DURING REFLOW SOLDERING

ABSTRACT

Consumer electronics market is one of the fastest growing markets in the world. Flip chip (FC) technology is one of the technologies for interconnecting semiconductor devices, and with the demand for shrinking in footprint of electronic packages, FC technology must handle the increase in I/O interconnect density, and at the same time need to offer higher performance, more function, at lower cost. Furthermore, with the restriction of usage of leaded solder, industry needs a solution to overcome the hassle, and copper (Cu) pillar bump FC appears as a good solution. However, Cu pillar FC is not widely used nowadays because its reliability remained a concern. Thus, optimization of the technology must be done. In this work, computational fluid dynamic (CFD) approach is used to model the reflow soldering process of Cu pillar type FC, particularly in reflow stage. Volume of Fluid (VOF) modeling and Solidification/Melting modeling are used for this simulation purpose. A simulation model which capable to visualize the melting and solidification of solder is presented in this work. The effect of diameter of Cu pillar on reflow soldering is investigated. Findings suggest that the solder volume is the key factor affecting reflow soldering. However, findings also hinted that the capability of the numerical model is limited due to inability to capture displacement of solid during simulation. Future recommendation is suggested to overcome the limitation.

CHAPTER 1 INTRODUCTION

1.1 Motivation

Consumer electronics market is one of the fastest growing markets in the world. This market segment includes, for example, radios, TV sets, MP3 players, stereo systems and DVD players as well as hardware derived from the field of communications electronics, e.g. desktop computers, laptops, tablets and smartphones. In year 2018, revenue in the Consumer Electronics segment amounts to US$307,279 Million worldwide, with 1,547.5 Million users and the figure is expected to reach US$454,492 Million of market volume, with 2562.5 Million of user by year 2023 (Statista, 2019).

It is no doubt that the consumer electronics industry is today a business with high growth and extremely competitive. Constant technology advancement of high pace is required to keep up with the constant innovation and optimization of products and fabrication processes used by major players in the industry.

Flip chip (FC) technology is one of the technologies for interconnecting semiconductor devices, such as IC chips and microelectromechanical systems (MEMS), to external circuitry with solder bumps that have been deposited onto the chip pads (Jin et al., 2011). First introduced by IBM in 1960s, this technology has been constantly improved to meet industry's demand.

In recent year, as the line width and spacing of advanced semiconductor devices become more compact, FC technology must handle the increase in I/O interconnect density, and at the same time need to offer higher performance, more function and lower cost (Cheng et al., 2015; Luo et al., 2016). However, FC with ball grid array (BGA), or C4 (controlled-collapse chip connection) technology will soon draw near to its bottleneck due to the large diameter of solder bump (Lau, 2016). Recently, copper (Cu) pillar bump technology, also known as C2 (Cu-pillar with solder cap) bump, is receiving great attention for FC package because it provides a more promising solution in shrinking the bump pitch alongside several advantageous features such as lower joint resistance, etc.

The reliability of Cu pillar bump in FC assembly, especially in reflow process, however, is yet to be proven. This is due to the self-alignment characteristic of Cu pillar bump is nowhere near the C4 bump's (Lau, 2016). The yield of Cu pillar FC is nowhere near C4 bump (to be discussed in next chapter) and hence is seldom being used by the industry.

Furthermore, the ban of lead-based solder due to European Union Waste Electrical and Electronic Equipment Directive (WEEE) and Restriction of Hazardous Substances Directive (RoHS) introduced back in year 2006 forced the industry to shift from lead-based solder to silver-based solder imposed an increase in cost. Companies have been looking at less expensive solder alternatives, especially for use in inexpensive products that have short operating lives and are used in mild application conditions (Cheng et al., 2017). In this context, Cu pillar bump technology appears as a good alternative to solve the situation.

1.2 Problem statement

The demand for FC packages with higher I/O interconnect density and smaller footprint is increasing exponentially. However, conventional BGA type FC will soon reaches its bottleneck because further shrinkage in pitch length or solder bump diameter is difficult to achieve. In this case, the potential of Cu pillar bumping is promising and hence continuously development is mandatory. However, the reliability of Cu pillar bump in FC has yet to be validated: the yield of Cu pillar bump FC is relatively low compared to BGA type FC and inevitable stress induced on the chip (due to its physical structure) during manufacturing process resulting in reduced lifespan of Cu pillar bump type FC. In the meantime, only limited researchers are working on Cu pillar bump technology and studies are often limited to finite element (FE) analysis to determine the durability of such technology after long term of usage. Minimal to no research work are done to optimize the manufacturing of Cu pillar bump, such as optimizing the reflow process to increase the throughput of Cu pillar bump FC.

1.3 Objectives

The numerical simulation of electronic product soldering process has shown great potential to provide precise, simple, fast and economical way, to predict the thermal reflow cycle in soldering process. Design optimization can be carried out efficiently with the result obtained from the simulation model, to avoid possible problems which might be encountered during production of products.

With the objective of understanding the behaviour of reflow soldering with the variation of Cu pillar bump structure and then predict the entire reflow process, CFD approach was utilized to simulate the process. Parameter of the structure of Cu pillar bump in concern is its diameter.

The objectives of this work are specifically the following:

1. To simulate the reflow thermal cycle of Cu pillar bump FC package using CFD technique.
2. To visualize the deformation of solder tip during a reflow thermal cycle, specifically in its melting and solidification.
3. To analyse the influence of diameter of Cu pillar bump on the reflow process during thermal reflow.

1.4 Scope of research

This study is limited to the development of CFD model for the simulation of the reflow soldering process of Cu pillar FC package in a simplified reflow thermal cycle, particularly in the reflow stage. The CFD simulation model is constructed by using ANSYS 18.1 software. A trial model is prepared to verify the feasibility of modelling of melting and solidification. Once the solution of trial model is justified, the work proceeds to model the reflow stage of Cu pillar bump FC.

1.5 Thesis outline

In Chapter 2, FC technology and its development in recent years are presented in general. Advantages and limitations of Cu pillar bumping are listed in this chapter as well. Researches done previously are reviewed and summarized at the end of the chapter.

Chapter 3 explores ANSYS Fluent, more specifically the VOF model and Solidification/Melting Model. The methodology for simulation is also outlined in this chapter.

In Chapter 4, the result obtained from simulation is presented. Validation and discussion are done in this chapter.

Lastly, the conclusion of this thesis is made in Chapter 5. Some recommendations are suggested as future improvement.

CHAPTER 2 LITERATURE REVIEW

2.1 Overview

In this chapter, the state of art of Cu pillar bump technology is reviewed and defined. The advantages and limitations of the technology is discussed. Literatures of previous research initiatives were reviewed and discussed at the end of the chapter.

2.2 Flip chip technology

A flip chip is defined as a chip attached to the pads of a substrate or another chip with various interconnect materials (e.g., Sn-Pb, Cu, Au, Ag, Ni, In, and isotropic or anisotropic conductive adhesives) and methods (e.g., mass reflow and thermocompression bonding (TCB)), as long as the chip surface (active area or I/O side) is facing the substrate or another chip (Lau, 2016). First introduced by IBM in the early 1960s for their solid logic technology, flip chip technology has become the logical foundation of the IBM System/360 computer line, and widely used in high functional performances of electronic devices in computer, military, mobile, automobile, etc. (Lau, 2016; Tsai et al., 2018).

First IBM flip chip is created with three terminal resistors, which are Ni/Au plated Cu balls embedded in a Sn/Pb solder bump on the three I/O pads of transistor. A Cr-Cu-Au adhesion/seed layer is deposited between the Al-Si contact pads on the Si chip and the solder bump and was joined to ceramic package. See Fig. 2.1.

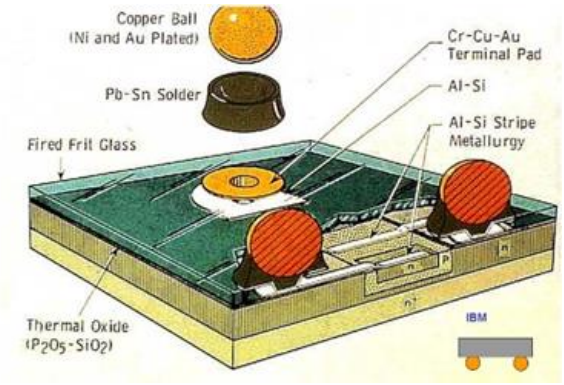


Figure 2.1 IBM's first flip chip with three terminal transistors (Lau, 2016)

As the number of I/O increases, the Cu balls are replaced by solder bump – the so-called C4 technology. This technology utilizes high-lead solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and all solder joints are made simultaneously by reflowing the solder.

2.2.1 State of the art

Chip interconnection bumps technology has been evolved over five decades and is generally divided into three generations according to the connection method (Tsai et al., 2018). The first generation – C4 bumps, typically has the bump pitch over 130µm, while the second generation, Cu pillar bump's bump pitch is within a range from 40 to 130 µm. The most recent one (third generation), known as 3DIC assembly, has been developed to be smaller than 30µm, and the existing soldering process can no longer support this new bump scaling and new process such as Cu-to-Cu direct bonding are required. However, Cu-to-Cu direct bonding is beyond the scope of discussion in this paper. Fig. 2.2 shows current bumping technology generation excluding Cu-to-Cu direct bonding technology.

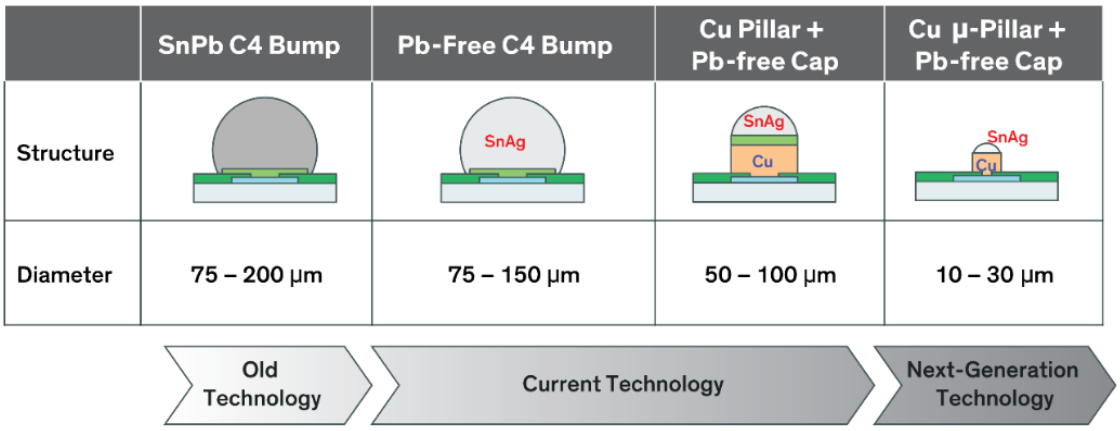


Figure 2.2 FC bumping technology generations in a glance (Wei, 2016)

Copper, owing to its superior electrical and thermal properties, is an idea material for flip chip bumps to replace SnPb or lead-free solders. This is due to the thermal conductivity (W/m K) and electrical resistivity (µΩ m) of Cu (400 and 0.0172) are superior than those (55−60 and 0.12−0.14) of solder. Cu pillar with solder tip is also one of the

solutions that the solder volume is reduced to prevent bumps bridging (Tung, 2003). Although copper balls had been used for interconnect, it is much more desirable to form the interconnecting bumps in a tall, slim post structure to narrow the bump footprint.

The fabrication process of Cu bump with solder tip is similar to that of solder bump, except for the thickness of copper and solder plating process are adjusted. The main Cu pillar bump process consists of physical vapor deposition (PVD), Lithography, Electroplating, Etch and Reflow (Koh et al., 2011; Luo et al., 2016). Fig. 2.3 shows the flow chart for standard wafer bumping fabrication process.

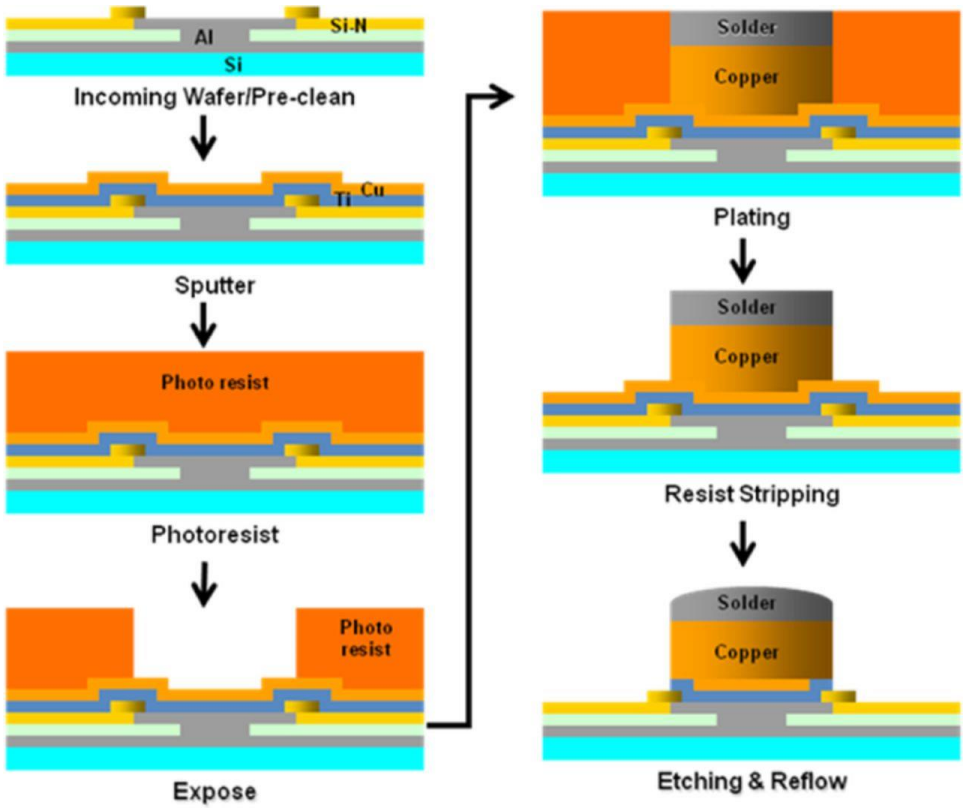


Figure 2.3 Fabrication process of Cu pillar bump (Lau, 2016)

2.2.2 Advantage and limitation of Cu pillar bump technology

For flip chip and package assembly, there are additional advantages in choosing Cu pillar bump (Koh et al., 2011; Lau, 2016):

- Ultra-fine pitch bumps as small as 30um staggered bumps.
- Drop-in replacement for fine pitch solder bump flip chip devices and packages.
- Flexible pillar shape, size, and height.
- Use on flip chip device existing in-line or staggered pads with no need for redistribution layer (RDL).
- Compatible with wafer level processing with similar RDL and TSV fab process tools.
- Use on IC devices with high I/O count and high performance (higher frequency, better signal integrity).
- Better electromigration resistance.
- Higher standoff hence easier underfill capillary flow and use of mold underfill.
- Lower alpha particle effect.
- Better thermal performance, option to add thermal pillar bumps.
- Application for ultra-low profile package on package (PoP).

However, there are also some major concerns for Cu pillar type FC manufacturing and assembly. The main concern is low yield and high defect rate compared to C4 assembly. Due to the larger volume of solder, the surface tension of C4 solder bump enables it to perform self-alignment, making the process very robust. The assembly process for Cu pillar type chip is the same as that of C4 bumps. However, in Cu pillar bump, because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the self-alignment of the Cu pillar with the solder cap bump, thus making it seldom being used (Lau, 2016).

Other major concerns for Cu pillar manufacturing and assembly include (Koh et al., 2011; Lau, 2016):

- Initial high cost of capital investment for wafer bumping.
- Wafer level bump fabrication process experience to gain good bump uniformity and yield.
- Throughput in flip chip assembly using thermal compression.
- Stress management over ELK and ULK layer for sub 30nm node devices.
- Long term reliability data.

2.3 Previous research

The reflow soldering process has been studied extensively by scholars to improve yield and reliability. However, most of the researches focused only on BGA type package, since it is the mainstream flip chip type in today's market. Although some literatures were found discussing Cu pillar bumping, these discussions are very much limited to a specific situation, such as the visualization of warpage, temperature and stress distribution on the substrate and chip and so forth.

For example, interfacial delamination is a problem when Cu pillar bumping is applied on ultralow-K chip. Chen et al., (2014) has proposed to use redistribution layer technology to relocate under bump metallurgy pads with aim to reduce the thermal-mechanical stress of ultralow-K chip. FEA model was conducted by them to determine the reduction of thermal-mechanical stress. In addition, Che et al., (2015) also conducted stress analysis with FE method to optimize the design for interconnection between low-k chip and Cu pillar bump. Pun et al., (2016) has studied the effect of substrate surface finish, pad sizes and substrate flatness on occurrence of solder joint failure in Cu pillar solder flip chip interconnects.

These examples of previous work shown that most of the study done on Cu pillar bump type flip chip are mostly on FE analysis. The analysis is usually done on the situation after the flip chip package is completely assembled on substrate. It is worth mentioning that minimal work has been done on assembly process, which is the reflow process of Cu

pillar bump type flip chip by using CFD approach. However, CFD approach has been employed thoroughly in surface mount technology (SMT) industry in recent years, especially in the modelling of reflow soldering process.

As per reviewed by Lau et al., (2016), the modelling of the reflow soldering process is divided into two important stages, namely board-level analysis and package-level analysis. Firstly, in board-level analysis, environment model at the reflow oven is developed to study the thermal characteristic of the three key elements in reflow process: reflow oven, PCB and solder joints. The developed model is often validated through experimental methods. The understanding of thermal characteristic of these elements enables engineers to sustain and control the quality of solder joint in reflow soldering process.

One notable work of environment modelling is the CFD modelling of flow field inside a reflow oven by Yu & Kivilathti, (2002). They presented a CFD model of the air heat flow inside a reflow oven and described the geometrical mesh and boundary conditions in detail. Their results were found to be coincident with measured data. The result obtained was then utilized in their following transient analysis as well as board level model (Yu et al. , 2006).

Apart from that, Deng et al., (2016) has proposed a simulation method which can accurately predict the temperature distribution in a reflow oven for the reflow process of system in package (SiP). Their model capable to design the temperature profiles for reflow process which result in very minimal deviation to the actual temperature in the SiP. It was concluded that their model is effective in designing thermal profile for reflow soldering production and able to decrease development time significantly.

Secondly, package-level analysis is performed to investigate temperature and thermal stress response within the solder joints of surface mount components (SMCs). Such analysis can be conducted through three approaches: modelling reflow thermal profile, fluid-structure interaction (FSI) and global/local modeling (Lau et al., 2016).

Recent work by Lau & Abdullah, (2013) has outlined a methodology for the thermal modelling of a BGA assembly during forced convection reflow soldering by using FSI method. Their work provided a new guideline for thermal coupling method and is useful for the accurate control of temperature distribution within PCB assembly.

Some other authors also carried out study on specific part of the reflow process, such as, the preheating phase (Lau et al., 2012b) or the cooling phase (Lau, et al., 2012a) of the reflow soldering process, to investigate the effect of different parameters on the solder joint reliability in the product.

Both board-level analysis and package-level analysis reviewed were found to consider solder joints as solid part in the simulation model. The goal of above-mentioned studies aimed to increase the reliability of solder joint came out from the reflow oven after reflow process. Even though the solution obtained proven to be reliable, but the solder joints are indeed undergoing phase change during reflow process. Simulation of the phase change process is often overlooked in previous study.

One interesting work was done by Costa et al., (2015), which simulated the deformation of solder paste in a simplified thermal cycle. In the work, the reflow process of surface mounted component (SMC) was modelled by using ANSYS Fluent. The reflow soldering process was modelled using combined Volume of Fluid (VOF) and Solidification/melting method. VOF method was used to capture the position of the existing interfaces and the Solidification/melting method which uses an enthalpy-porosity approach was used to simulate the fusion of the material.

Another similar work by Rodrigues et al., (2016) used VOF method to simulate the melting shape of SAC305 solder. The model showed that it is possible to accurately predict the melting shape of melted solder by using ANSYS Fluent software. The prediction of solder melting can have significant role in optimizing reflow process, provided a robust numerical model is present.

2.4 Summary

To the best of author's knowledge, no study has been conducted on the reflow soldering of Cu pillar bump type FC by using CFD approach, nor parametric study on Cu pillar structure during reflow soldering. Thus, a methodology to simulate the process of reflow assembly of Cu pillar bump type FC is very much favorable. However, the modeling of entire reflow soldering process is tedious due to the long transient time which can go as much as 300 s. Hence, the simulation model will focus particularly in the reflow stage, which visualizes the deformation of solder tip on Cu pillar bumping, during melting/solidification process.

In this case, a commercial computational software which highly adopted by scholars, ANSYS Fluent is a good choice of simulation tool due to its reliability in providing solution with high accuracy in an efficient manner.

CHAPTER 3 METHODOLOGY

3.1 Overview

The methodology of the thesis is presented in detail in this chapter. The ANSYS Fluent, more specifically, the VOF model and Solidification/Melting model, are explored since they are utilized extensively in this work.

Two simulation models were developed in this work. The first simulation model was developed as trial model to ensure the prediction of melting and solidification is correct and the result was validated. Then, Cu pillar bump type flip chip assembly simulation model was developed to study the influence of diameter to reflow process. The development of simulation model in ANSYS Fluent environment is discussed in this chapter.

3.2 ANSYS Fluent

ANSYS Fluent software contains the broad, physical modelling capabilities needed to model flow, turbulence, heat transfer and reactions for industrial applications. These range from air flow over an aircraft wing to combustion in a furnace, from bubble columns to oil platforms, from blood flow to semiconductor manufacturing and from clean room design to wastewater treatment plants. Fluent spans an expansive range, including special models, with capabilities to model in-cylinder combustion, aero-acoustics, turbomachinery and multiphase systems.

3.2.1 Multiphase modelling

Normally the flows found in nature or in industry they are a mixture of phases. The physical phases of materials are three, gas, liquid and solid, but the concept of phase in multiphase flows it is applied in an ampler way. In multiphase flows one phase can be defined as a class of identified material that it has a particular answer of inertia and it interacts with the flow and with the potential field in which it is immersed.

Multiphase flows regimes can be divided into three categories as (A. Inc., 2016a):

- Flows gas-liquid or liquid-liquid
- Flows gas-solid
- Flows liquid-solid
- Flows with three phases, which are combinations of other flow regimes listed above.

In ANSYS Fluent, three different Euler-Euler multiphase models are available, the volume of fluid (VOF) model, the mixture model, and the Eulerian model (A. Inc., 2016a). The mixture model and Eulerian model are beyond the scope of discussion in this work.

3.2.1 (a) VOF model

The VOF model is a technique of surface-tracking applied to a fixed Eulerian mesh. This model was developed for two or more immiscible fluids where the interface between the fluids has interest. In the VOF model, one unique set of momentum equations is shared by all fluids, and the volume fraction of each fluid in each cell is tracked across the domain. The VOF model can be applied for stratified flows, free-surface flows, filling, sloshing, the movement of large bubbles in a liquid, the movement of liquid after a dam break, and the steady or transient tracking of any interface liquid-gas.

However, this model has some limitations as (A. Inc., 2016a):

- The VOF model is only available with the pressure-based solver.
- The entire domain of simulation has to be filled with a unique phase or a combination of phases. The VOF model does not allow empty regions where none fluid of any type is present.
- Only one phase can be defined as a compressible ideal gas. However, there is no limitation about the use of compressible liquids when a user-defined function (UDF) is used.
- The second-order implicit time-stepping cannot be used with the VOF explicit scheme.

3.2.2 Solidification/melting

The ANSYS Fluent can be utilized to solve solidification and melting problems, at constant melting temperature for pure metals, or at a range of melting temperatures for metallic alloys. The ANSYS Fluent instead of tracking the liquid-solid front explicitly, it utilizes the enthalpy-porosity formulation, which was suggested by Prakash et al., (1987). In this formulation, the porosity is obtained through the liquid fraction, which is the fraction of volume in one cell that it is in the liquid form. The liquid fraction is associated with each cell of domain and it is calculated in each iteration based in the enthalpy balance (A. Inc., 2016b).

The Mushy-zone is a region with a mixture of solid and liquid material, which it is treated as a porous zone with porosity equal to the liquid fraction. In this way, the liquid fraction has a value between 0 and 1. The solid region has a liquid fraction of 0, so the porosity is also 0. In opposite way, in the liquid region, the liquid fraction is 1, so the porosity is also 1. When the material solidifies, the porosity decreases from 1 to 0, and when the porosity becomes 0, the velocity drops also for 0 m/s. The mushy zone parameter measures the amplitude of the damping; the higher this value, the steeper the transition of the velocity of the material to zero as it solidifies (A. Inc., 2016b).

ANSYS Fluent has the following capabilities to modulate solidification and melting (A. Inc., 2016b):

- Calculation of liquid-solid solidification/melting for pure metals and binary alloys.
- Modulation of continuous casting processes this is, “polling” the solid material to out of domain).
- Modulation of thermal contact resistance between the solid materials and the wall (for example, because of the existence of an air gap).
- Modulation of species transport with the solidification/melting model.
- Post-processing of variables related to the solidification/melting model (this is, liquid fraction and pull velocities).

These capabilities allow the ANSYS Fluent to model a high range of problems involving the solidification/melting model, such as melting, solidification or freezing, crystal growth and continuous casting.

However, in ANSYS Fluent the solidification/melting model has the following limitations (A. Inc., 2016b):

- The solidification/melting model is available only with the pressure-based solver, so this model cannot be used with the density-based solver.
- The solidification/melting model cannot be used with compressible fluids.
- For the generality of multiphase models (VOF, mixture and Eulerian), only the VOF model can be utilized with the solidification/melting model.
- Except for species diffusion, it is impossible to specify different properties to the same material when it is liquid or solid through the GUI (Graphical User Interface). However, if necessary, different properties can be utilized to solid and liquid form of the same material with UDF.
- When the solidification/melting model is used in conjunction with the species transport and its reactions, there is not any action that restricts the reaction only in the liquid region, so the reaction is solved in the entire domain of simulation.

3.3 Trial model

A model of melting and solidification of phase change material (PCM) was developed based on VOF method proposed by Kim et al., (2013). The illustration of the computational domain of their model is shown in Fig. 3.1. Thermal input was specified at one end of the PCM and the PCM was slowly heated to its melting point by conduction. The melting/dripping behavior was observed from the numerical solution. The numerical solution in the model is able to accurately predict the deformation of PCM at PCM-air interface as shown in Fig. 3.2.

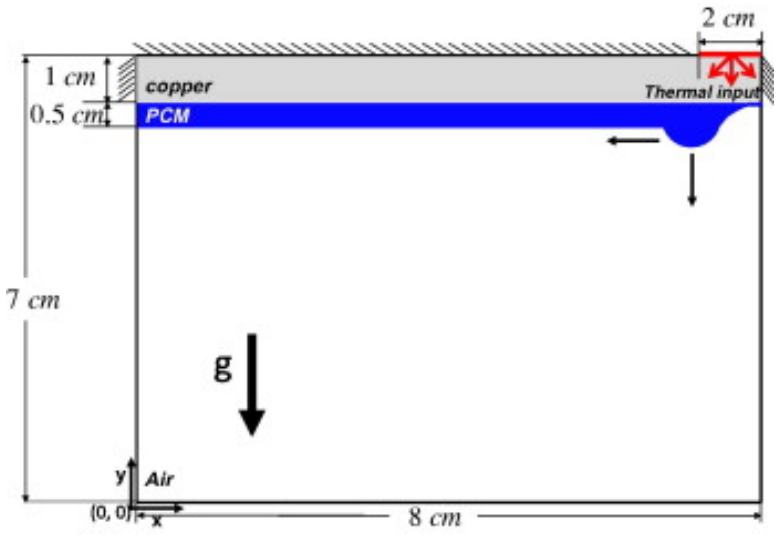


Figure 3.1 Schematic illustration of the computational domain by (Kim et al., 2013)

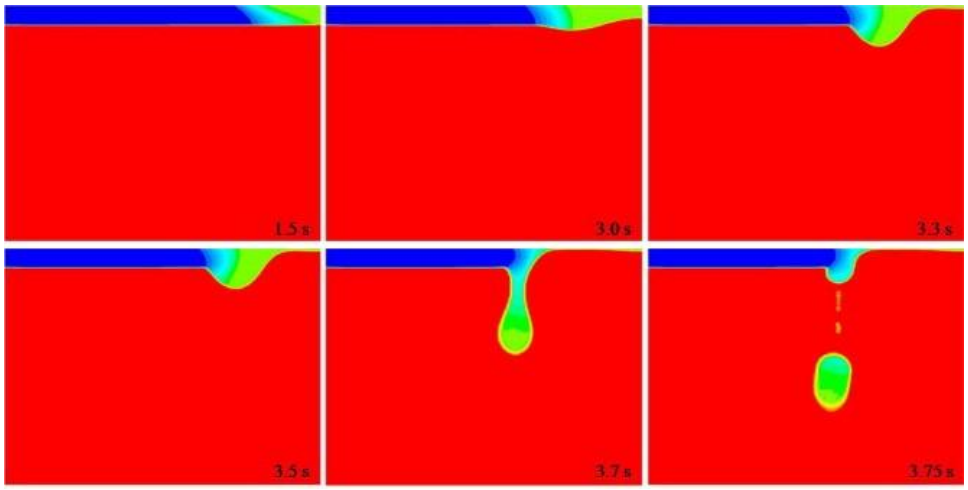
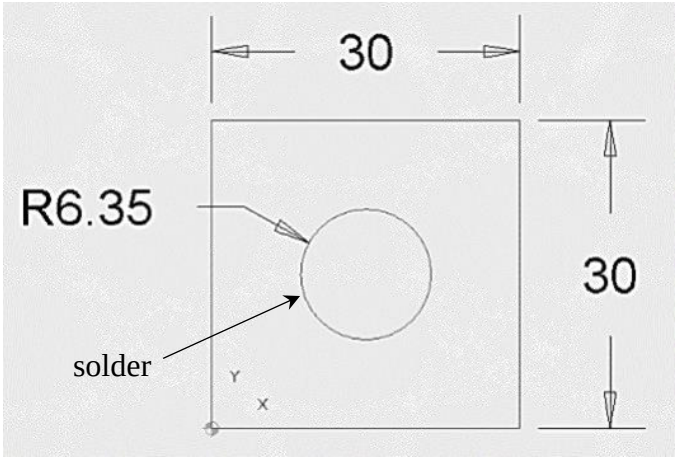


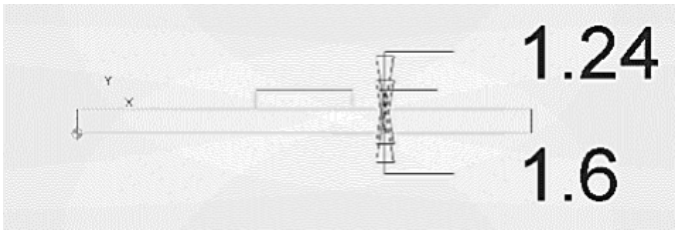
Figure 3.2 Melting and dripping of PCM with deformable PCM-air interface demonstrated by (Kim et al., 2013)

Hence, similar method was used to develop the trial model for melting and solidification of solder paste in reflow stage during reflow process. Solder paste is the PCM in this model. However, contrary to the model mentioned earlier, the thermal input in reflow process is not conduction. In fact, heat is transferred to solder via convection of heat from the heated air within reflow oven. Therefore, a new model was constructed, to simulate the melting behaviour of solder paste by inputting heat externally to the solder paste via convection.

Two models were developed in ANSYS 18.1, to investigate the solder melting numerically in (a) 2D and (b) 3D configuration, via convective heating. Schematic diagram of the numerical domain is shown in Fig. 3.3. Then, simulation models were created by using ANSYS Design Modeler in both 2D and 3D as shown in Fig. 3.4.

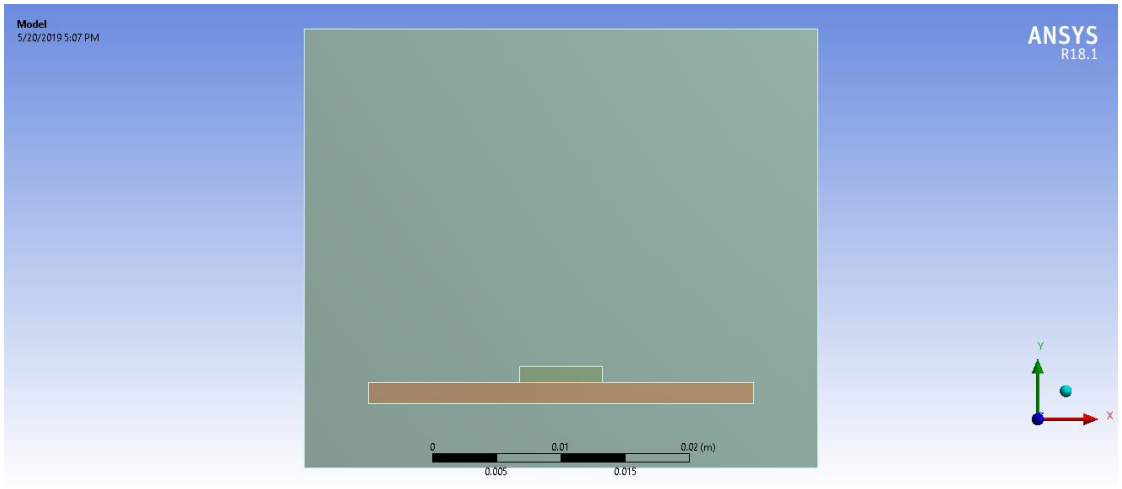


(a)

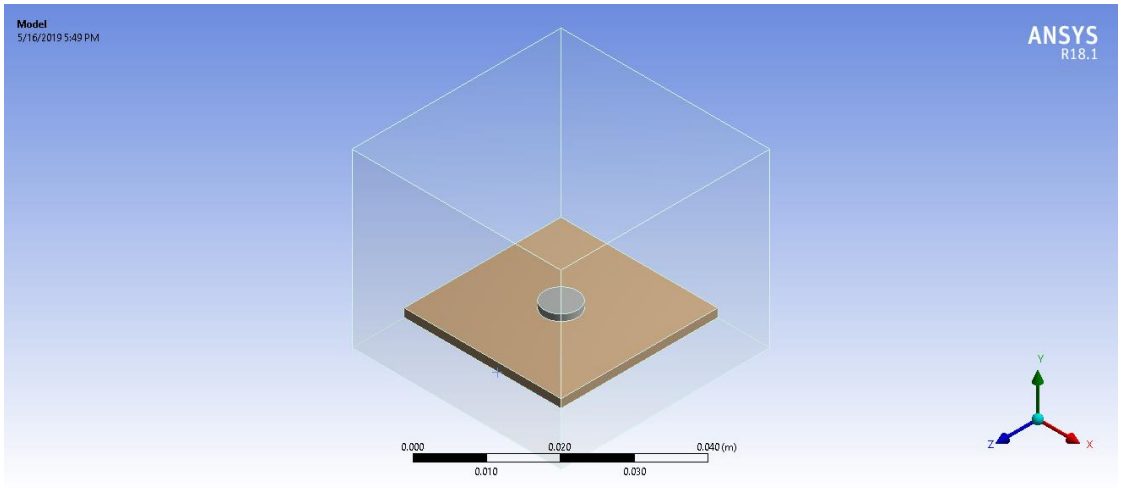


(b)

Figure 3.3 Schematic diagram for trial model (a) top view and (b) side view



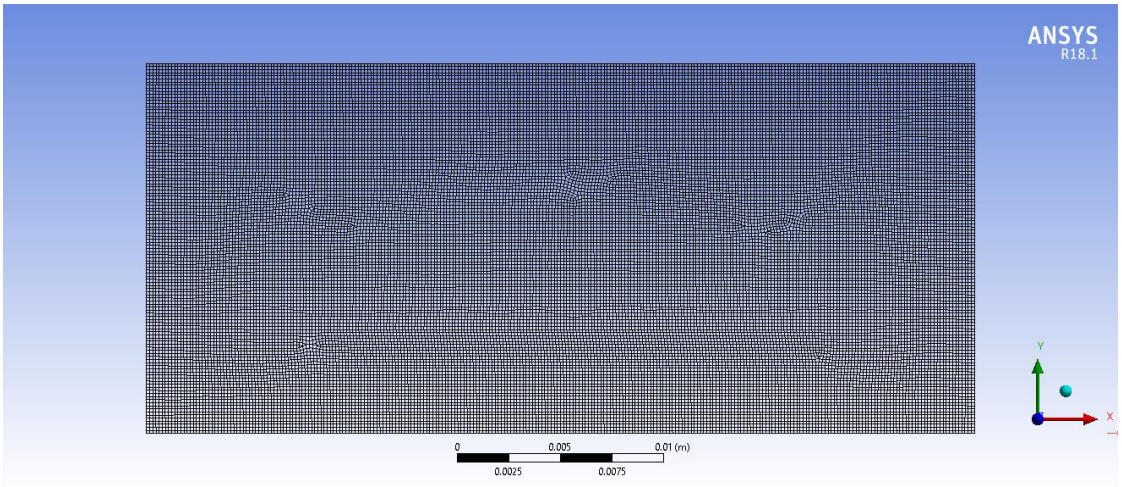
(a)



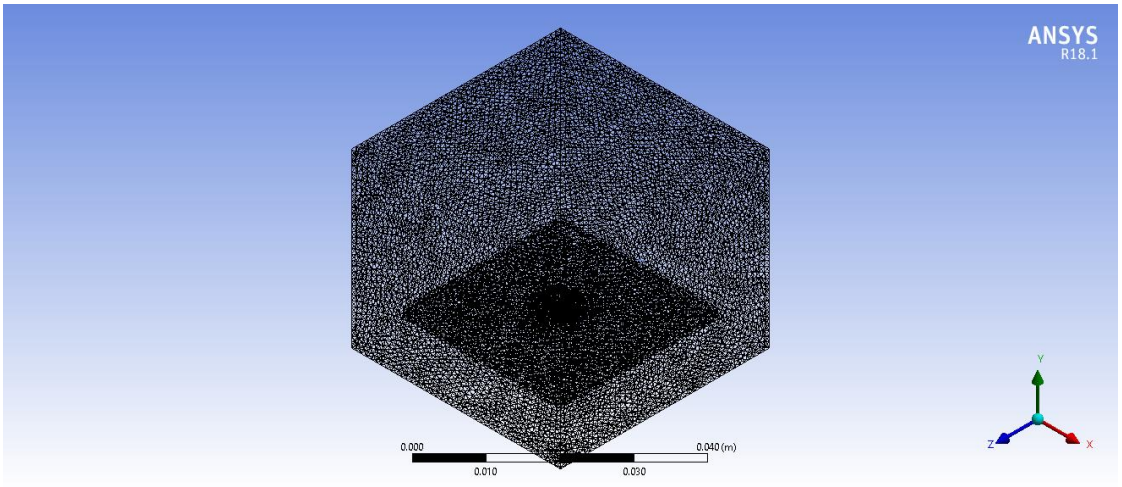
(b)

Figure 3.4 (a) 2D and (b) 3D model of trial model in ANSYS Design Modeler

The surface and volume mesh of the model were generated by using ANSYS Meshing. In the 2D geometry, fine structured mesh was generated throughout the computational domain for accurate solution. In 3D model, due to the limitation of computational power, tetrahedral mesh was used, and the mesh density was made denser around the solder to capture the flowing of solder more accurately. Generated mesh is shown in Fig. 3.5, and the detail for each mesh is tabulated in Table 3.1. The mesh size test was optimized for better accuracy and computational time. The generated mesh was then exported to ANSYS Fluent 18.1 solver.



(a)



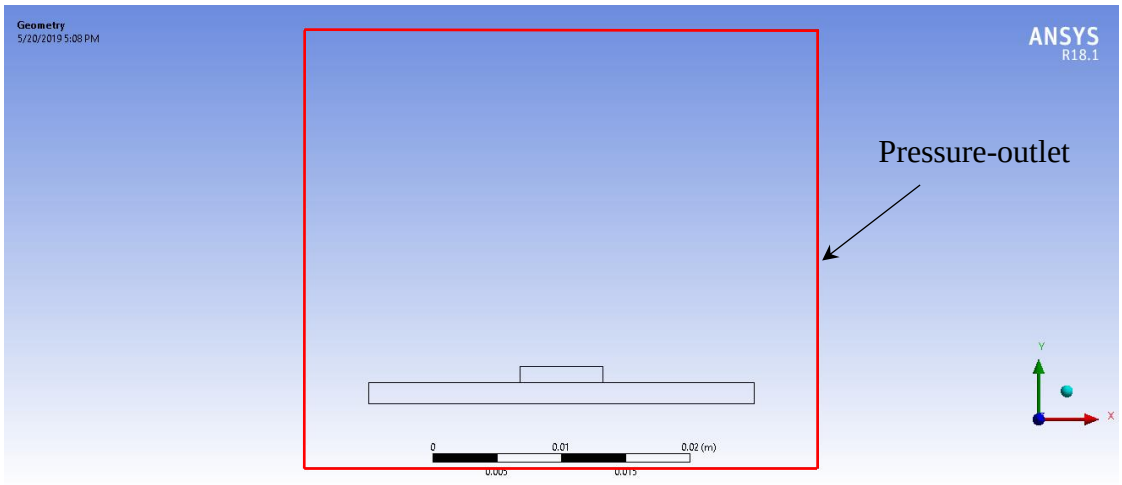
(b)

Figure 3.5 (a) 2D model meshed with structural grid and (b) 3D model meshed with tetrahedral grid

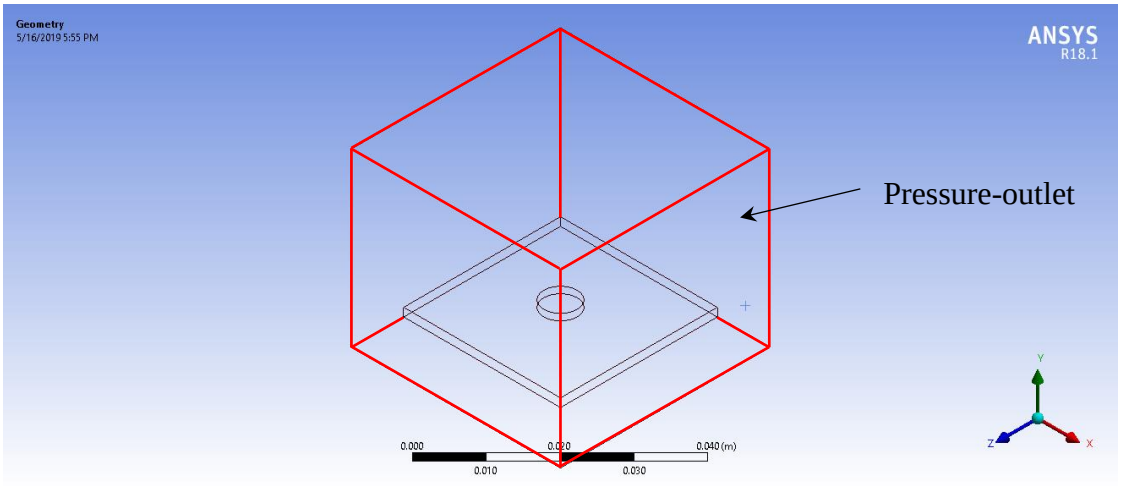
Table 3.1 Statistic for mesh generated in 2D and 3D model

	2D model	**3D model**
Nodes	32215	89440
Elements	31836	496216

At the initial condition, the model was initiated at constant temperature of 485 K, to resemble the condition in before reflow stage in the reflow process. Pressure-outlet boundary condition was set around the boundary, and temperature UDF was assigned at the back-flow temperature of the pressure-outlet according to the actual oven condition. The temperature UDF is designed to bake the solder paste in reflow oven for 45s, and then the spreading of solder is observed (Chellvarajoo & Abdullah, 2018). Solder was patched in the numerical model at the initial condition by using patching function. The boundary condition setting is shown in Fig. 3.6, whereas Fig. 3.7 shows the temperature UDF applied at the pressure-outlet boundary.



(a)



(b)

Figure 3.6 Boundary condition applied in (a) 2D model and (b) 3D model

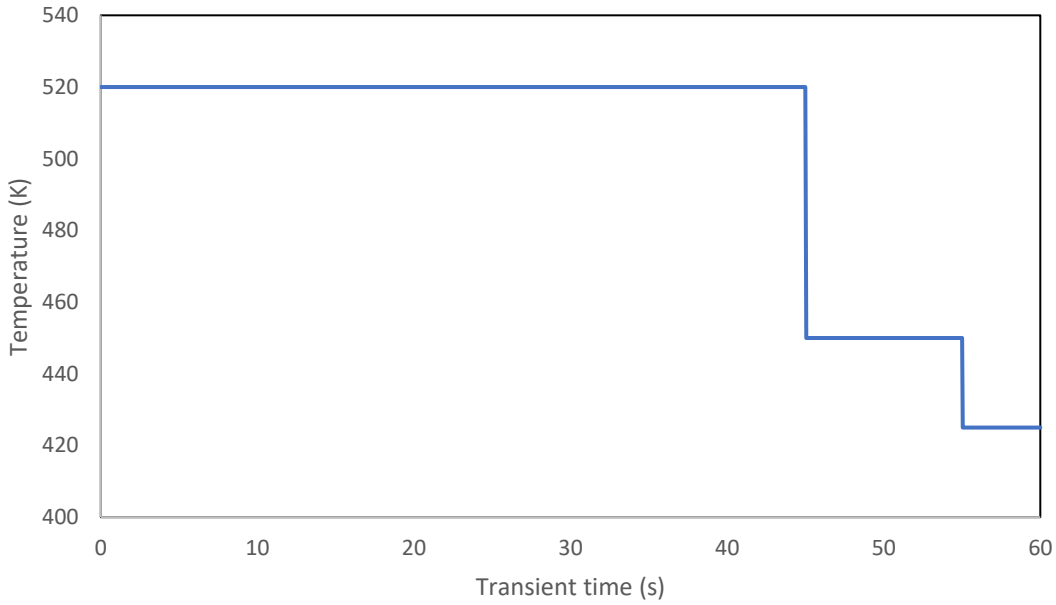


Figure 3.7 Temperature UDF applied at pressure-outlet

Implicit VOF model in ANSYS Fluent was enabled with two Eulerian phases. The Solidification/melting model in ANSYS Fluent was also enabled to simulate the melting and solidification of solder paste. The K-epsilon turbulent model was enabled to model the turbulent flow field around the PCM region. Air was set as default and the thermal properties of solder were applied into ANSYS Fluent. The material properties used in the model are specified in Table 3.2 whereas the thermophysical properties of solder used are specified in Table 3.3.

Table 3.2 Material properties used in trial model

	PCB
Density (kg/m^3)	1700
Thermal conductivity (W/m K)	0.2
Specific heat (j/kg K)	920

Adapted from Liang et al., (2005)

Table 3.3 Thermophysical properties used in trial model

	Solder − SAC405
Density (kg/m^3)	7640 – 0.9T
Thermal conductivity (W/m K)	236
Specific heat (j/kg K)	62
Solidus temperature (K)	490
Liquidus temperature (K)	498
Melting Enthalpy (J/kg)	59500
Viscosity (kg/m s)	0 – 490K > 0.271
	490 – 655K > linear from 0.271 to 0.01148
	655 – 1500K > 0.01148

Adapted from Costa et al., (2015)

Different time steps were tried, and the optimum time step is chosen to perform the simulation. Among time step of 0.05 s, 0.01 s, 0.005 and 0.001 s, time step of 0.01 s is proven to be optimum for both cases. The simulation was run on a computer with Intel i7 CPU 2.6 GHz processor with 3 parallel processes in Windows environment. Simulated flow time from t = 0 s to t = 60 s took approximately 40 minutes of elapsed time in 2D model, whereas 11 hours in 3D model. The corresponding result is presented in latter chapter.

3.4 Reflow assembly of Cu pillar bump flip chip assembly

The simulation of flowing of solder proceeded with Cu pillar type flip chip assembly. However, a Cu pillar bump-type flip chip consists up to thousands of Cu pillar beneath and it is almost impossible to model the complete flip chip package in a single simulation due to expensive computational cost. Therefore, a simplified flip chip, with 10 Cu pillar bumps was modelled in this work. A 2D planar model was constructed in this session to ease the computational cost. Although 3D model can guarantee solution with better accuracy, fine-meshed 2D model is sufficient to visualize appropriate result and can be used to refine future model of 3D model (Illés, 2014).

The specifications of a Cu pillar type FC was adapted from literature by Chen et al., (2014). The Cu pillar bump in this FC has dimension of ⌀ 105 × 45 µm and pitch of 162 µm. The solder cap height is 25 µm. Detailed actual dimension of the FC package is

tabulated in Table 3.4. With this information, a computational domain of a simplified FC assembly was constructed, as shown in Fig. 3.8.

Table 3.4 Dimensions of the Cu pillar bump type FC package

Item	**Dimension**
Die size (mm^3)	10 × 10 × 0.76
Substrate size (mm^3)	31 × 31 × 1.08
Pitch (µm)	162
Solder mask thickness (µm)	5
Solder mask opening (µm)	80
Pillar diameter (µm)	105
Pillar height (µm)	45
Solder cap height (µm)	25
Count	2132

Adapted from Chen et al., (2014)

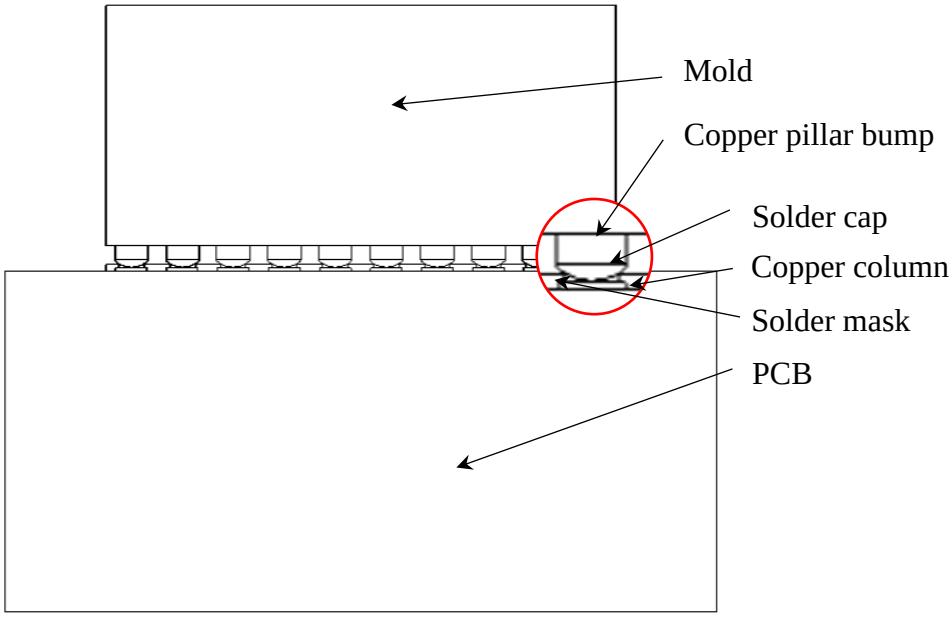


Figure 3.8 Schematic illustration of simplified FC assembly

The surface mesh of the model was generated by using ANSYS Meshing. Similarly, the mesh density is higher around the solder cap, and tetrahedral mesh was used to create the volume mesh, as shown in Fig. 3.9. The total number of nodes in this mesh is 57434