THERMAL MANAGEMENT IN STACKED DIES
(*PENGURUSAN HABA DALAM DAI BERTIMBUN*)

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DECLARATION

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree

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This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by giving explicit references. All bibliography/references are appended.

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Last but not least, I dedicate this work to my parents who have been the beacon of light throughout his project and for bringing me to where I am today. This project would never have been completed without their support.

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NOMENCLATURE

ASIC	Application-specific integrated circuits
CSP	Chip scale package
CTE	Coefficient of thermal expansion (1/K)
DIP	Dual-in-line package
DRAM	Dynamic random access memory
DSP	Digital signal processors
FBGA	Fine Pitch Ball Grid Array
FEA	Finite element analysis
FEM	Finite element method
IC	Integrated circuit
LBGA	Low-Profile Ball Grid Array
LCD	Liquid-crystal display
LLP	Leadless Leaded Package
LQFP	Low-Profile Quad Flat Package
MB	Megabyte
MCM	Multichip module
MLC	Multi-level cell
OEM	Original equipment manufacturer
PCB	Printed circuit board
PSRAM	Pseudo static random access memory
QFP	Quad Flat Package
RAM	Random access memory
SCSP	Stacked chip scale packaging
SIP	System-in-package
SRAM	Static random access memory
TE-PBGA	Thermally Enhanced-Plastic Ball Grid Array
3-D	Three-dimensional

ABSTRAK

Aliran dalam pakej litar bersepadu pada masa terdekat ini, yang menuju ke arah pengurangan dalam saiz dan penambahan fungsi dalam pakej litar bersepadu, telah mencetuskan keperluan untuk mengintegrasikan dai secara vertikal di dalam sebuah pakej tunggal. Penambahan fungsi dan kapasiti melalui pakej dai bertimbun yang meliputi luas tapak yang sama dengan pakej dai tunggal bermaksud pakej dengan kuasa yang lebih tinggi dan ini mencetuskan isu-isu terma. Kajian ini telah dijalankan akibat daripada tercetusnya minat akan kecenderungan taburan terma dan tegasan dalam pakej elektronik untuk berubah dengan beban kuasa yang berbeza-beza ke atas dai-dai silikon. Hasil penemuan daripada kajian ini adalah sangat bermakna terutamanya dari aspek pengurusan terma kerana salah satu cabaran pada masa kini adalah untuk menyingkirkan haba daripada pakej dai bertimbun secara efektif. Kajian ini telah dijalankan dengan bantuan ANSYS^{TM} 7.0 sebagai satu media simulasi dan analisis. Taburan suhu dan tegasan di dalam pakej dai bertimbun di bawah kuasa yang berbeza-beza telah dikaji. Tegasan terma dalam pakej elektronik adalah hasil daripada perbezaan dalam kadar pengembangan haba bagi setiap bahan dalam pakej. Dalam semua kes, suhu maksimum dan tegasan didapati berkadar terus dengan jumlah kuasa yang dikenakan kepada pakej. Suhu maksimum didapati tidak bergantung kepada nisbah agihan kuasa kepada dai-dai dalam setiap pakej. Peningkatan dalam suhu maksimum dengan jumlah kuasa semakin berkurangan daripada pakej dai tunggal kepada pakej empat dai bertimbun. Papan litar menyediakan suatu laluan konduksi bagi penyingkiran haba secara efektif dari bahagian bawah pakej ke persekitaran, seperti mana yang terbukti dalam keputusan simulasi yang diperoleh.

ABSTRACT

The present trend in integrated circuit (IC) packaging, geared towards reduction in size and higher functionality in IC packages, has called about the need for integrating dies vertically in a single package. Added functionality and capacity of stacked dies packages within the same footprint as a single die package practically means higher power densities packages, and this is where thermal issues arise. Through the present study, it is of utmost interest to determine how the temperature and stress distribution within the package varies with the different loads of power applied in the silicon dies. The findings from the present study are of in-depth meaning particularly in the thermal management aspect because the challenge arises in attempting to remove heat efficiently from stacked dies packages. The research study is facilitated with ANSYS^{TM} 7.0, which is used as a finite element modelling and analysis tool. The temperature and stress distribution in stacked dies packages under different source power is studied. Thermal stresses are induced in the package as a result of mismatch in the coefficient of thermal expansion (CTE) properties of the various package materials. Warpage of the package is to be limited to avoid the loss of electrical and mechanical connections. For all cases, the junction temperature and stress increases linearly with total power generation rates in the package. The junction temperature in each package is found to be independent of the power splitting ratios among the dies. The increment in junction temperature with respect to total power decreases from the single die package to the four stacked dies package. The printed circuit board provides a conduction path for effective heat removal from the bottom of the package to ambient as proven from the simulation results.

Chapter 1

INTRODUCTION

1.1 General

Over the last thirty years, we had witnessed progressive evolutions taking place in the field of electronics packaging, from simple Dual-In-Line Packages (DIP) to more complex structures of Chip Scale Packages (CSP) and packages with solder balls. Such significant advances in the subject of electronics packaging typically highlight the enthusiasm inside researchers to satisfy the ever-increasing challenges in Integrated Circuit (IC) packaging requirements which emphasize, among others, for high-performance and low cost packages.

Until now, microsystems packaging has always been geared towards ever-greater miniaturisation and the fact that package sizes are currently progressively approaching the size of the chip or chips it packages justifies the above statement. More recently, people are starting to look into stacking one or more bare dies on top of one another like a sandwich, in which the bare dies are connected and subsequently packaged as a single subject. The convergence of smaller electronic products but with added functionality in the communications and computing genre has been the driving force for the development of die stacking technology.

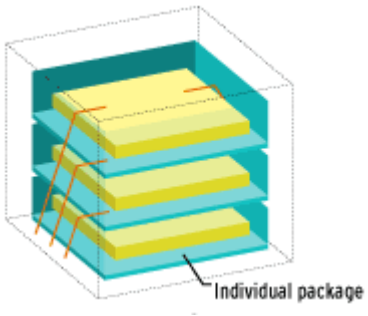

Figure 1.1: Typical arrangement of a stacked dies package [21]

1.2 Advantages of Stacked Dies

The need for die stacking technology arises because people are always interested in pushing the amount of silicon chips that can be integrated in a given package footprint area to obtain more functionality compared to single chip packages. Prior to die stacking, people have been resorting to multichip modules (MCM) or packaging to enhance the functionality characteristics in a packaged device. MCM is a single package which consists of two or more dies working together as a system building block [6].

In MCM, two or more individual dies are interconnected on a common substrate at a minimal spacing between them to achieve higher packing density, thus achieving better performance density per unit cost. While the advantages of both stacked dies and MCM are relatively similar, die stacking technology holds an edge over MCM in that the stacked dies occupy a smaller footprint area on the printed wiring board compared to MCM.

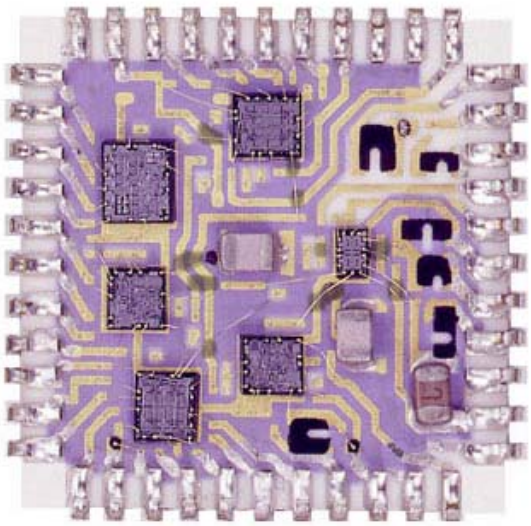

Figure 1.2: Example of a multichip module (MCM) [22]

Die stacking also enhances lower manufacturing costs due to the reduction in board real estate which subsequently contributes to higher packaging efficiency which is highly desirable. Die stacking also reduces packaging costs as a result of eradication of individual IC

packages and the reduction in substrate area. Packages of more conventional designs such as Quad Flat Packages (QFP) only yield a board-level efficiency of approximately 10 %, and although the introduction of CSP and packages with solder balls have certainly led to a significant increase in packaging efficiency of around 50 %, die stacking is expected to further increase the packaging efficiency to greater heights. Packaging efficiency is defined as the area covered by all the base chips to the area of the substrate.

The technique of stacking multiple chips in a given package is also highly favoured because it enhances electrical performance of the package by enabling relatively shorter interconnects routes among the stacked chips. This helps to speed up the electrical signalling between them and packaging costs are further reduced due to shorter substrate wiring length. The noise and time delay effects are greatly reduced in the system due to the shorter interconnects. Noise is defined as undesired signals which can prevent a particular system from operating as intended. Time delay results in a signal travelling from part of the circuit to another not arriving at the receiver instantly due to the combination of resistance and capacitance.

Another advantage is the simplification of the board assembly because stacking dies practically reduces the need for more components to be integrated on the board. Lastly, die stacking enhances the reliability of packaged devices due to the reduction in the number of interconnects between the chip and the board. Higher reliability typically implies lower failure rates and this is vital to ensure that the system functions and operates as intended.

1.3 Applications of Stacked Dies

The application of die stacking technology was initially found in two-chip memory combinations such as flash, dynamic random access memory (DRAM) and static random access memory (SRAM) which remains popular even today. In a typical memory chip package, two or three memory chips are stacked one over another with a thin layer of die attach material in between them. The chips are bonded to die-bond pads on the substrate package with wires.

Die stacking are not confined only to memory chips but has reached out to other applications such as logic and analogue ICs in packages. Die stacking has also paved the way for memory chips to be combined with digital signal processors (DSPs), microprocessors, and application-specific integrated circuits (ASICs) [17]. On a wider note, stacked dies are also used in spacecraft and military programs as well as commercial applications where substantial storage of information is involved.

1.4 Evolution of Stacked Chip Scale Packaging (SCSP)

The year 1998 marked the beginning of the development in die stacking technology when Intel Corporation introduced its first Stacked Chip Scale Packaging (SCSP) which basically consists of only two dies; a 2 MB SRAM die and an 8 MB Flash die contained in a fine pitch ball grid array package (FBGA) measuring 8×10×1.4 mm [16]. The packaging technology in which Intel Corporation had stumbled upon paved the way for handset manufacturers and related original equipment manufacturers (OEMs) to produce smaller forms of products which are equipped with greater memory capacity but with lower consumption of power as can be seen from the figure below.

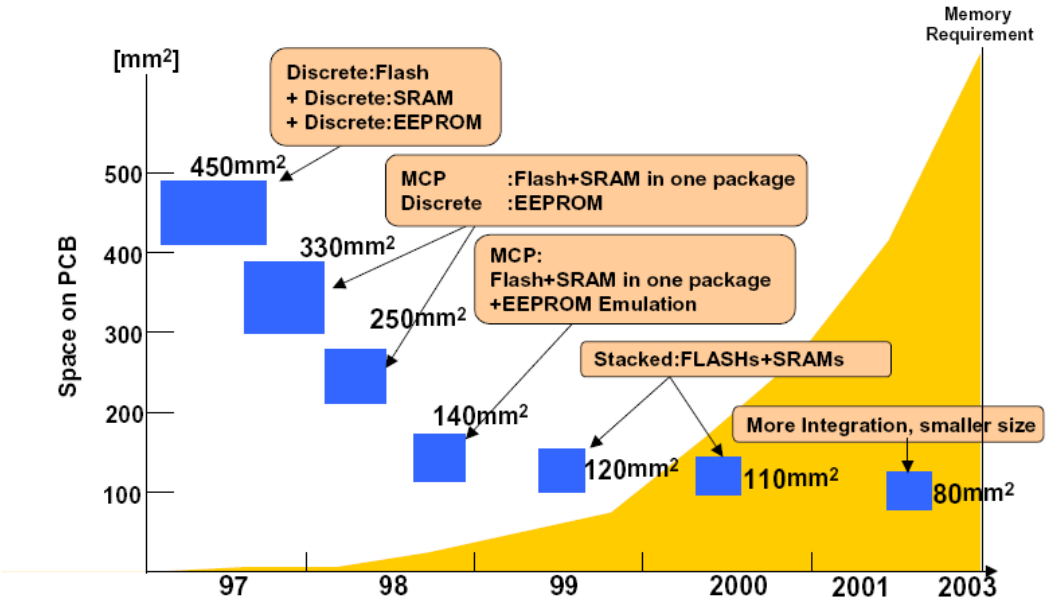

Figure 1.3: Wireless Memory Package Trends [16]

On April 10, 2003, Intel Corporation declared that they had came up with a new Chip Scale Packaging (CSP) technology, in which stacking of a total of five dies with densities of 512 MB Flash, 128 MB Pseudo-SRAM (PSRAM), and 8 MB SRAM in a package measuring 8×11×1.2 mm is made possible. In addition, the amount of memory density is more than 60 times of that combined in almost the same package size. This new technology also marked a reduction in the package of the stacked dies of approximately 50 % because prior to this, Intel Corporation had came up with a four-die stacking technology in which the package heights were 1.6 mm. Simultaneously, thirteen standard packaging products were introduced into the market in which the above technology, dubbed Ultra-Thin Stacked CSP was the driving force behind these products.

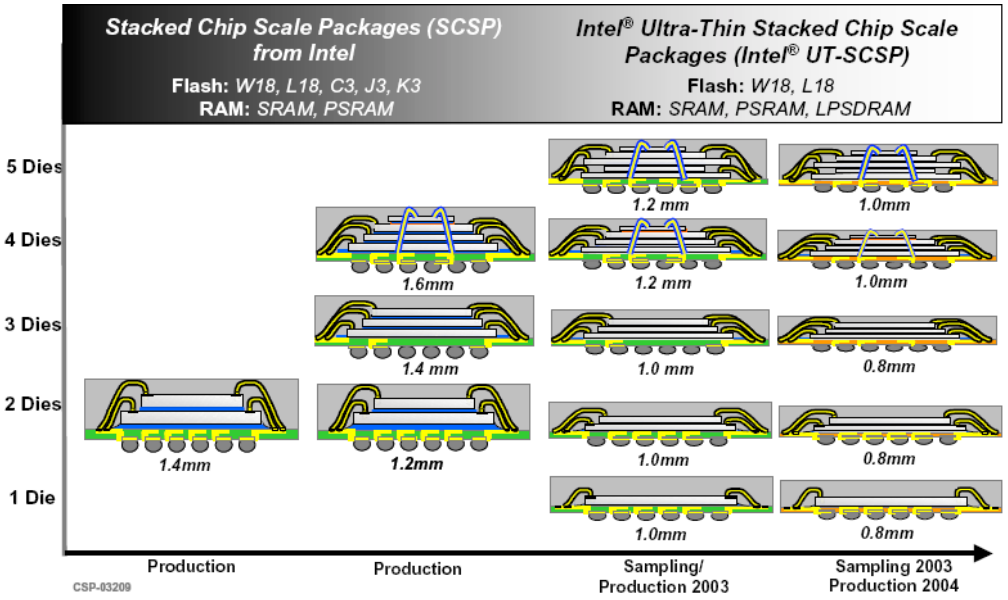

Figure 1.4: Evolution of Stacked Chip Scale Packages (SCSP) from Intel [16]

Among the more obvious applications of the Ultra-Thin CSP can be found in small handsets equipped with multiple functions that include, among others, cameras and colour liquid-crystal displays (LCD). Through to this new discovery also, original equipment manufacturers (OEMs) are now able to stack a combination of different types of chips which includes the multi-level cell (MLC) flash-memory technology dubbed StrataFlash [19]. This

SCSP technology also contributes to the evolution of RAM memory technology because besides SRAM, PSRAM and low power-SDRAM technology are also incorporated in SCSP.

1.5 Thermal and Mechanical Challenges of Stacked Dies Packaging

The emergence of die stacking technology could not have possibly come at a more appropriate timing than at present where people are pushing for higher functionality into a microelectronics package within the same footprint area as before. While stacked dies have much to offer in the microelectronics industry compared to a typical single die package, there are the thermal and mechanical challenges in which one has to address to enhance the performance and reliability of stacked dies packages.

Thermal issues in stacked dies packages are more complex because there are multiple heat sources in which more than one die generates heat. The thermal performance aspect of stacked dies is of great importance to ensure that the packaged dies does not fail under normal operating conditions due to excessive power supply. There is a limitation in the junction temperature in silicon-based semiconductor devices after which if it is being exceeded, failures are bound to take place. Stacked dies packages practically means higher power density packages and a more meticulous approach is necessary to ensure that sufficient thermal energy is being dissipated from the package to ambient.

Thermomechanical failures are bound to take place as a result of stresses and strains induced within the stacked dies due to thermal loading. The existence of these thermally-induced stresses and strains is due to several factors such as geometric limitations, thermal gradients in the system, or the disparity in the coefficient of thermal expansion among different materials. The more common modes of thermomechanical failure mechanisms are creep, interfacial delamination, plastic deformation, and fatigue crack. This has caught the interest of researchers to look into exploring the many options available to minimise, if not eliminate, thermal stresses within the area of a widespread approach towards thermal management.

More recently, people are also beginning to look into stacking dies of similar sizes or stacking larger dies on top of smaller ones as opposed to the previous option of die stacking. In cases of stacking dies of similar sizes, bonding is facilitated by a dummy die (spacer) inserted in between live dies which separates the top and the bottom die at a minimal gap. At the same time, this dummy die also assists in reducing or eliminating unwanted interactions between the live dies. However, the spacer die could pose severe problems related to the stress distribution between the stacked dies due to its material properties and this is one of the many challenges in which researchers are currently trying to overcome [4].

While work on increasing the number of dies that can be stacked in a package is still pretty much the subject of discussion where die stacking technology is concerned, people are also beginning to shift their attention towards reducing the package heights as the number of stacked dies increases. Lower package heights typically imply that thinner silicon wafers are being used to produce the dies needed for stacking; as much as 90 percent of the silicon is removed each time the wafers are being backgrinded and polished [17]. Thinner silicon dies could possibly contribute to the change in maximum stress inside the dies due to the decrease in die bending stiffness.

1.6 Objective

From the literature review, it is observed that minimal effort has been devoted towards studying the thermal and stress characteristics of stacked dies packages under different power loadings. This is despite the fact that many microelectronic devices today utilised substantial amount of power compared to those devices of decades ago. In view of this, there is a need to further investigate this area of interest which also corresponds to the performance and reliability of packages. The objectives of the present study are listed as below:

i. To carry out the thermal and stress analysis on isolated single die and stacked dies packages modelled in ANSYS^{TM} 7.0. The important parameters under investigation are junction temperature, maximum stress, total power generation, and power splitting ratios among the dies.

ii. To determine the various combinations of power generated in dies that will result in acceptable junction temperature desired for the design of the packages.
iii. To identify critical-stress areas as a result of mismatch in the coefficient of thermal expansion (CTE) properties of the package materials.
iv. To carry out the thermal analysis on single die and stacked dies packages attached to the printed circuit board (PCB) to investigate on what extent the board is going to facilitate the heat removal process from a package to ambient as of real life situations.

1.7 Scope of Work

The present study will be dealing with the thermal and stress characteristics of stacked dies packages utilising the three-dimensional finite element analysis (FEA), in which reasonable amount of data will be generated in a systematic manner. A large portion of this study will be devoted towards finding the temperature and stress distribution in isolated single die and stacked dies packages modelled in ANSYS^{TM} 7.0, one of the many commercial FEM software packages available in market. Finite element method (FEM) based computer simulations are highly favourable in conducting advanced analysis because the results can be readily obtained in a reasonable time frame, thus minimising development costs.

For intended safe and highly reliable operation, the junction temperature in microelectronics packages is restricted to approximately 125ºC. On this basis, simulations which result in junction temperatures beyond 400 K will not be carried out. The present study will also be investigating the change in junction temperature with respect to power splitting ratios among the silicon dies which will be of great importance to the microelectronics industry, especially in the design of high power density packages. The single die and stacked dies packages modelled correspond to isolated packages

The temperature distribution in stacked dies packages under different loadings of source power will be of great interest because this temperature variation can lead to stress concentration in the package as a result of mismatch in the coefficient of thermal expansion (CTE) properties of the various package materials involved in the construction of a typical

package. Past researchers works had indicated that under thermal loading, the package will either bend upwards or downwards. There is a maximum deflection in which the warpage of the package is allowed to occur in which the distortion of the package beyond this limitation can pose severe problems pertaining to the reliability of the package.

The approach of thermal management also ensures that the IC packages are sustained within their operational and maximum allowable boundaries. Researchers are coming up with various designs of stacked dies, which include among others, different die dimensions and the arrangement of stacked dies, to meet the increasing demand for optimal thermal performance. Subsequently, the present study will also be looking into the role of the printed circuit board (PCB) as a conduction path in removing heat effectively from the bottom of the package to ambient. It is of greatest hope that the present study would be of help and facilitate current works undergoing in the aspect of thermal management in stacked dies.

Chapter 2

LITERATURE REVIEW

Technology demand for smaller but more functionality embedded in a package promotes the use of existing technology optimisation which supports the concept of die stacking as a viable solution. A wide variety of literature is scanned for research work carried out on multiple integrated circuits (ICs) stacked within a single package, a packaging technology which is on the rise, particularly on issues regarding thermal management in stacked dies. Although the search results indicate that substantial amount of work has been conducted in this area, there was no specific study which coincides with the present study.

2.1 Packaging Challenges and Solutions for Multi-Stack Die Applications

Chylak et al. (2003) addressed the challenges of stacked dies package with advances in wafer thinning, wire bonding, molding, and other packaging and assembly areas. Since two or more dies are incorporated into a single package, this typically implies that every dimension of the package attributes such as the die thickness, the mold cap thickness, the bond line thickness, and the wire bond loop profile has to decrease. The authors also conducted a study on the interconnect requirements in stacked dies, in which technologies including forward ball bonding, reverse ball bonding, and stud bumping for flip chip applications were reviewed. Developments in ball bonder capabilities, which comprise of ultra-low loop shapes, long wire spans, and overhang bonding, were presented. The authors summed up by proposing packaging design guidelines to address critical design and assembly issues.

2.2 Thermal Characterisation of Stacked Dies Packages

Li et al. (2004) evaluated the thermal performance of stacked dies package through a comprehensive testing and modelling test samples built on four popular packaging platforms which include a 7 mm 44L Leadless Leaded Package (LLP), a 15 mm 196L Low-Profile Ball Grid Array (LBGA), a 20 mm 144L Low-Profile Quad Flat Pack (LQFP), and a 35 mm 388L

Thermally Enhanced-Plastic Ball Grid Array (TE-PBGA). It is relatively difficult to define thermal resistance in a stacked dies package because the temperature of multiple dies needs to be measured at various power level combinations. The authors carried out a thermal analysis by relating the junction temperature and board temperature of the stacked dies packages to the thermal resistance values of equivalent single die packages.

2.3 Structure Function Evaluation of Stacked Dies

Rencz et al. (2004) utilised the structure function evaluation methodology to detect the thermal properties of various layers in the heat flow path. The authors also demonstrated how the above methodology could be conveniently applied to detect the location of die attach layers in stacked die structures of up to four silicon layers. This methodology holds an advantage over other methods because there is no requirement for any additional circuit elements on any of the dies of the stacked dies structure. The feasibility of the method, both for stacked die structures of the same die size, and for pyramidal stacked die packages were presented, in which it was discovered that the method works well in both cases. The method presented enables fast diagnosis of the die attach problems of stacked dies and does not require any additional circuit elements in any of the stacked dies.

2.4 Stacked-Chip Packaging: Electrical, Mechanical, and Thermal Challenges

Awad et al. (2004) addressed the electrical, mechanical, and thermal challenges associated with stacked dies packaging. The authors demonstrated the role of modelling and simulation in package design to subdue these challenges while improving the overall module performance in a shorter time frame. Recent demands for stacked dies packages typically suggest that people should start looking into the possibility of performing a thorough electrical, mechanical, and thermal analysis of the stacked dies package which is of great importance from the package's reliability point of view. The authors carried out a thermal analysis on a Pin Ball Grid Array (PBGA) package consisting of two dies in which they discovered that the junction temperature and the temperature distribution of both dies were

almost similar. The authors concluded that for such package design, the low-power die will achieve a temperature close to that of the junction temperature of the adjacent die.

The authors also carried out a study on the transient performance of the stacked dies package. Since the thermal diffusivity of the silicon is much higher than that of the mold compound, a space occupied by the die can act as a temporary heat sink when the power is switched on. Simulations were also carried out that compared a dual-chip package in which both dies were wirebonded with another package in which only the top die was wirebonded while the bottom die was attached with gold-stud bumps. The authors discovered that there were no variations in the junction temperature for both cases in the flip chip situations.

Chapter 3

METHODOLOGY

3.1 Introduction

A finite element analysis (FEA) approach is utilised to predict the temperature and the stress distribution in single die and multi die stacked packages at different combinations of power generation. The finite element method (FEM) is a numerical approach commonly used for obtaining approximate solutions to many of the problems faced in engineering analysis in which the results can be readily obtained in a reasonable time frame and effort.

ANSYS^{TM} 7.0, one of the many commercial FEM software packages available in market, is used as a finite element modelling and analysis tool. ANSYS^{TM} 7.0 is highly regarded in analysing complex problems in areas of mechanical structures, thermal processes, and computational fluid dynamics. ANSYS^{TM} 7.0 is capable of providing a complete detailed description of temperature and stress distribution in packages and a rich graphics capability that can be utilised to display results obtained on a high-resolution graphics workstation.

3.2 Single Die and Stacked Dies Packages

Three typical stacked dies packages, each measuring 14 × 11 mm are analysed. These packages consist of dies stacked vertically ranging from two to four dies. A typical single die package bearing similar dimensions is also analysed to study how integrating dies vertically in a single package would contribute to the changes in temperature and stress distribution within the package. In all four packages, each silicon die is measured at 12 × 9 mm. The outline drawing of the package, which applies to all the packages involved in this problem study, is depicted in Figure 3.1.

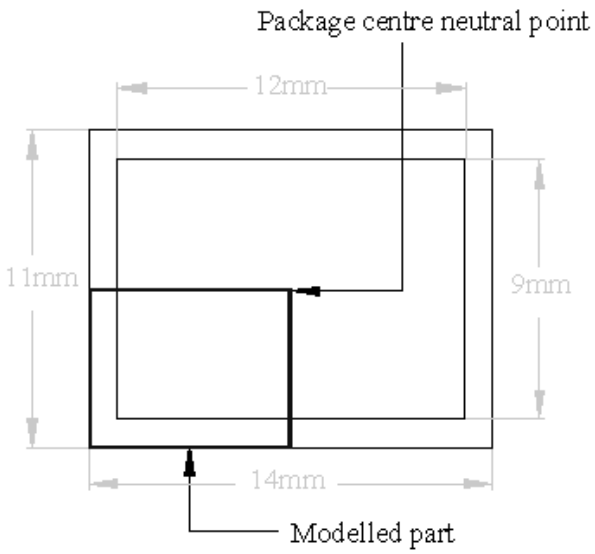

Figure 3.1: Package outline drawing

The basic structure of a single die package is illustrated in Figure 3.2. The basic structural layer layout of the typical single die package consists of a silicon die, with a thickness of 0.100 mm, which is attached to the substrate via the die attach layer while the mold encompasses the silicon die. The substrate has a thickness of 0.200 mm while the die attach is 0.025 mm thick. The mold possesses a thickness of 0.425 mm from the substrate. The stack-up layer dimensions of the single-die package is depicted in Table 3.1.

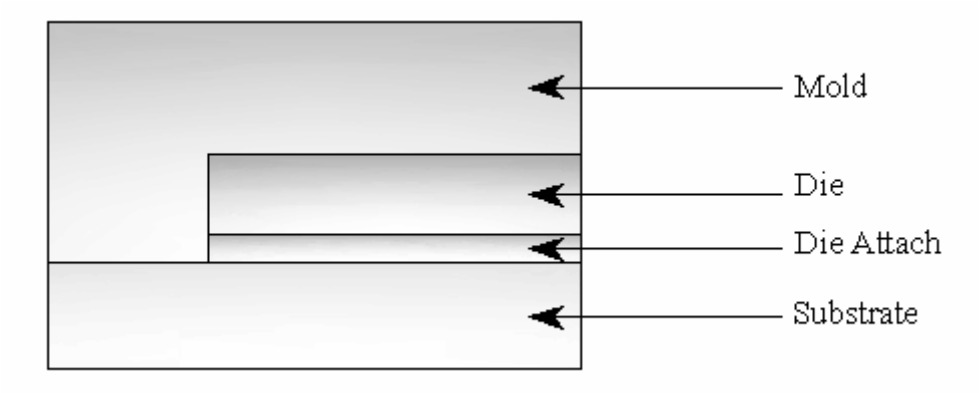

Figure 3.2: Basic structure of a single die package

The basic structure of a typical stacked dies package consisting of two dies is depicted in Figure 3.3. The top die is attached to the bottom die via the die attach layer while the bottom die is subsequently attached to the substrate through the die attach layer. The mold encapsulates both the top and bottom die. Both the dies are 0.100 mm thick. The substrate has a thickness of 0.200 mm while the die attach is 0.025 mm thick. The mold possesses a thickness of 0.550 mm from the substrate. The stack-up layer dimensions of the stacked dies package consisting of two dies is summarised in Table 3.1.

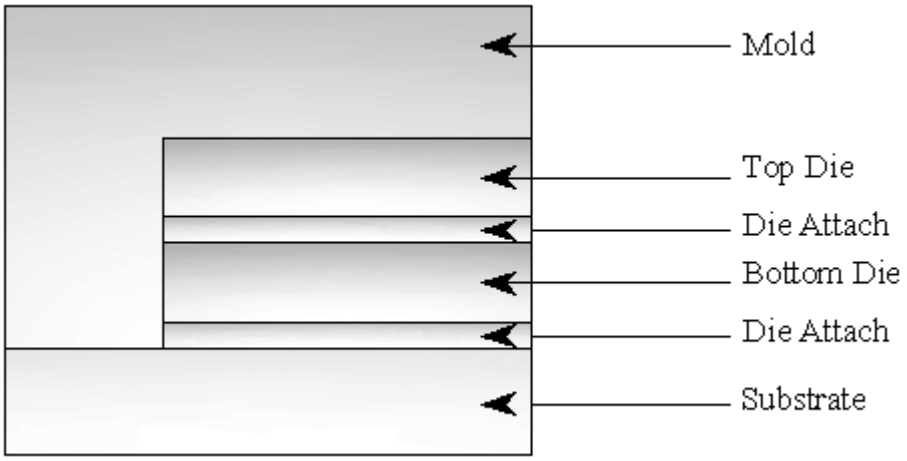

Figure 3.3: Basic structure of a stacked dies package consisting of two dies

Similarly, the basic structure of a typical stacked dies package consisting of either three of four dies is akin to that shown in Figure 3.3, with additional dies being stacked vertically above the top die. The dimensions of the substrate, silicon dies, and die attach layers are similar to that of the previous two packages. The mold of the three stacked dies package possesses a thickness of 0.675 mm from the substrate. In the case of the four stacked dies package, the mold is 0.800 mm thick from the substrate. The stack-up layer dimensions of the stacked dies packages consisting of three dies and four dies is depicted in Table 3.1.

Table 3.1: Stack-up layer dimensions of the single die and stacked dies packages

Package Attribute		Dimension (mm)			
		Single die	**Two stacked dies**	**Three stacked dies**	**Four stacked dies**
Substrate	Thickness	0.200	0.200	0.200	0.200
	Size	14 × 11	14 × 11	14 × 11	14 × 11
Silicon Die	Thickness	0.100	0.100	0.100	0.100
	Size	12 × 9	12 × 9	12 × 9	12 × 9
Die Attach	Thickness	0.025	0.025	0.025	0.025
	Size	12 × 9	12 × 9	12 × 9	12 × 9
Mold	Thickness	0.425	0.550	0.675	0.800
	Size	14 × 11	14 × 11	14 × 11	14 × 11

3.3 Single Die and Stacked Dies Packages with Printed Circuit Board (PCB)

The models of single die and stacked dies packages described earlier all correspond to isolated packages. It is also of great interest to study on what extent the total maximum power generated in the package will be enhanced with the inclusion of the printed circuit board (PCB). Substantial amount of heat is dissipated through the printed circuit board because the board practically introduces a mean of conduction path from the bottom of the package to ambient, besides providing electrical connections between the package and the board. People have witnessed the evolution of printed circuit board assembly process from through-hole assembly to surface mount assembly.

Through-hole packages, which are products of through-hole assembly, refer to those packages equipped with leads that can be inserted into plated holes in the board. Meanwhile, surface mount packages, which are products of surface mount assembly, are packages that are mounted on the surface of the board. Surface mount packages hold the advantage over through-hole packages in view of the higher packaging density they can achieve because it is possible to utilise both sides of the printed circuit board.

All four packages as described earlier in the previous section are analysed with the introduction of solder balls at the bottom of the substrate into this thermal analysis which form

the interconnection between the package substrate and the printed circuit board. A total number of 192 solder balls (16 ×12 full ball matrix) at 0.80 mm pitch are located at the bottom of the package which is subsequently attached to a 50 ×50 mm board with thickness of 0.5 mm. Each solder ball has a stand-off height of 0.30 mm and diameter of 0.40 mm. The outline drawing of the package attached to the printed circuit board, which applies to all the packages involved in this problem study, is depicted in Figure 3.4 while the basic structure of a typical single die package mounted onto a printed circuit board is depicted in Figure 3.5.

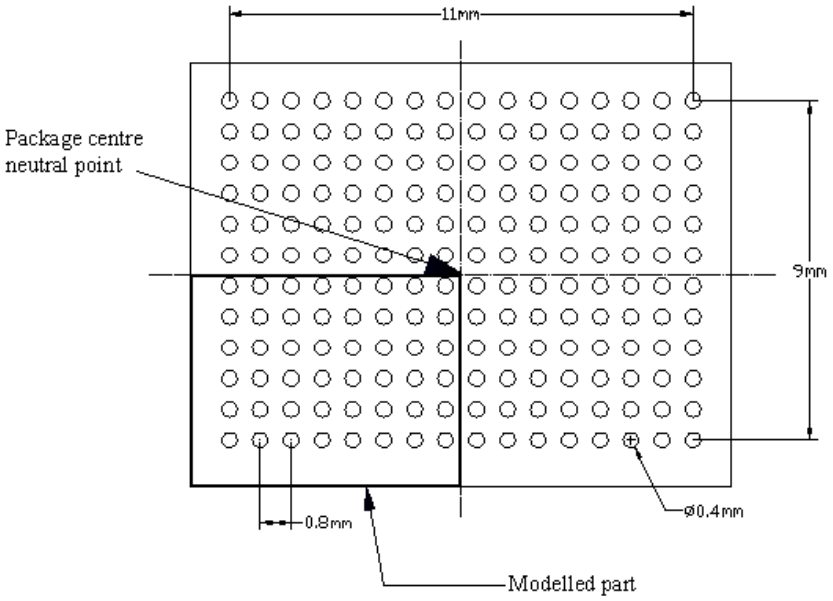

Figure 3.4: Package outline drawing of package attached to PCB

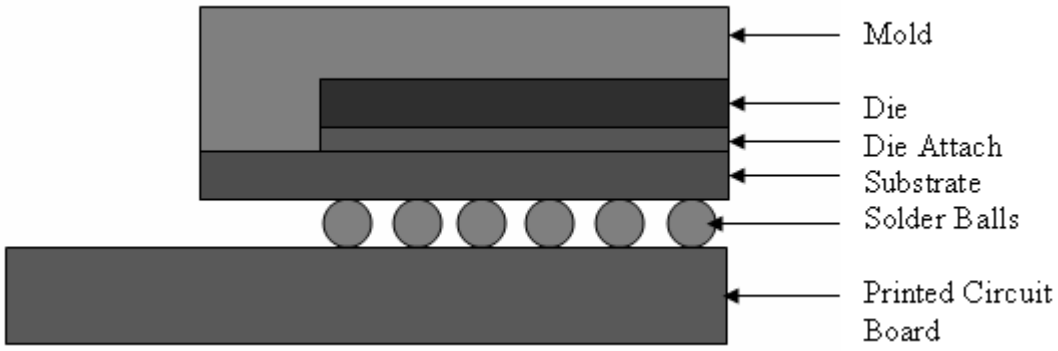

Figure 3.5: Basic structure of a single die package attached to PCB

3.4 Modelling

Based on the dimensions of the package attribute, three-dimensional models of single die, two stacked dies, three stacked dies, and four stacked dies package are assembled utilising ANSYS^{TM} 7.0. Since there is symmetry existence in the packages, only one-fourth of the entire assembly is modelled for the thermal-stress simulations to reduce modelling complexity and to facilitate reasonable simulation run times. A coupled-field analysis is carried out because the input of the stress analysis depends on the results from the thermal analysis of the models under study.

The model is first created in the thermal environment with SOLID70 elements which has a three-dimensional thermal conduction capability and has 8 nodes with a single degree of freedom, temperature, at each node. The need for remodelling of the packages in structural environment does not arise because the geometry is kept constant although the element type is switched from SOLID70 to SOLID45, a three-dimensional structural element defined by 8 nodes having 3 degree of freedom at each node: translations in the nodal x, y, and z directions.

For the second part of the analysis involving the single die and stacked dies packages attached to the printed circuit board by means of solder balls, the models of the packages and the printed circuit board are created in the thermal environment with SOLID70 elements. Many researchers, who have been working on predictions of solder joint fatigue life, utilised a viscoplactic finite element simulation methodology in which the solder balls are created with VISCO elements since the deformation behaviour experienced by the solder balls under high homologous temperature is linked with the irreversible, temperature and rate dependent inelastic characteristics [5]. However, the modelling of solder balls with VISCO elements are meant for other areas of interest and takes up substantial amount of simulation time. Thus, it is reasonably logical to lump the solder balls in this thermal analysis and represent these balls by means of a block modelled with SOLID70 elements. This simplification is further justified by the fact that the degree of freedom under study in this analysis, which is temperature, is a scalar quantity.

3.5 Material Properties

The material properties of the package attributes for the stress analysis are depicted in Table 3.2. The substrate is modelled as an orthotropic linear elastic solid while the remaining materials are modelled as isotropic linear elastic solids. This is because the substrate is made up of many different layers of materials and thus, the material properties are no longer independent of direction. As such, the substrate may possibly have different elastic constants, such as Young's modulus, Poisson's ratio, and shear modulus, in the three principle directions.

The properties utilised in the analysis are independent of temperature; the material properties are assumed to be constant although there is a change in temperature. The material properties of the silicon die, die attach, mold, and substrate for the thermal analysis are depicted in Table 3.3. The thermal conductivity of all the elements has been taken as isotropic properties.

Table 3.2: Material properties used in the package models for stress analysis

Package Attribute	**Material Properties**			
	Young's Modulus (MPa)	**CTE (10^{-6}/ºC)**	**Poisson's Ratio**	**Shear Modulus (MPa)**
Substrate	22000 (X)	18	0.28 (XY)	1520 (XY)
	10000 (Y)	70	0.11 (YZ)	1520 (XY)
	22000 (Z)	18	0.28 (XZ)	152 (XZ)
Silicon Die	131000	2.8	0.30	-
Die Attach	310	155	0.30	-
Mold	6000	30	0.35	-

Table 3.3: Material properties used in the package models for thermal analysis

Package Attribute	**Thermal Conductivity (W/m·K)**
Substrate	1.2
Silicon Die	120
Die Attach	0.3
Mold	0.712
Circuit Board	50.2

3.6 Meshing

Once a quarter of the entire package has been successfully assembled utilising ANSYS™ 7.0, the element attributes established earlier such as element type and material properties are assigned to the appropriate elements of the model. All four models utilised a mapped or structured finite element mesh because the entire volume of the models resemble the shape of a brick. A mapped mesh is constrained in terms of the element shape it constitutes and the pattern of the mesh. For the second part of the analysis where the packages are mounted onto the printed circuit board, all four models utilised a free mesh due to the complexity of the geometry which constrained the utilisation of mapped mesh. The finite element mesh of the model is generated once the meshing controls have been set.

The mesh element size is determined appropriately to avoid the existence of poorly shaped elements with poor aspect ratios or poor Jacobian ratios. Elements that are badly shaped can occasionally result in very poor results. The number of elements and nodes, in which all four quarter models are comprised of after meshing is carried out, is depicted in Table 3.4. The quarter model of the entire single die package, two stacked dies package, three stacked dies package, and four stacked dies package, with and without the printed circuit board, are illustrated in subsequent figures together with their resulting meshes.

Table 3.4: Number of elements and nodes in all four packaging models

Packaging Models	Analysis	Number of Elements	Number of Nodes
Single-die	Without PCB	5290	6336
	With PCB	26587	6005
Two-stacked dies	Without PCB	6877	8064
	With PCB	37021	8040
Three-stacked dies	Without PCB	8464	9792
	With PCB	47267	10094
Four-stacked dies	Without PCB	10051	11520
	With PCB	57382	12125

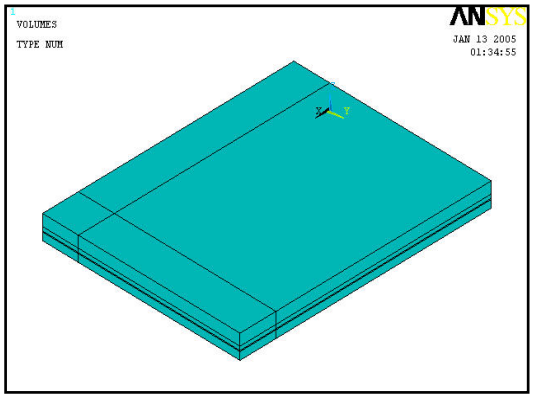

Figure 3.6: Quarter model of a typical single die package

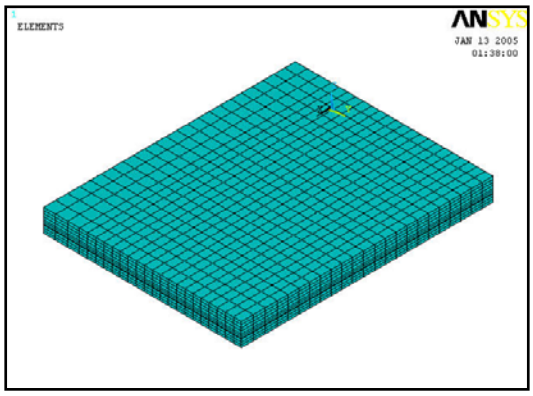

Figure 3.7: Meshed quarter model of a typical single die package

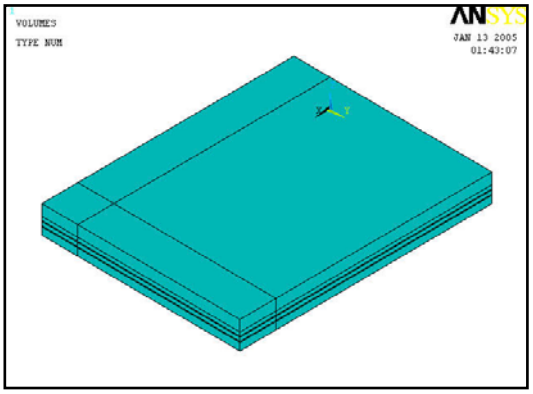

Figure 3.8: Quarter model of a typical two stacked dies package

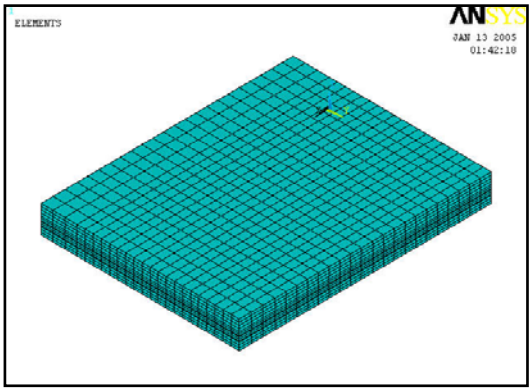

Figure 3.9: Meshed quarter model of a typical two stacked dies package

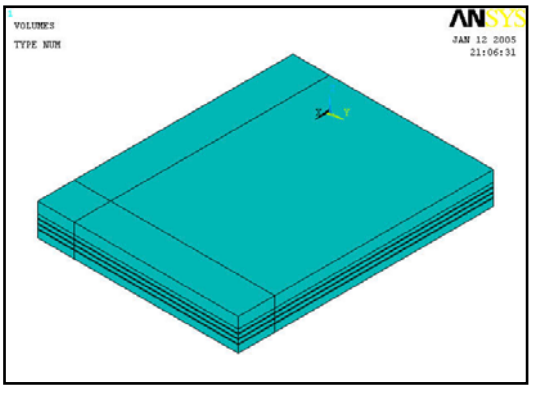

Figure 3.10: Quarter model of a typical three stacked dies package

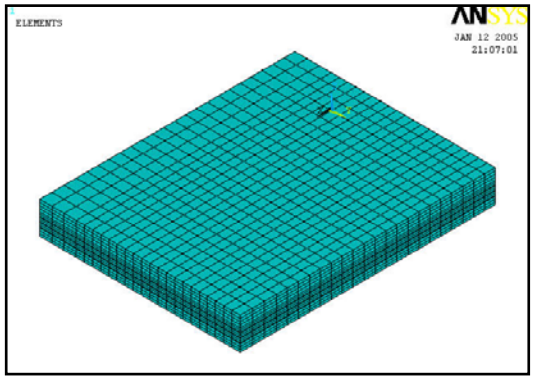

Figure 3.11: Meshed quarter model of a typical three stacked dies package

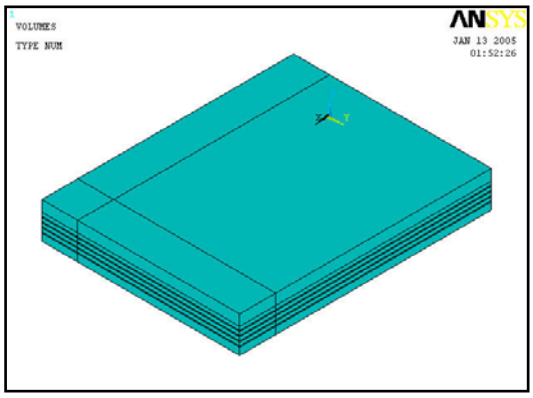

Figure 3.12: Quarter model of a typical four stacked dies package

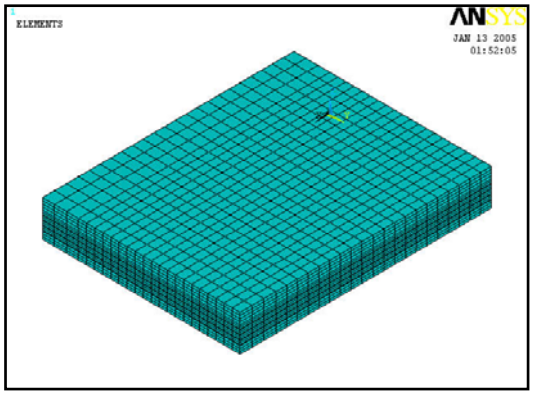

Figure 3.13: Meshed quarter model of a typical four stacked dies package

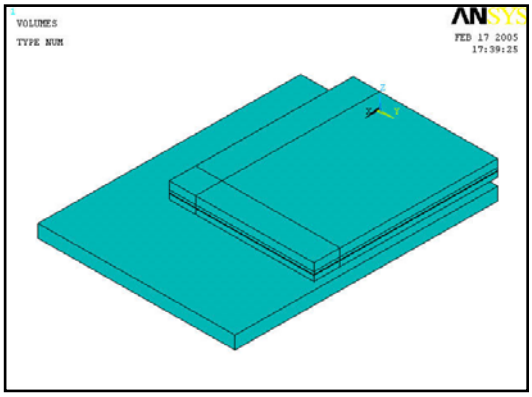

Figure 3.14: Quarter model of a typical single die package with PCB

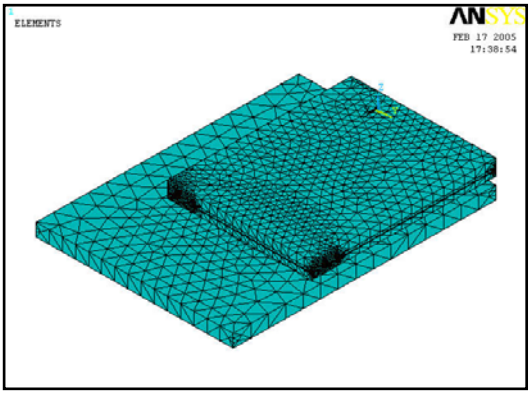

Figure 3.15: Meshed quarter model of a typical single die package with PCB

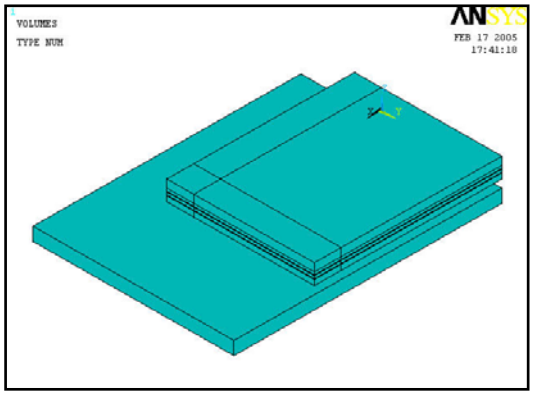

Figure 3.16: Quarter model of a typical two stacked dies package with PCB

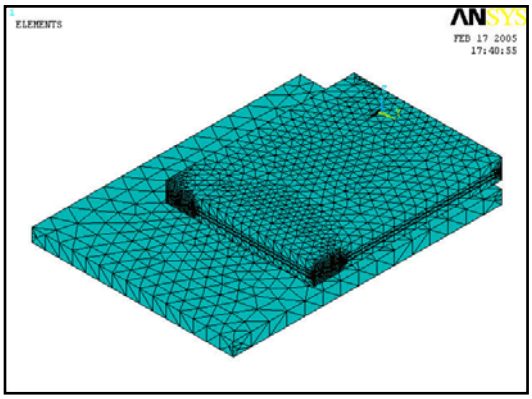

Figure 3.17: Meshed quarter model of a typical two stacked dies package with PCB

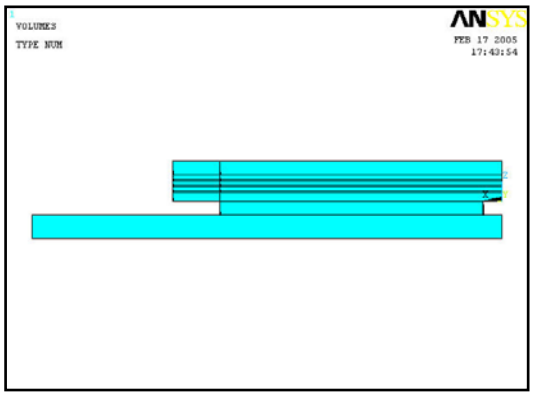

Figure 3.18: Quarter model of a typical three stacked dies package with PCB

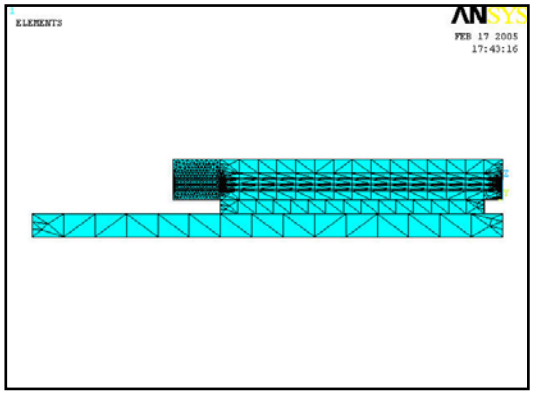

Figure 3.19: Meshed quarter model of a typical three stacked dies package with PCB

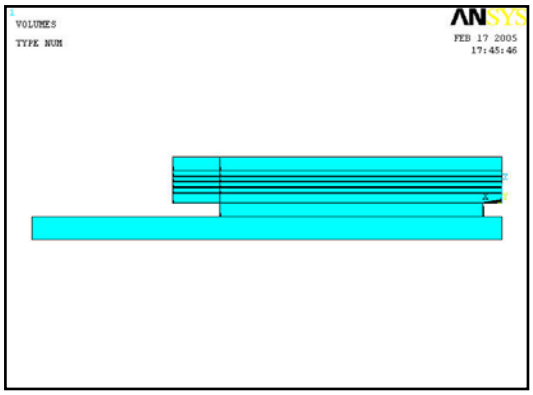

Figure 3.20: Quarter model of a typical four stacked dies package with PCB

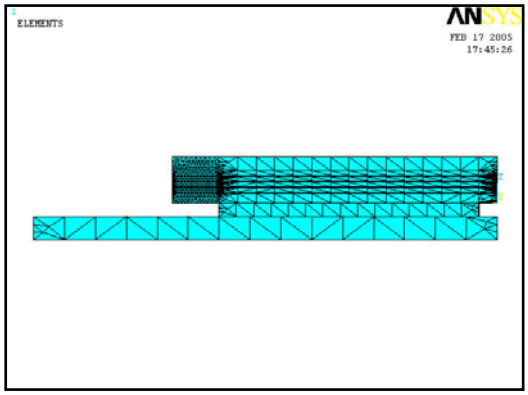

Figure 3.21: Meshed quarter model of a typical four stacked dies package with PCB

3.7 Boundary Constraints of the Model

The model of the package configured in ANSYS™ 7.0, which constitutes a quarter of the entire package, is sufficient in taking into consideration all components of the package under study. However, it has to be noted that the utilisation of one-quarter model in simulations calls for the need of proper consideration of boundary conditions that has to be constrained on the model. Without doubt, the consideration of these boundary constraints is clearly a representation of the actual boundary constraints by which the actual assembly of the package is fully subjected to. The boundary constraints applied to all the four packages, whether it is a single die package or a stacked dies package, is practically similar and is clearly represented in one of the models as depicted in Figure 3.22.

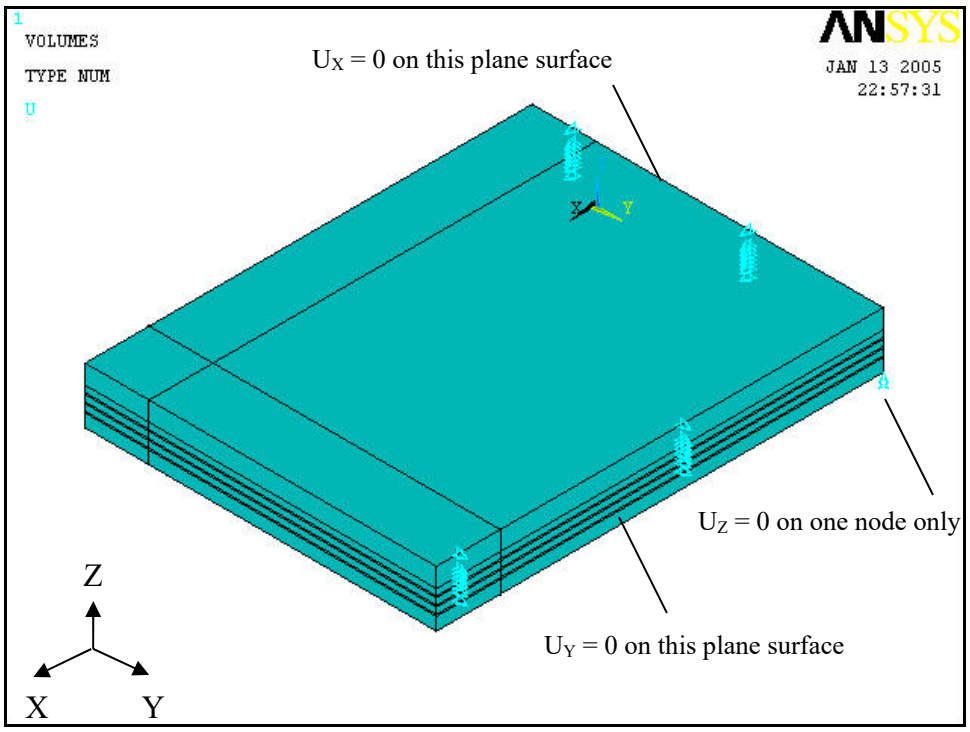

Figure 3.22: Boundary constraints applied to a typical three stacked dies package

The surface of the one-quarter model which slices across the silicon die and normal to the x-axis is refrained from moving in the x-direction, while the surface which