REKABEBTUK PENGUAT HINGAR RENDAH (LNA) CMOS BERARUHAN MEROSOT BEBEZAAN PENUH UNTUK PENERIMA WCDMA

Oleh

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ABSTRAK

Projek ini adalah berkaitan penghasilan rekabentuk satu penguat hingar rendah (LNA) menggunakan 0.18-m CMOS process. Litar LNA yang direkabentuk adalah beroperasi pada nilai voltan yang rendah 1.8V. Frekuensi operasi pula adalah 2.1 GHz. Penggunaan arus adalah kurang iaitu hanya 12.66mA dengan angka hingar 1.7dB pada galangan masukan sumber 50Ω. Gandaan kuasanya ialah sebanyak 11.42dB. Topologi induktor punca merosot telah digunakan kerana ia menghasilkan hingar yang rendah berbanding seni-seni lain.

Bagi satu LNA, hingar dan sifat lelurus adalah ciri-ciri kritikal. Litar kebezaan penuh dengan penggunaan induktor merosot digunakan kerana topologi ini dapat mengurangkan hingar seperti hingar harmonik tertib genap. Titik kompressi 1dB bagi LNA yang direkabentuk adalah -9.82dB.

Masalah utama yang dihadap adalah membekalkan galangan masukan sumber pada 50Ω di samping mengekalkan gandaan pada julat 10-15dB.

LNA yang direkabentuk berjaya menemui semua spesifikasi.

ABSTRACT

A 2.1 GHz low noise amplifier (LNA), intended for use in a Wide-band Code Division Multiple Access (WCDMA) receiver has been implemented in 0.18μm RF process. The amplifier provides a forward gain (S_{21}) of 11.42dB with a noise figure of only 1.7dB and drawing 12.66mA from a 1.8V supply voltage. The 1dB-compression point of the LNA is -9.82dB. In this thesis, detailed analysis of the LNA architecture will be presented.

The LNA employed an inductive source degeneration topology, that is, a degenerative inductor is used to provide 50Ω input impedance matching. An advantage of this method is that unlike other methods, it does not bring with it the thermal noise of an ordinary resistor because a pure reactance is noiseless. This LNA uses differential architecture rather than single-ended architecture to provide better common-mode rejection ratio.

The main problem faced in the project was to obtain a 50Ω input and output impedance while maintaining the gain to be in the range of 10dB to 15dB. This gain specification is to ensure that the LNA provide enough gain but not too high as to avoid nonlinearity that can cause distortion.

LNA should not consume too much power to have good portability.

Finally, the performance of the designed low noise amplifier meets all of the specification.

APPRECIATION

First of all, I want to take this opportunity to say thank you to my final year project supervisor, Pn. Norlaili for the opportunity to work on an interesting research topic and her encouragement and guidance during the research. I also want to say thank you to Dr. Tun Zainal because he gave me some idea to carry out the research.

Throughout this project, Mr. Harikrishnan gave me a lot of guidance. My teammates, who are also doing the research for the WCDMA direct conversion front-end receiver, are also not selfish to share their knowledge with me. They also give me the encouragement to complete my project.

For all my course mates who have accompany me for 4 years in USM, thanks for your accompany and encouragement.

Finally, thanks to my family who gave me a lot of support all these years.

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Chapter 1

INTRODUCTION

1.1 Project Objective

The main purpose of this project is to design a Low Noise Amplifier (LNA), that has an operating frequency in the range of 2110MHz-2170MHz. The input impedance of the LNA has to match 50 ohms for maximum power transfer. It also needs to have noise as low as 2dB. The gain should be around 10 to 15dBto prevent nonlinear distortion. The design was implemented using Siltera's 6 metals 0.18μm technology.

1.2 Motivation for the project

The evolution of current wireless communication systems has been very rapid. The goal has been small-size and low-cost terminals that can be programmed for different applications. Hence, the trend has been towards digital transceivers. The implementation of a "full" digital transceiver is still unrealistic and, therefore, many analog circuits that shape and transform the data are required. In addition, the implementation of future systems sets new challenges for circuit and system level design. The implementation of high data rates in wireless systems may require for example, wide channel bandwidths, continuous-time reception, and, because of the available frequency bands, usually high receive and transmit frequencies (> 2GHz). In addition, new systems should be implemented using low supply voltages without significantly degrading the performance compared to the current systems. Therefore, the design of integrated analog circuits becomes very challenging and new circuit- and system-level solutions will be needed.

The first terminals using 3G wide-band code division multiple access (WCDMA) systems are already available to consumers. These terminals can provide high-speed data connections, thus partly making possible fast and real-time internet connections. At first, these systems will cover urban areas and, in order to maintain a connection to these terminals, the terminal should be able to use other existing systems in rural areas.

However, there are some problems with WCDMA system such as multi-user detection. that performance of CDMA system is limited by multi-access interference (MAI).

Optimum detector can completely eliminate MAI, thus greatly increase CDMA system capacity. However, the complexity of the optimum detector is exponential in number of users, which is too complicate for practical implementation. Therefore, research is still going on as trying to come up with ways of optimizing the system.

In this thesis, the limitations imposed by different types of receiver architectures are described. Without knowing these limitations, it becomes difficult to understand the choices made in the experimental circuits. As for the LNA topology, the inductively-degenerated LNA is the basis for all the experimental circuits. The different components for this configuration are analyzed and compared to other commonly-used configurations in order to justify the use of the inductively-degenerated LNA.

1.3 LNA Introduction

LNA is an important block in the receiver design of RF communication network. LNA is the first building block, whose main function is to provide enough gain to overcome the noise of subsequence stage, other requirement include good input matching and small power consumption.

LNA plays a key role in determining the SNR of the overall system. Although high gain is desirable for better sensitivity under weak signal conditions, it is not desirable under strong signal conditions because of intermodulation. In WCDMA applications, a high peak-to-average power ratio requires an LNA with high linearity. The intermodulated signal is also regarded as a noise and thus its level should be kept small so as not to degrade the SNR

All the aspects will be discussed in detail in this thesis make it a possible reference for others who want to be involved in LNA designs.

Chapter 2

LOW NOISE AMPLIFIER AND RECEIVER ARCHITECTURE

The integration of radio receivers has reached a state where the transceiver can mostly be implemented on a single chip. However, this integration level depends partly on the receiver architecture, which will be discussed in this chapter. The choice of receiver architecture affects the performance, size, and cost of the receiver. The superheterodyne receiver has hitherto been the dominant radio architecture, because of its good sensitivity and selectivity. However, superheterodyne receivers require expensive filters, which, with the existing technologies, cannot be integrated on the same chip as the receiver. Therefore, architectures using a minimum number of external components, such as direct conversion, have become popular.

The emphasis of this chapter is to point out the challenges in LNA design in modern telecommunication systems and to justify some of the choices made in the circuits design.

2.1 Superheterodyne receiver

A superheterodyne receiver removes the image by filtering before each downconversion stage. The block diagram of a superheterodyne receiver, with one intermediate frequency (IF) is shown in Figure 2.1. It is well known for its superior selectivity and sensitivity, and it is still widely used in different applications. In a superheterodyne receiver, the signal passes through the LNA, which is usually connected and matched to filters at both sides. The pre-select filter preceding the LNA passes the whole reception band for the desired system and attenuates signals outside this band. The following filter is required for image noise filtering because the LNA frequency response is not usually selective enough to suppress the noise at the image band. Hence, without this filter, the mixer would downconvert the noise from the image to the first IF. In addition, this filter may be used to filter out possible out-of-band tones that could corrupt reception. As an alternative, this filter can be replaced with an image-reject downconverter [13]. However, this requires additional hardware and good matching between different components in order to achieve high image suppression. After downconversion, a channel-select filter limits the spectrum

for the following stages to the desired signal by attenuating those signals which are out-of-channel. The first IF must be higher than half of the reception bandwidth.

Hence, the image is then always outside the reception band. The channel-select filter is followed by a variable-gain amplifier and demodulator, which divides the signal into I and Q branches. This basic concept may be altered to achieve block specifications that are sufficient for the targeted applications. A second IF stage may be used, which performs part of the channel filtering and interference cancellation. However, the use of a second IF may increase costs, and, because of the third LO, frequency planning becomes more difficult. Obviously, the channel filtering and gain may be distributed among different blocks in order to achieve an adequate performance. This distribution of gain and filtering is the reason why this architecture gives a good performance. The main reason why this architecture is currently unpopular is that it requires expensive external components. The pre-select, image, and channel-select filters cannot be integrated with current technologies. Thus, the size and cost of the receiver increase. Therefore, other architectures, which can be integrated on a single chip, have been widely explored.

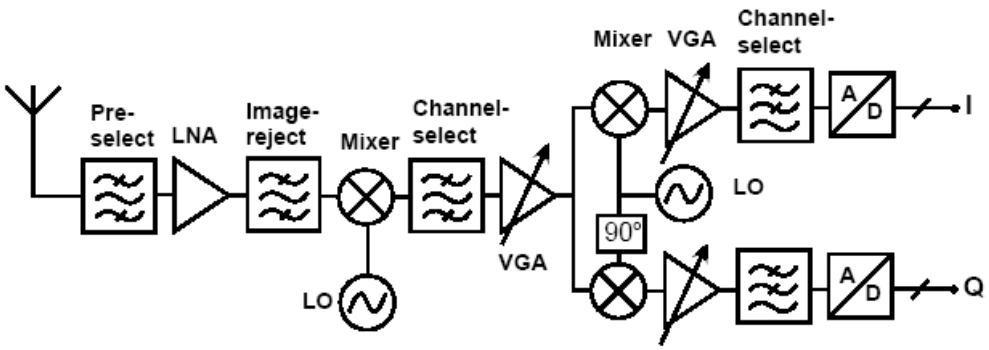

Figure 2.1: Block diagram of a superheterodyne receiver

2.2 Direct-conversion receiver

The direct-conversion architecture, shown in Figure 2.2, is well suited for single-chip integration. This architecture, which is also known as zero-IF or homodyne, converts the center of the desired RF signal directly to DC in the first mixers. The direct-conversion receiver suffers from special problems that do not appear in superheterodyne receivers. These problems limited the use of DCRs until the 1980s and 1990s, when they were first applied in paging and digital cellular receivers, respectively [2].

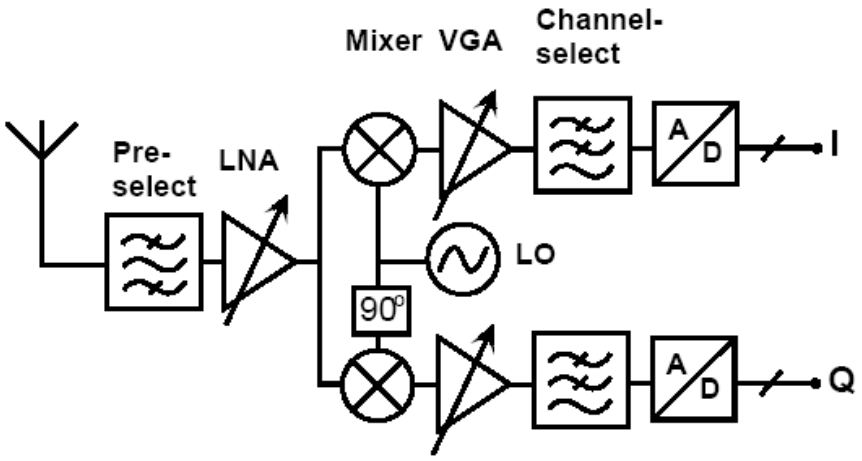

Figure 2.2 Block diagram of a direct conversion receiver.

A typical DCR includes a pre-select filter, an LNA, and quadrature mixers, followed by channel-select filters, variable-gain amplifiers, and A/D converters. The pre-select filter is required prior to the LNA in order to attenuate out-of-band signals, as in the superheterodyne receiver, because of poor front-end selectivity. The image filter after the LNA is not because the desired signal is directly converted to baseband. Obviously, this relaxes the design of the LNA-mixer interface because there is no need to drive external impedance, for example, 50Ω. In DCR, there is typically no need to drive any off-chip circuits, such as external filters. Thus, no matching to certain impedance, such as 50Ω, between different blocks is required. The quadrature I and Q channels are necessary while receiving typical phase and frequency modulated signals, because the two sidebands of the RF spectrum contain different information and result in irreversible corruption if they

overlap each other without being separated into two phases [9]. Channel filtering in DCRs is performed with low pass filters, which can be implemented with on-chip active circuits. The amplification and channel filtering can be distributed across the baseband chain to improve the performance of the receiver.

The major challenge in DCRs, compared to the superheterodyne receiver, arises from the LO signal, which is located at the same frequency as the desired signal. Thus, for example, the center of the desired signal is downconverted to DC. The leaked LO is on the passband of the pre-select filter and antenna. Hence, it can radiate out and may appear as an in-band interferer to other nearby receivers in the same frequency band. In addition, LO leakage causes DC offsets because of selfmixing. The LO signal can couple to different nodes at the receiver through capacitive and substrate coupling and, if the LO signal is provided externally, through bond wire coupling. The coupled LO signal is then mixed down to DC. In general, a selfmixed LO causes static DC offset.

All blocks create static DC offsets because of random and systematic device mismatches. The DC offset can corrupt the reception because a DC offset of only a few mV at the mixer output saturates the receiver if the typical voltage gain from 40dB to 70dB is implemented at the baseband. The DC offset can be removed in the baseband using different approaches. For example, it can be filtered out after the mixers using a highpass filter, such as an AC coupling. However, the highpass filter removes part of the signal and, therefore, the -3dB corner frequency corner frequency must be sufficiently low compared to the signal bandwidth. The low -3dB corner frequency of the highpass filter corresponds to a large time constant. Hence, the highpass filter may require a large chip area.

Direct downconversion also has limitations which affect the whole channel and not only DC. For example, if two interferers, $A_1 \cos(\omega_1 t)$ and $A_2 \cos(\omega_2 t)$, are fed into a device which has a second-order nonlinearity, $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$ then y (t) results a term $\alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t$. Hence, second-order nonlinearity creates low-frequency interference if $\omega 1 \approx \omega 2$.

2.3 Other architectures

Figure 2.3 illustrates the block diagram of a low-IF receiver. The low-IF receiver differs from the previous architectures in that the first IF is placed above DC but lower than half of the system reception bandwidth. The low-IF architecture tries to circumvent the problems related to previous architectures. In this receiver the problems related to DCR DC offsets are mitigated because there is no signal information at around DC. Thus, DC offsets can be filtered without signal information being removed. However, matching between the I and Q branches is critical if sufficient image rejection is to be achieved.

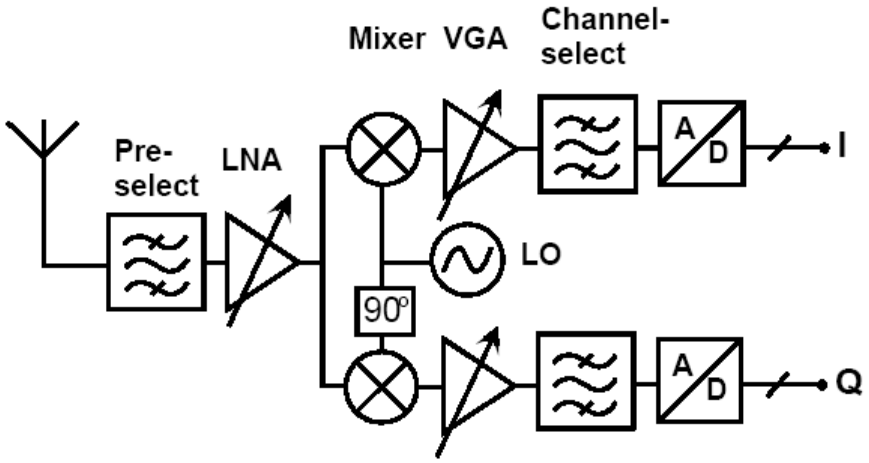

Figure 2.3: Block diagram of low-IF filter

A detailed description of, and comparison between, low-IF and other architectures, such as a wide-band IF receiver and direct digital receiver, can be found in [4]. In general, the other architectures set similar performance requirements for the LNA. The main differences between the different architectures, as regards to the LNA design, are the output load, reverse isolation, and the different spurious signals on-chip. The load can be an external filter or an on-chip device. For example, if the load is not an external filter, the interface between the LNA and mixer can be altered to optimize receiver performance. The reverse isolation of the LNA is important if the LO is on the reception band of the receiver.

2.4 Wireless telecommunication systems

Telecommunication systems were originally developed mostly for voice applications and they normally use analog signal processing. However, in modern systems, the signal processing is mostly performed in the digital domain. In the last few years, the main design driver has become data rather than voice. In Table 2.1, the key parameters of several existing standards are collected. The reception bands for these systems are usually located in the UHF band (between 0.3-3GHz). However, due to the limited spectrum in this band, systems such as WLAN 802.11a are operating in the SHF band (3-30GHz). In addition, it can be seen that the trend in system development has been to increase channel bandwidths in order to make communication at higher data rates possible. The sensitivity level determines the minimum signal, which has to be detected with a sufficient signal quality.

Table 2.1: Wireless telecommunication systems.

	Main Application	Access Method	Duplexing	Reception Bands[MHz]	Channel Spacing (kHz)	Sensitivity Level (dBm)
WCDMA	Data, Voice	DS-CDMA	FDD	1920-1980 2110-2170	5000	-117
GSM900	Voice	TDMA	TDD/FDD	880-915 925-960	200	-102
DCS1800	Voice	TDMA	TDD?FDD	1710-1785 1805-1880	200	-102
DCS1900	Voice	TDMA	TDD/FDD	1850-1910 1930-1990	200	-102
WLAN 802.11b	Data	DS-CDMA	TDD	2400-2483.5	22000	-76
GPS	Location	-	-	1575.42	-	-136
Bluetooth	Data	FH-CDMA	TDD	2400-2483.5	1000	-70

Chapter 3

LOW NOISE AMPLIFIER DESIGN

This chapter concentrates on the design issues of single-system low-noise amplifiers. The emphasis is on the single-stage inductively-degenerated common-source amplifier, which is the basis for the circuits designed in this thesis. A comparison between the most common LNA topologies and design issues is given. However, the feedback theory is only addressed briefly in this section. Ideal feedback does not add noise; however, resistive feedback does add additional noise sources. For this reason, resistive feedback is to be avoided in low noise amplifiers. It is also assumed, that the load for the LNA is on-chip. Thus, no matching is required at the LNA output.

3.1 Comparison of the LNA topologies

In the design of low noise amplifiers, there are several common goals. These include minimizing the noise figure of the amplifier, providing gain with sufficient linearity—typically measured in terms of the third-order intercept point, IP3—and providing a stable 50 input impedance to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier. A good input match is even more critical when a pre-select filter precedes the LNA because such filters are often sensitive to the quality of their terminating impedances. The additional constraint of low power consumption which is imposed in *portable* systems further complicates the design process. When it is low power, we are more difficult to get high gain and good noise performance.

With these goals in mind, we will first focus on the requirement of providing stable input impedance. This subsection compares four different single-ended LNA input stage configurations, illustrated in Figure 3.1. The three configurations, resistively terminated LNA, feedback LNA, and common-gate or $1/g_m$ termination LNA, which have all been used as LNA input stages, are included to clarify why the inductively-degenerated common-source LNA was chosen. Each of these architectures may be used in a single-ended form (as shown), or in a differential form. Note that differential forms will require the use of a balun or similar element to transform the single-ended signal from the antenna

into a differential signal. Practical baluns introduce extra loss which adds directly to the noise figure of the system.

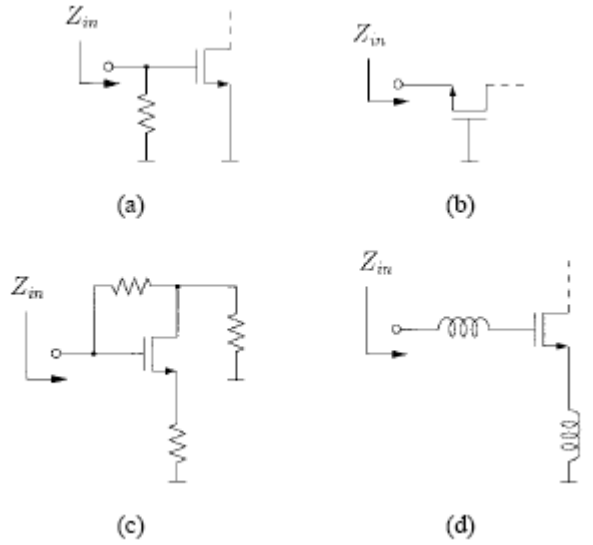

Figure 3.1: Common LNA architectures (a) Resistive termination (b) $1/g_m$ termination, (c) shunt-series feedback, and (d) inductive degeneration

3.1.1 Resistive terminated LNA

The first technique uses *resistive termination* of the input port to provide 50 ohms impedance. This approach in its differential form is shown by Chang *et al.* [12]. Unfortunately, the use of real resistors in this fashion has a deleterious effect on the amplifier's noise figure. The noise contribution of the terminating resistors is neglected in that work because an antenna would be mounted directly on the amplifier, obviating the need for input matching. Hence, the reported noise figure of 6 dB corresponds to a hypothetical "terminationless" amplifier.

In general, however, the LNA is driven by a source that is located some distance away, and one must account for the influence of the terminating resistor. Specifically, we require that the amplifier possess a reasonably stable input impedance of approximately 50 ohms. To evaluate the efficiency of simple resistive input termination, suppose that a given LNA employing resistive termination has power gain of G_a and output noise power of $P_{na,i}$ due

to internal noise sources only; and independent of the source impedance. Then, the noise factor is found to be

$$F = {Total\ \ output\ \ noise} \Big/ {Total\ \ output\ \ noise\ \ due\ \ to\ \ the\ \ source}$$

$$= 1 + \frac{P_{na,i} + kTBG_a}{kTBG_a} = 2 + \frac{P_{na,i}}{kTBG_a} \tag{3.1}$$

where B is the bandwidth over which the noise is measured. When the amplifier termination is removed, the noise figure expression becomes approximately

$$F = 1 + \frac{Pna,i}{4kTBG_a} \tag{3.2}$$

where we have assumed high input impedance relative to the source. From (3.1) and (3.2), we may surmise that a "terminationless" amplifier with a 6 dB noise figure would likely possess an 11.5 dB noise figure with the addition of the terminating resistor. The added resistor contributes its own noise to the output which equals the contribution of the source resistance. The large noise penalty resulting from these effects therefore makes this architecture unattractive for the more general situation where a good input termination is desired.

3.1.2 Common-gate LNA

A second architectural approach, shown in Figure 3.1(b), uses the source or emitter of a common-gate or common-base stage as the input termination. A simplified analysis of the $1/g_m$ -termination architecture, assuming matched conditions, yields the following lower bounds on noise factor for the case of CMOS amplifiers:

$$F = 1 + \frac{\gamma}{\alpha} \geq \frac{5}{3} = 2.2dB \tag{3.3}$$

Where

$$\alpha \equiv \frac{g_m}{g_{d0}} \tag{3.4}$$

In the CMOS expression, γ is the coefficient of the thermal noise, g_m is the device tranconductance, and g_{d0} is the zero-bias drain conductance. For long-channel devices, $\gamma = \frac{2}{3}$ and $\alpha = 1$. The value of 2.2dB in the CMOS expression neglects both short-channel effects ($\alpha \leq 1$) and excess thermal noise due to hot electrons ($\gamma \geq \frac{2}{3}$). Indeed, for short-channel MOS devices, γ can be much greater than 1 and α can be much less than 1. Accordingly, the minimum theoretically achievable noise figures to be around 3 dB or greater in practice.

3.1.3 Shunt-series feedback LNA

Figure 3.1(c) illustrates yet another topology, which uses resistive shunt and series feedback to set the input and output impedances of the LNA. This amplifier suffers from fewer problems than the previous circuit, yet the resistive feedback network continues to generate thermal noise of its own. As a consequence, the overall amplifier's noise figure, while usually better than the resistive termination amplifier, still exceeds the device F_{min} by a considerable amount (typically a few decibels).

All three of the preceding topologies suffer noise figure degradation from the presence of noisy resistance in the signal path. Fortunately, we can provide resistive input impedance without resistors. A better method is to employ inductive source degeneration. With such an inductance, current flow lags behind an applied gate voltage. An important advantage of this method is that we can control over the real part of the impedance through choice of inductance

3.1.4 Inductive source degenerative LNA

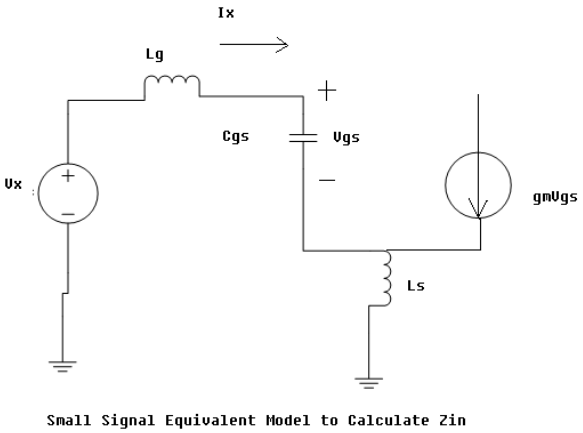

Figure 3.2: Small signal equivalent model to calculate input impedance

The fourth architecture, and the one that we have used in this design, employs inductive source or emitter degeneration as shown in Figure 3.1(d) to generate a real term in the input impedance. To further understand the inductive source degeneration method, consider a device model that includes only a tranconductance and a gate-source capacitance [15]. In that case, it is not hard to show that the input impedance has the following form

$$V_X = I_X\left(\frac{1}{jwC_{gs}} + jwL_g\right) + \left(I_X + g_m V_{gs}\right)\left(jwL_S\right) \tag{3.5}$$

$$V_{gs} = \frac{I_X}{jwC_{gs}} \ , \tag{3.6}$$

rearranging the equation will give us

$$V_X = I_X\left(\frac{1}{jwC_{gs}} + jwL_g + jwL_S\right) + I_X\left(\frac{g_m}{C_{gs}}\right)L_S \tag{3.7}$$

$$Z_{in} = s\left(L_S + L_g\right) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right)L_S \tag{3.8}$$

It can be shown that the real part of the input impedance is

$$R_{in} = \left(\frac{g_{m1}}{C_{gs}} \right) L_S \approx w_T L_S \tag{3.9}$$

Whatever the value of the resistive term, it is important to emphasize that it does not bring with it the thermal noise of an ordinary resistor because a pure reactance is noiseless. The inductance L_s is chosen to provide the desired input resistance (equal to R_s, the source resistance). Since the input impedance is purely resistive only at resonance, an additional degree of freedom, provided by inductance L_g, is needed to guarantee this condition.

Chapter 4

LNA CHARACTERISTICS

Parameters used to determine the performance of the LNA circuit

4.1 Voltage gain

The first stage of a receiver is typically a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages (such as a mixer). However, High voltage gain will degrade the noise figure and the linearity. So, it is important to get a balance between these parameters.

At resonance, the gate-to source voltage is Q-times as large as the input voltage. With the output current proportional to the voltage on C_{gs} , the overall stage tranconductance G_m under this condition is therefore [15]

$$G_m = g_{m1}Q_{in} = \frac{g_{m1}}{\omega_0 C_{gs}(R_S + \omega_T L_S)} = \frac{\omega_T}{\omega_0 R_S\left(1+\frac{\omega_T L_S}{R_S}\right)} = \frac{\omega_T}{2\omega_0 R_S} \tag{4.1}$$

where we have use the approximation that ω_T is the ratio of g_{m1} to C_{gs}. Q_{in} is the effective Q of the amplifier input circuit. In this expression, which is valid at the series resonance ω_0, R_l and R_g have been neglected relative to the source resistance, R_S . The tranconductance of this circuit at resonance is independent of g_{m1} (the device tranconductance) as long as the resonant frequency is maintained constant. If the width of the device is adjusted, the transconductance of the *stage* will remain the same as long as L_g is adjusted to maintain a fixed resonant frequency. This result is intuitively satisfying, for as the gate width (and thus g_{m1}) is reduced, C_{gs} is also reduced, resulting in an increased Q_{in} such that the product of g_{m1} and Q_{in} remains fixed.

Basically, the voltage gain is equal to

$$G = \frac{Vout}{Vin}$$

$$= g_{m1} Q_{in} Z_L \qquad (4.2)$$

Where Z_L is the load impedance.

4.2 Noise Figure

The standard CMOS noise model is shown in Figure 4.1. The dominant noise source in CMOS devices is channel thermal noise. This source of noise is commonly modeled as a shunt current source in the output circuit of the device.

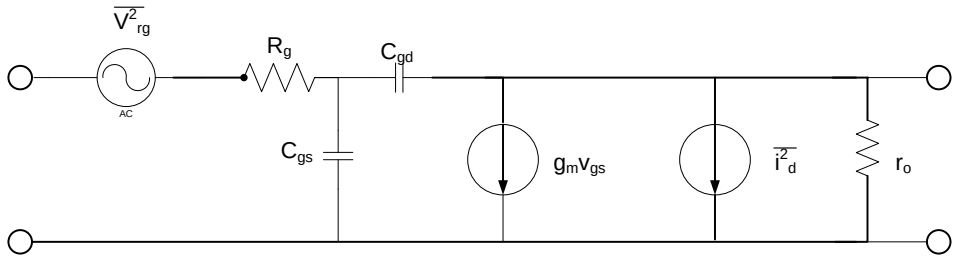

Figure 4.1: The standard CMOS noise model.

The channel noise is white with a power spectral density given by

$$\frac{\overline{i_d^{\,2}}}{\Delta f} = 4kT\gamma g_{d0} \qquad (4.3)$$

Where g_{d0} is the zero-zero-bias drain conductance of the device, and γ is a bias-dependent factor that, for long-channel devices, $\gamma = \frac{2}{3}$ when the device is saturated.

For short-channel devices, however, γ does not satisfy (4.2). In fact, γ *is much greater than 2/3 for short-channel devices operating in saturation* [3]. This excess noise may be attributed to the presence of hot electrons in the channel. The high electric fields in submicron MOS devices cause the electron temperature, T_e , to exceed the lattice temperature. The excess noise due to carrier heating was anticipated by van der Ziel as early as 1970 [6].

An additional source of noise in MOS devices is the noise generated by the distributed gate resistance [14]. This noise source can be modeled by a series resistance in the gate

circuit and an accompanying white noise generator. By interdigitating the device, the contribution of this source of noise can be reduced to insignificant levels. For noise calculation purposes, the distributed gate resistance is given by [8].

$$R_g = \frac{R_\Delta W}{3n^2 L} \tag{4.4}$$

Where R_Δ is the sheet resistance of the polysilicon, W is the total gate width of the device, L is the gate length, and n is the number of gate fingers used to lay out the device. The factor of 1/3 arises from a distributed analysis of the gate, assuming that each gate finger is contacted only at one end. By contacting at *both* ends, this term reduces to 1/12. In addition, this expression neglects the interconnect resistance used to connect the multiple gate fingers together. The interconnect can be routed in a metal layer that possesses significantly lower sheet resistance, and hence is easily rendered insignificant.

Though playing a role similar to that of base resistance in bipolar devices, the gate resistance is much less significant in CMOS because it can be minimized through interdigitation without the need for increased power consumption, unlike its bipolar counterpart. Its significance is further reduced in silicided CMOS processes which possess a greatly reduced sheet resistance, R_Δ.

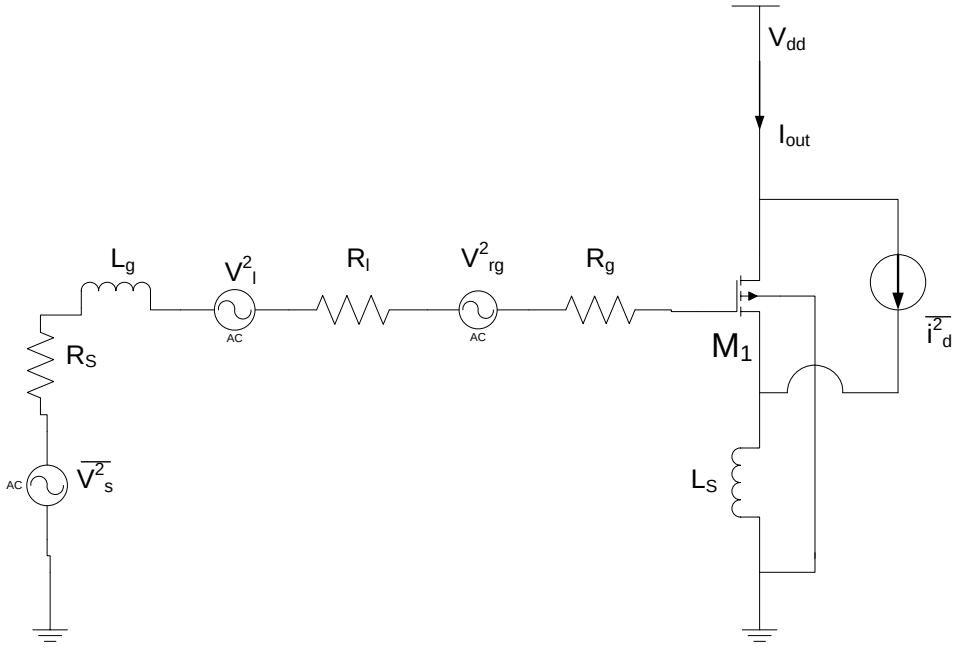

Figure 4.2: Equivalent circuit for input noise calculations

The noise figure of the LNA can be computed by analyzing the circuit shown in Figure 4.2. In this circuit, R_l represents the series resistance of the inductor L_g, R_g is the gate resistance of the NMOS device, and $\overline{i_d^{\,2}}$ represents the channel thermal noise of the device. Analysis based on this circuit neglects the contribution of subsequent stages to the amplifier noise figure. This simplification is justifiable provided that the first stage possesses sufficient gain and permits us to examine in detail the salient features of this architecture. Note that the overlap capacitance C_{gd} has also been neglected in the interest of simplicity. The use of a cascaded first stage helps to ensure that this approximation will not introduce serious errors.

The noise factor for an amplifier is defined as

$$F = \frac{Total\ output\ noise}{Total\ output\ noise\ due\ to\ the\ source} \tag{4.5}$$

Using (4.1), the output noise power density due to the 50-Ω source is

$$S_{\alpha,src}(\omega_0) = S_{src}(\omega_0)G_{m,eff}{}^2 = \frac{4kT\omega_T{}^2}{\omega_0{}^2 R_S\left(1+\frac{\omega_T L_S}{R_S}\right)} \tag{4.6}$$

The output noise power density due to R_l and R_g can be expressed as

$$S_{\alpha,Rl,Rg}(\omega_0) = \frac{4kT\left(R_l+R_g\right)\omega_T{}^2}{\omega_0{}^2 R_S{}^2\left(1+\frac{\omega_T L_S}{R_S}\right)} \tag{4.7}$$

Equation (4.6) and (4.7) are also valid only at the series resonance of the circuit.

The dominant noise contributor internal to the LNA is the channel current noise of the first MOS device. Recalling the expression for the power spectral density of this source from (4.2), one can derive that the output noise power density arising from this source is

$$S_{\alpha,id}(\omega_0) = \frac{\frac{\overline{i_d^{\,2}}}{\Delta f}}{\left(1+\frac{\omega_T L_S}{R_S}\right)^2} \tag{4.8}$$

The total output noise density is the sum of (4.6)-(4.8). Assuming a 1 Hz bandwidth and substituting these into (4.4) yields

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \gamma g_{d0} R_S \left(\frac{\omega_0}{\omega_T} \right)^2$$
$$= 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha} g_m R_S \left(\frac{\omega_0}{\omega_T} \right)^2 \quad (4.9)$$

Where $\omega_T = \frac{g_m}{C_{gs}}$, and $\alpha = \frac{g_m}{g_{d0}}$

The equation (4.9) shows the inverse dependence on $\omega_T{}^2$. Continue improvements in technology which improve ω_T will therefore naturally lead to improved noise performance at a given frequency of operation.

To predict a fundamental limit of noise performance of this architecture, we should include the induced gate current noise in MOS devices.

The gate noise is partially correlated with drain noise, with a correlation coefficient given by [7]

$$c = \frac{\overline{i_g i_d{}^*}}{\sqrt{\overline{i_g{}^2}\,\overline{i_d{}^2}}} \approx 0.395\,j \quad (4.10)$$

The value of 0.395j is exact for long-channel device.

The gate noise can be expressed as

$$\frac{\overline{i_g{}^2}}{\Delta f} = 4kT\delta g_g \left(1 - |c|^2\right) + 4kT\delta g_g |c|^2 \quad (4.11)$$

Where the first term is the uncorrelated gate noise and second part is the correlated gate noise.

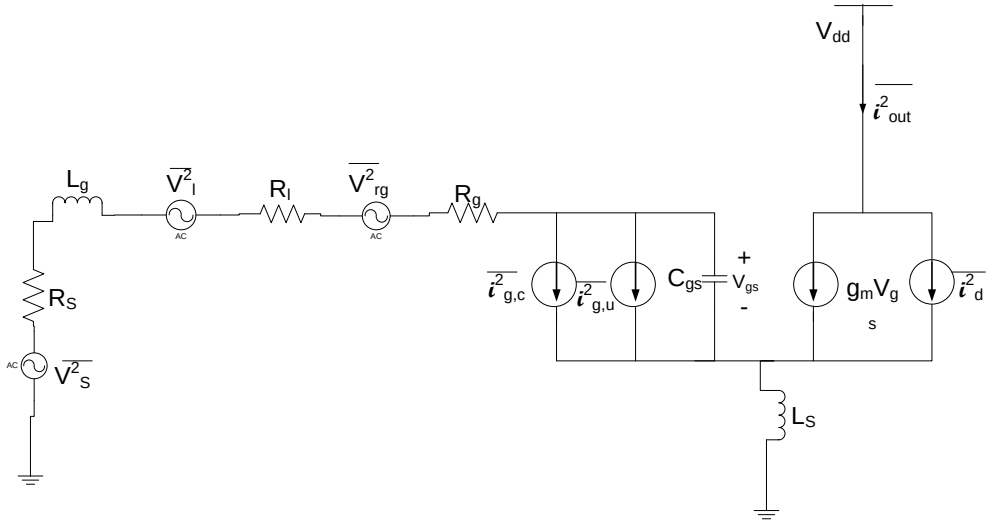

Figure 4.3 Small-signal model for LNA noise calculations

We employ the circuit of Figure 4.3 to evaluate the noise performance of the LNA in the presence of the gate-noise. The combined effect of the drain noise and the correlated portion of the gate noise is

$$S_{\alpha,id,ig,c}(\omega_0) = \kappa S_{\alpha,id}(\omega_0) = \frac{4kT\gamma\kappa g_{d0}}{\left(1+\frac{\omega_T L_S}{R_S}\right)^2} \tag{4.12}$$

Where

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1+|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 \tag{4.13}$$

$$Q_L = \frac{\omega_0(L_S+L_g)}{R_S} = \frac{1}{\omega_0 R_S C_{gs}} \tag{4.14}$$

The uncorrelated portion of the gate noise:

$$S_{\alpha,ig,u}(\omega_0) = \xi S_{\alpha,id}(\omega_0) = \frac{4kT\gamma\xi g_{d0}}{\left(1+\frac{\omega_T L_S}{R_S}\right)^2} \tag{4.15}$$

Where

$$\xi = \frac{\delta\alpha^2}{5\gamma}\left(1-|c|^2\right)\left(1+Q_L{}^2\right) \tag{4.16}$$

Since all of the noise term by the first device M_1 are proportional to $S_{\alpha,id}(\omega_0)$, drain noise, hence it is convenient to define the contribution of M_1 as a whole as

$$S_{\alpha,M1}(\omega_0) = \chi S_{\alpha,id}(\omega_0) = \frac{4kT\gamma\chi g_{d0}}{\left(1+\frac{\omega_T L_S}{R_S}\right)^2} \tag{4.17}$$

Where,

$$\chi = \kappa + \xi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1+Q_L{}^2\right) \tag{4.18}$$

From (4.17), it can be seen that the effect of induced gate noise is to modify the noise contribution of the device in proportion to χ. It follows that

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \gamma\chi g_{d0} R_S\left(\frac{\omega_0}{\omega_T}\right)^2 \tag{4.19}$$

By factoring out Q_L from the expression for χ, and note that

$$g_{d0}Q_L = \frac{g_m}{\alpha}\frac{1}{\omega_0 R_S C_{gs}} = \frac{\omega_T}{\alpha\omega_0 R_S} \tag{4.20}$$

We can re-express F as

$$F = 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \tag{4.21}$$

The equation of χ includes terms which are constant, proportional to Q_L, and proportional to $Q_L{}^2$. Equation (4.21) will therefore contain terms which are proportional to Q_L and also inversely proportional to Q_L. Therefore, a minimum *F* exists for a particular Q_L.

4.3 Linearity

4.3.1 Third Order intercept Point (IIP3)

There are many measures of linearity, the most commonly used are third-order intercept (IP3) and 1-dB compression point (P_{1dB}).

For fully differential circuits, the even-order distortion components are ideally zero and, thus, third-order distortion typically dominates. However, incases where second-order distortion dominates, a similar concept is also possible and is referred to as the second-order intercept point (IIP2).

To relate these measures to readily calculated circuit and device parameters, the amplifier's output signal may be represented by a power series [15]:

$$v_O(t) \approx a_0 + a_1 v + a_2 v^2 + a_3 v^3 \tag{4.22}$$

Where the equation above describes the specific case of a tranconductance.

Consider two sinusoidal input signals of equal amplitude but slightly different frequencies:

$$v = A[\cos(\omega_1 t) + \cos(\omega_2 t)] \tag{4.23}$$

In this case, the output signal can be shown to be approximated by

$$\begin{aligned} v_O(t) \equiv & \left(a_1 A + \frac{9a_3}{4} A^3 \right) [\cos(\omega_1 t) + \cos(\omega_2 t)] \\ & + \frac{a_3}{4} A^3 [\cos(3\omega_1 t) + \cos(3\omega_2 t)] \\ & + \frac{3a_3}{4} A^3 [\cos(2\omega_1 t + \omega_2 t) + \cos(2\omega_2 t + \omega_1 t)] \\ & + \frac{3a_3}{4} A^3 [\cos(\omega_1 t - \Delta\omega t) + \cos(\omega_2 t + \Delta\omega t)] \end{aligned} \tag{4.24}$$

Where we see a fundamental term and third-harmonic term. $\Delta\omega$ is defined to be the difference between the input frequencies (i.e. $\Delta\omega \equiv \omega_2 - \omega$) which we assume to be small. Here, we see that the first line of the (4.24) is the fundamental components, the second line show the levels at three times the fundamental, the third line also describe distortion at nearly three times the fundamentals, and the fourth line describes the distortion levels at two new frequencies that are close to the input frequencies (slightly below ω_1 and slightly above ω_2). The difference frequency of third-order IM components can be quite troublesome since their frequencies may lie in band if ω_1 and ω_2 differ by only a small amount. It will give nonlinearity to magnitude of the output because it lies in band with the fundamental frequency. As a result, for a narrowband or low-pass filter, these two new distortion fall in the passband and can be used to predict the third-order distortion term.

Approximate the linear component of output term as

$$I_{D1} = a_1 A \tag{4.25}$$

and the third0harmonic term as

$$I_{D3} = \frac{3a_3}{4} A^3$$

The ratio of these two is the third-order intermodulation value, given by

$$ID_3 = \frac{I_{D3}}{I_{D1}} = \left(\frac{a_3}{a_1}\right)\left(\frac{3A^2}{4}\right) \tag{4.26}$$

For every dB increase in input power, the third order products will increase by 3 dB. Plotting third products versus input power predicts a 3:1 response which intersects the 1:1 response at the third order intercept point. Third order intercept point will be approximately 10 to 20 dB higher than the 1 dB gain compression point, P_{1dB}.

Thus, third order intercept point (IIP3) is an important measure of linearity.

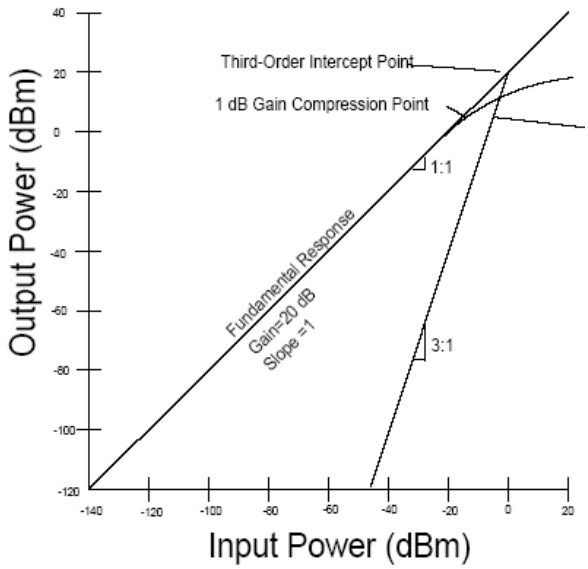

Figure 4.4: Third order intercept point [15]

4.3.2 1-dB Compression Point (P_{1dB})

Another important measure is the P_{1dB}. In RF circuits, the gain compression is defined as the "-1dB compression point", which is the point where the gain is decreased by 1dB from

the gain at small signal levels. In receivers, the compression point is usually defined at the input (ICP) and in transmitters at the output (OCP)

Chapter 5

THE DESIGN OF DIFFERENTIAL INDUCTIVE SOURCE DEGENERATED LNA

5.1 Power-Constrained Noise Optimization.

The circuits that will be used are similar to the circuit below [15]:

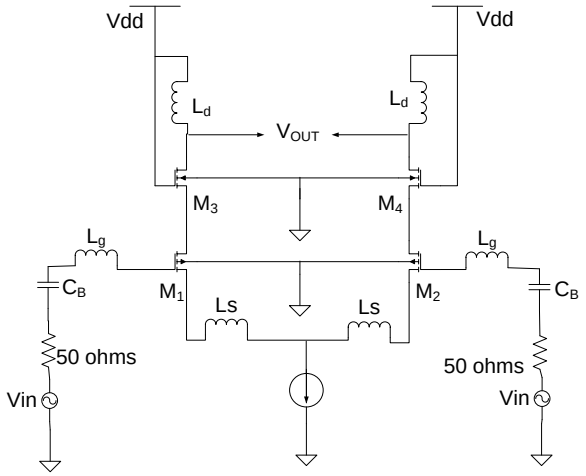

Figure 5.1: LNA differential topology

The topology that is being used is inductive source degeneration differential LNA, where two cascode amplifiers are connected in differential. The cascode transistor has several benefits which make it especially suitable for DCRs. The cascode transistor reduces the Miller effect in the input transistor, since the input impedance of the cascode transistor is usually smaller than the load impedance. In addition, the cascode transistor increases the separation between the input and output terminals of the LNA compared to a single-transistor LNA. Hence, the input matching, size of input transistor and load can be separately optimized. The increased separation can have a significant effect on the performance of the DCR. The improved reverse isolation reduces the LO leakage to the LNA input. The specifications determine the maximum spurious emissions for the terminal. Because the LO signal is located in the receiver reception band, the pre-select filter does