INVESTIGATE INSTABILITY BEHAVIOUR IN HIGH POWER LDMOS POWER AMPLIFIER

Oleh

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ABSTRACT

In this thesis the models of LDMOS power amplifier was been investigated using Advanced Design System (ADS) version 2004A software from Agilent Technologies for operation below 1 GHz frequency range. There are two models considered in this project. Both of the models were provided by Motorola. The two models are RD01MUS1 and RD07MVS1 based on a 59 mil LDMOS transistor using type of FR4 PCB Board. Large-signal simulations of both models have demonstrated results, which lead to the conclusion that, these models cannot be efficiently utilised for design of input and output matching networks using Unilateral value for Conjugate Matching. However, there are other matching applications; Load Line Matching and Load Pull Analysis that can be used that have not been explored yet by the researcher due to time constraint. Hence, it is important to take into account during new processes of LDMOS as well as to improve the CAD model. The final conclusion regarding LDMOS cannot be made just based on these simulation results, since they are not in accordance with the published ones. The next step should be aimed at improving the model and further investigation of LDMOS to prove their ability to operate with optimum efficiency in above1 GHz frequency range.

ABSTRAK

Dalam tesis ini, model penguat kuasa menggunakan transistor LDMOS dikaji menggunakan perisian ‘Advanced Design System’ versi terbaru 2004A keluaran ‘Agilent Technologies’. Kajian adalah meliputi kemampuan model tersebut beroperasi kurang daripada 1 GHz. Terdapat dua model penguat kuasa yang dikaji sepanjang projek ini dijalankan. Model-model tersebut terdiri daripada RD01MUS1 dan RD07MVS1 keluaran Mitsubishi yang diekstrak daripada transistor LDMOS transistor yang berukuran 59 mil pada PCB board jenis FR4. Hasil simulasi bagi kedua-dua model tersebut menunjukkan bahawa rekabentuk rangkaian kesepadanan untuk masukan dan keluaran adalah tidak efisien jika menggunakan nilai ‘Unilateral’ yang diaplikasi dengan cara Pemadanan Konjugat. Walaubagaimanapun, terdapat dua lagi aplikasi kesepadanan yang boleh digunakan tetapi tidak sempat dicuba oleh pengkaji kerana masalah kesuntukan masa iaitu aplikasi Pemadanan Talian Beban (Load Line Matching) dan Analisis Talian Beban (Load Pull Analysis) Dengan itu, adalah penting untuk menghasilkan transistor yang mampu untuk beroperasi dengan kecekapan yang tinggi semasa proses pembuatan lagi untuk menjimatkan masa dan kos untuk menyelesaikan masalah ketidakstabilan di bawah keadaan tidaksepadanan transistor LDMOS. Kesimpulan mengenai kemampuan transistor LDMOS tidak boleh dibuat hanya berdasarkan keputusan simulasi kerana keputusan simulasi tidak semestinya bertepatan dengan keputusan pengukuran yang menggunakan alatan sebenar. Langkah seterusnya sepatutnya difokuskan untuk memeperbaiki model dan kajian lanjutan perlu diteruskan terhadap kebolehan LDMOS untuk beroperasi dengan kecekapan optimum pada julat frekuensi lebih dripada 1 GHz.

ACKNOWLEDGEMENT

This project would not have been possible if not because of advices, contributions and moral supports from several individuals.

I would like to express my greatest gratitude and appreciation to my thesis supervisor, Proff Syed Idris Syed Hassan for being very supportive, and also for contributing invaluable helps, guidance, encouragement and patience throughout the process of this project.

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To my beloved parents, Haji Ab Rahman b. Yusof and Hjh Saleha bt Yaacob, and all my siblings, K Ayu, K Yeen, Abg Boy, K Intan and EE for all supports and encouragement throughout the course of this project. My special gratitude also goes to my dearest brother Irwan Hakimi b. Ab Rahman and my cousin, Amierul Azwan b. Ab Aziz for their technical support.

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LIST OF ABBREVIATION

LDMOS	Laterally Diffused Metal Oxide Semiconductor
PA	Power Amplifier
PAE	Power-Added Efficiency
ADS	Advanced Design System
BJT	Bipolar Junction Transistor
FET	Field Effect Transistor
JFET	Junction Field Effect Transistor
MOSFET	Metal Oxide Semiconductor FET
MISFET	Metal Insulator Semiconductor FET
D-MOSEFET	Depletion Metal Oxide Semiconductor FET
E-MOSFET	Enhancement Metal Oxide Semiconductor FET
IMN	Input Matching Network
OMN	Output Matching Network
MGA	Maximum Gain Amplifier
U-MOS	U-shaped channel MOSFET
V-MOS	V-shaped channel MOSFET

CHAPTER 1

INTRODUCTION

1.0 Introduction

Power Amplifiers are used to boost a small-signal to a large signal. LDMOS Power Amplifier (PA) devices are commonly and widely used in today's transmitter. LDMOS devices have higher gain and lower cost than bipolar parts. They are used for many applications including commercial FM broadcasting and TV power transmitters, cellular and paging communications systems, and military RF and microwave hand-held transceivers [Andrey V. Grebennikov, 2000].

From the block diagram shown in Figure 1.0, the location of Power Amplifier in general communication system can be seen. Solid-state microwave amplifiers play an important role in communication where it has different applications, including low noise, high gain, and high power amplifiers. The high gain and low noise amplifiers are small signal low power amplifiers and are mostly used in the receiver side where the signal level is low. The small signal S-parameter can be used in designing these low power amplifiers. The high power amplifier is used in the transmitter side where the signal should be at a high level to cross the desired distance [Saad Al-Shahrani, 2001]. The intent of this chapter is to give an overview of some basic principles used in the analysis and design of the microwave transistor amplifier.

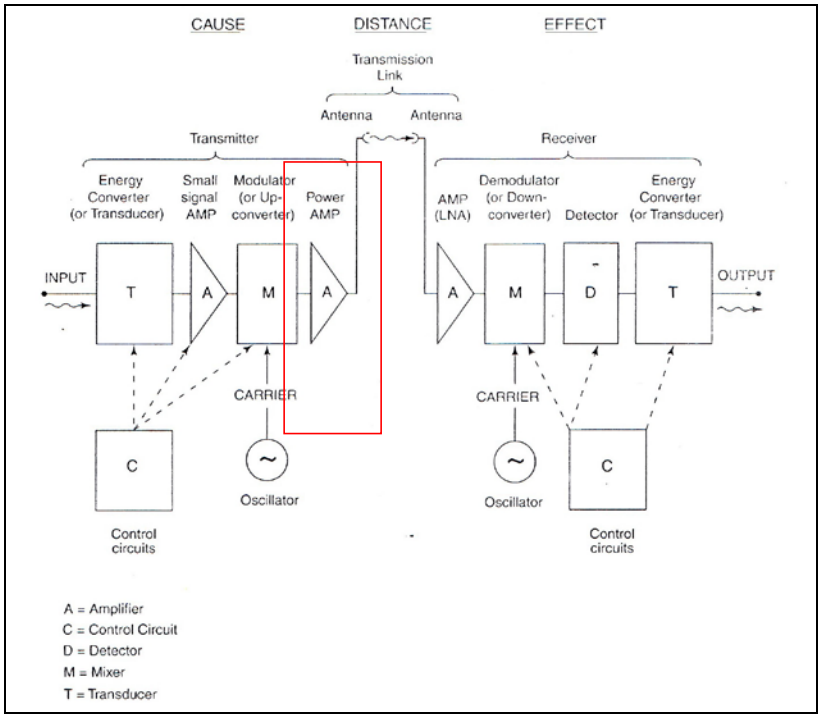

Fig 1.0- Block diagram of a general communication system

Based on Figure 1.0, an overview of the operation of general communication system and the importance of a power amplifier can be shown. The following is the explanation on the operation of transmitter where the power amplifier is located.

From left, the incoming energy (sound) will be converted to electrical energy in energy conversion stage by a signal conversion device, for example a microphone. Then, the electrical energy will flow into amplification stage. Here, high-gain small signal amplifier causes a higher signal to compensate for losses in the energy conversion stage.

After the amplification stage is the frequency conversion stage where carrier wave produced by local oscillator will be modulated with the signal that has been amplified at amplification stage.

After that, the modulated signal will flow into power amplification stage. This is the stage where the signal power level is boosted greatly so that a higher range of reception is allowed. The purpose of the power amplification stage is to compensate the signal being weaken after going through the different stages. Then, the modulated signal will be transported from 'cause or source point' to the 'effect or receipt point' in transmission link to receiver part.

Stages that include in receiver part are low-noise amplification stage, frequency conversion stage (or demodulation or down-conversion), detector stage, energy conversion stage and finally control stage.

The final stage is the stage where all the decisions with regard to circuit connection/disconnection, routing, switching and so on, take place. A control stage is present at both the source and the receipt points of the communication system [Matthew M.Radmanesh, 2001].

1.1 Background of Problem

The common problem with transmitter design is instability under mismatch conditions. Many stability techniques have been developed for bipolar devices. However, there is not much information on the possible instability modes for LDMOS as bipolar devices. Due to lack of information, the current stability fixes for the LDMOS is similar to bipolar parts which may not be optimum. The research project shall focus on the various instability modes and develop the appropriate solution.

1.2 Objectives

In general, this research is conducted to seek and survey the phenomena of instability of LDMOS Power Amplifier (PA) and develop solutions to its problem of instability under mismatch conditions. Therefore, the biasing and matching principle has been applied. The full energy has been utilized at optimum load impedance in order to achieve good efficiency.

There are several purposes to do this research. The main point is to verify power amplifier models that were provided by Motorola to increase efficiency of power amplifier using LDMOS devices.

Another purpose of this research project is to study and really understand I-V characteristic of power amplifier. There is also an opportunity to learn practically how to choose the quiescent point from I-V characteristic.

From this research, the researcher has to survey an amplifier classifications and definitions in order to design power amplifier in this project. This project gives an overview of basic matching principles used in the analysis and step to design the microwave transistor amplifier.

Another point to do this research is, to verify S-parameter values of simulation models where the frequency was fixed at 520 MHz in order to compare with measurement data.

In this project, the researcher must learn steps to design Class A power amplifier using LDMOS transistor using simulation model. The application of Unilateral or Bilateral Design has to be understood first in order to get parameter values that needed to apply Conjugate Matching.

Another objective to do this research project is to study the performance of power amplifier from the view of efficiency, power-added efficiency, gain and operation at 1dB point.

1.3 Scope

In this project, the simple PA simulation design process is performed mostly using Advanced Design System version 2004A and also Z-Match. The models that were considered during this project are two contemporary LDMOS transistor non-linear models (RD01MUS1 and RD07MVS1_encoded). Both models were provided by Motorola.

Research that has been done is investigation to have optimum efficiency of LDMOS Power Amplifier by using application of DC Analysis and S-Parameter Simulations. In order to tackle matching problems, Conjugate matching principle was applied. In order to get better result of input and output matching, other approaches that have been used in this project are optimization and tuning. Harmonic Balance Analysis is based on seeking performance of power amplifier operation at 1dB gain compression point (power output), gain and power –added efficiency (PAE).

1.4 Overview of Final Year Report

This report provides with steps to design Class A power amplifier and tackle problem of matching in order of instability behaviour in high power LDMOS Power Amplifier. In order to design the LDMOS PA, application of biasing, optimizing and tuning was applied. The performances of power amplifier including efficiency, gain and operation at P1dB point are also taken into account. The format of this report will therefore follow the goals.

Chapter 2 discusses the main types of transistors and their definitions, common topologies used in LDMOS Power Amplifier design, as well as briefly explain classes of power amplifier to give an overview about class of amplifier that will be designed at the next chapter. Chapter 2 also mentions some of the important properties of an LDMOS transistor.

Chapter 3 contains the Design Methodologies that have been used in the project. Introductory description is available for transistor models; RD01MUS1 and RD07MVS1_encoded that were considered in this project. The main part of the chapter is about the design flow and matching application that will be used for simulation.

Chapter 4 discusses the simulation results that were obtained after each step of matching, optimizing and tuning was applied to see the improvement in minimizing power reflection of input and output matching network.

Finally, conclusions from this project are presented in Chapter 5. List of references are available after Chapter 5. Result of phenomenon was discussed based on the investigation conducted. Some recommendations for future researches and the limitations occurred in this project are also available in this chapter.

Appendixes contain simulation models and results from ADS.

CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

In this chapter, the discussion will cover five main topics that need to be clarified as the idea and principles for this project. The topics include the main types of transistors and their definitions, common topologies used in LDMOS Power Amplifier design, as well as briefly explain classes of power amplifier to give an overview about class of amplifier that will be designed in the next chapter. Chapter 2 also mentions some of the important properties of an LDMOS transistor and software specifications that have been used in this project.

2.1 Transistor

All transistors are semiconductor devices, but there are numerous different configurations. Transistors can be categorized broadly into two types: the bipolar transistor and the field-effect transistor (FET).

2.1-1 The Basic Types of Transistors

Bipolar Junction Transistors (**BJT**) use both electrons and holes as charge carries whereas Field-Effect Transistors (**FET**) operate only with one type of charge carriers which gives the FET an alternate name: the Unipolar Transistor. [(Thomas L. Floyd, 1995]).

The BJTs are also called current-controlled devices, since the base current controls the collector current. On the other hand, in FETs the gate voltage controls the drain current through the device. Consequently, the FETs are voltage-controlled devices.

Another major difference between an FET and a BJT is the fact that an FET's gate input impedance is very large and that the current through the gate, for all practical purposes, can be considered to be zero [Matthew M.Radmanesh, 2001].

Figure 2-1 shows the different types of transistors such as **J**unction-**FET** (***J*FET**), **M**etal-**O**xide(**I**nsulator)-**S**emiconductor-**FET** (***MOS*FET or *MIS*FET**) and **M**etal-**S**emiconductor-**FET** or Schottky transistor (***MES*FET**).

The **M**etal-**O**xide **S**emiconductor **FET** ***(MOSFET)*** and the **J**unction **FET** ***(JFET)*** are used for lower frequencies and digital circuits. The **M**etal-**S**emiconductor **FET** ***(MESFET),*** using Gallium Arsenide or Indium phosphide material, is used at high RF, microwave and millimeter-wave frequencies

There are two main types of the MOSFET: a *depletion transistor* - (***D*-MOSFET**) and an *enhancement transistor* - (***E*-MOSFET**). The mostly used is E-MOSFET. There are many technologies such as low power CMOS, NMOS and power devices - LDMOS, VMOS, UMOS, which are based on the enhancement mode [Grigouri Doudorov, 2003]. As LDMOS transistor is being used in this project, the graphical structure below shows the group type where it belongs to (Fig 2.1).

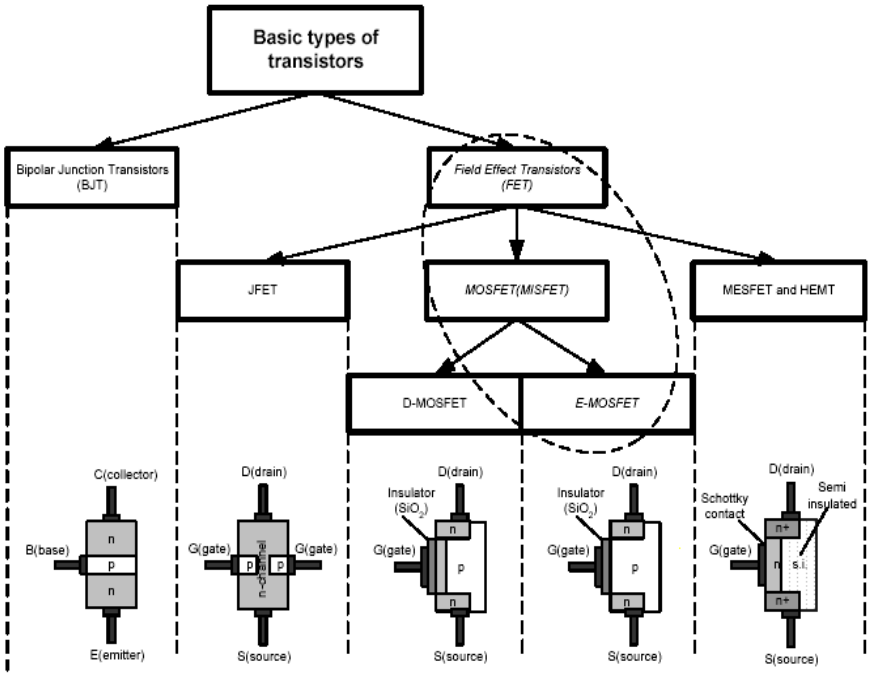

Figure 2.1- Basic Types of Transistors (the given structures illustrate NPN and n-channel devices)

2.2 Laterally Diffused Metal Oxide Semiconductor (LDMOS) transistor

Laterally Diffused Metal Oxide Semiconductor (LDMOS) devices have traditionally been used in high voltage switching operations and rectifier applications due to the high breakdown voltages. It also enables good high frequency performance possible to be achieved.

In the main, LDMOS transistors are lateral, surface effect silicon devices composed of a p– epi-layer over a p+ substrate. Typically such devices have three terminals (source,

gate and drain) where the voltage on the gate controls the current flowing from the drain to the source. [M. Jennings, 2003]. A typical structure is presented in Figure 2.2.

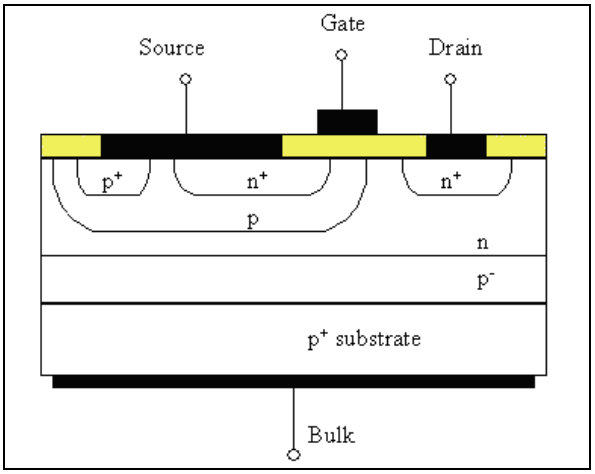

Fig 2.2 - Cross Section of LDMOS structure

2.2-1 Circuit Model

A simple circuit model is required to evaluate the transfer characteristic of the LDMOS under steady state conditions. Figure 2.3 shows a diagrammatic representation of a simple circuit employed to drive the LDMOS device. [A. Litwin et. al, 2000]. The small-signal equivalent circuit of a high-power LDMOS FET cell with channel length L = 1.25 µm and channel width W = 1.44 mm is shown in Figure 2.3. The device model parameters were extracted from I-V Characteristics and S-parameter measurements. The parameters of the equivalent circuit are given at a bias voltage for class AB operation with quiescent current Iq = 15 mA at Eds = 28 V. [V. Grebennikov, Andrey, 2000]. However, in this project, power amplifier was designed in Class A, for the purpose of exploring something new.

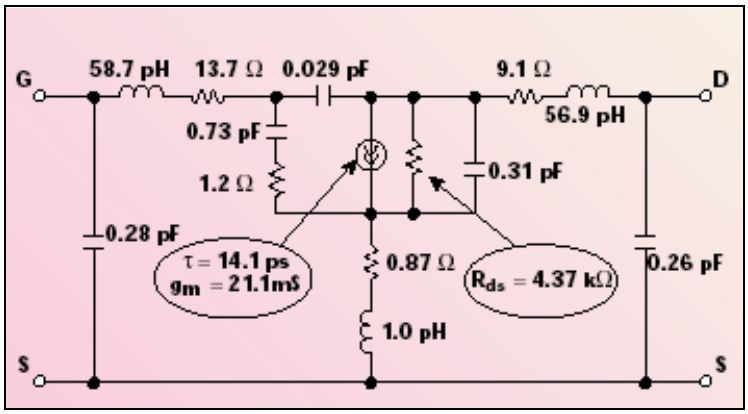

Fig 2.3- The LDMOS FET's small-signal equivalent circuit

The equivalent circuit of the simulated 500 MHz one-stage lumped power amplifier is shown in Figure 2.4. For the example, the total channel width used of the high-voltage LDMOS FET is ~~7~~ 71.44 mm.

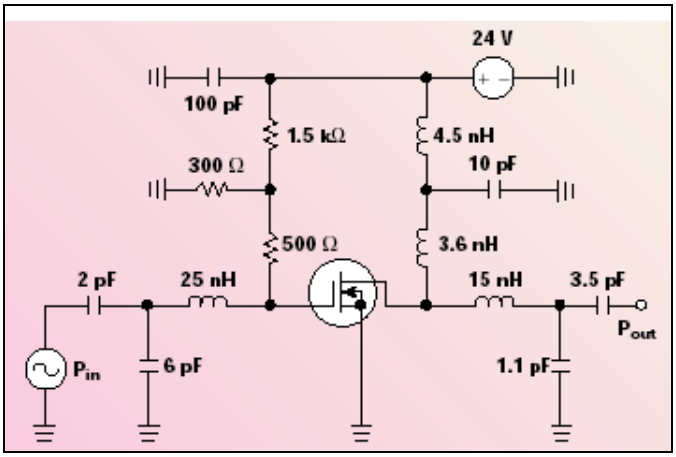

Fig. 2.4 - The simulated 500 MHz one-stage lumped power amplifier's equivalent circuit.

2.3 Amplifier Classifications

Amplifier circuits are classified as A, B, AB and C for analogue designs, and class D and E for switching design. In order to operate a transistor for a certain classes, the gate and drain DC voltages have to be biased carefully to the certain operation point (quiescent point or q-point). The reason is that the choice of q-point greatly influences linearity, power handling and efficiency. In addition, as can be seen further, the choice of optimal q-point is important for a certain operation frequency. Figure 2.5 shows typical classes that are chosen according to specific requirements [Grigouri Doudorov, 2003].

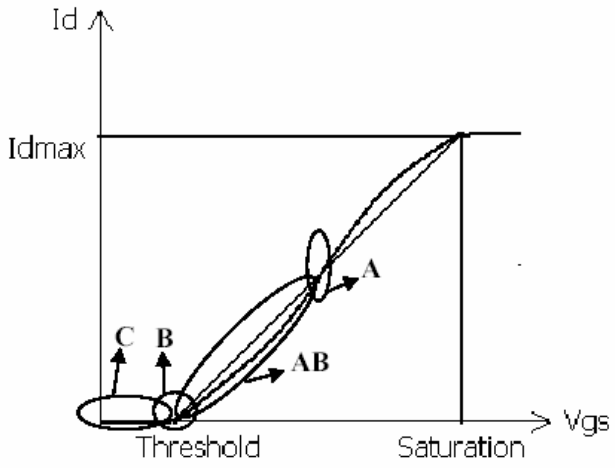

Figure 2.5 - Classes of operation of Power amplifier based on transfer characteristics

2.3-1 Class A

Class-A is the most linear amplifier with the q-point biased close to half of the maximum drain current. The class-A amplifiers are also characterized by maximum possible conduction angle (2π) and rather low DC power efficiency (equal or less than 50% in theory).

In a Class A circuit, the amplifying element is biased such that the device is always conducting to some extent, and is operated over the most linear portion of its characteristic curve (known as its transfer function or transconductance curve). Because the device is always conducting, even if there is no input at all, power is wasted. This is the reason for its inefficiency [Grigouri Doudorov, 2003].

Figure 2.6 shows ideal transfer characteristic with biased q-point for class-A operation. The strongly non-linear effect (overdrive) occurs only when the drain current exceeds its saturation point (pinch-off) and/or gets into sub threshold region (cut-off)

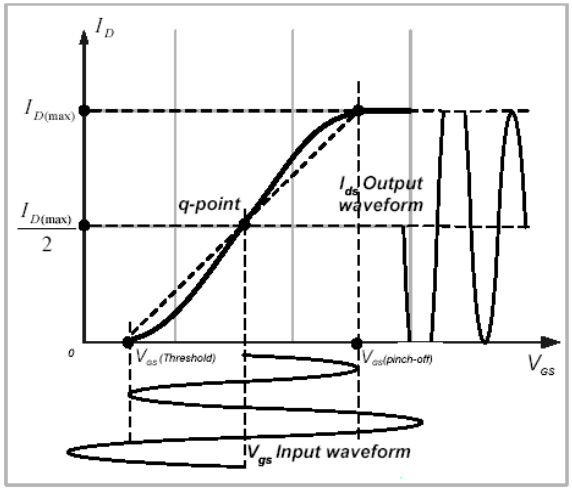

Fig 2.6- Class-A V_{GS} -I_{DS} transfer characteristic.

2.3-2 Class B

Class B amplifiers only amplify half of the input wave cycle. As such they create a large amount of distortion, but their efficiency is greatly improved. This is because the amplifying element is switched off altogether half of the time, and so cannot dissipate power.

A single Class B element is rarely found in practice, though it can be used in RF power amplifiers where the distortion is unimportant. A practical circuit using Class B elements is the complementary pair or "push-pull" arrangement. Here, complementary devices are used to each amplify the opposite halves of the input signal, which is then recombined at the output. [http://www.answers.com/electronic%20amplifier%20].

For a class-B amplifier the operation point has to be selected at the threshold voltage to achieve high power efficiency (equal or less 78 % in theory). In a given case the linear characteristics drastically decrease due to the fact that the conduction angle is half as that for class-A (Figure 2.7).

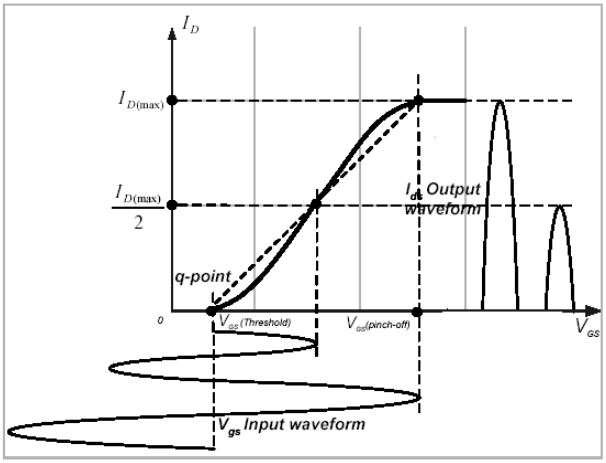

Fig 2.7- Class-B V_{GS} -I_{DS} transfer characteristic.

2.3-3 Class AB

The class-AB amplifier shows a flexible solution for a trade-off between linearity and efficiency of the previous classes. In this mode the q-point has to be chosen in between A and B points with its exact place being a matter of application requirements. Therefore, the conduction angle is π-2π and typically chosen closer to the threshold voltage (Figure 2.8).

Class AB is a solution of 'crossover distortion'. Crossover distortion is a small glitch at the "joins" between the two halves of the signal from the complementary pair or "push-pull" arrangement of Class B. Here, complementary devices are used to each amplify the opposite halves of the input signal, which is then recombined at the output. This arrangement gives excellent efficiency, but can suffer from the drawback that there is a cross-over distortion. [http://www.answers.com/electronic%20amplifier%20].

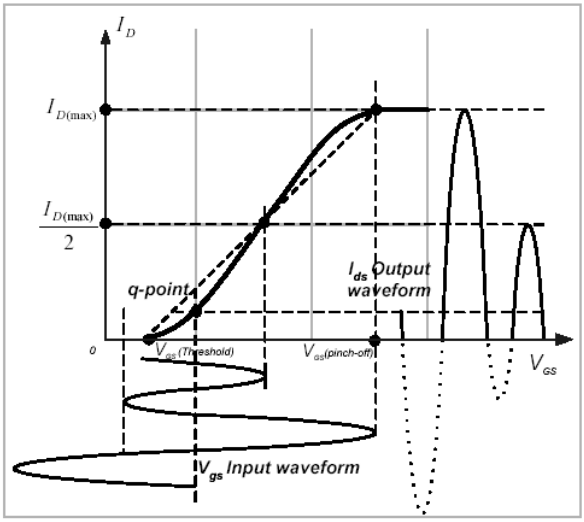

Fig 2.8- Class-AB V_{GS} -I_{DS} transfer characteristic.[GRIG00]

2.3-4 Class C

Class C amplifiers conduct over less than 50% of the input signal (Fig. 2.9). As such the distortion at the output is gross, but very high efficiencies can be reached—up to 90% or so. Some applications can tolerate the distortion, such as audio bullhorns. A much more common application for Class C amplifiers is in RF transmitters, where the distortion can be vastly reduced by using tuned loads on the amplifier stage. The input signal is used to roughly switch the amplifying device on and off, which causes pulses of current to flow through a tuned circuit. The tuned circuit will only resonate at one particular frequency, and so the unwanted harmonics are suppressed, and the wanted full signal (sine wave) will be developed across the tuned load. Provided the transmitter is not required to operate over a very wide band of frequencies, this arrangement works extremely well. Any residual harmonics can be removed using a filter [http://www.answers.com/electronic%20amplifier%20].

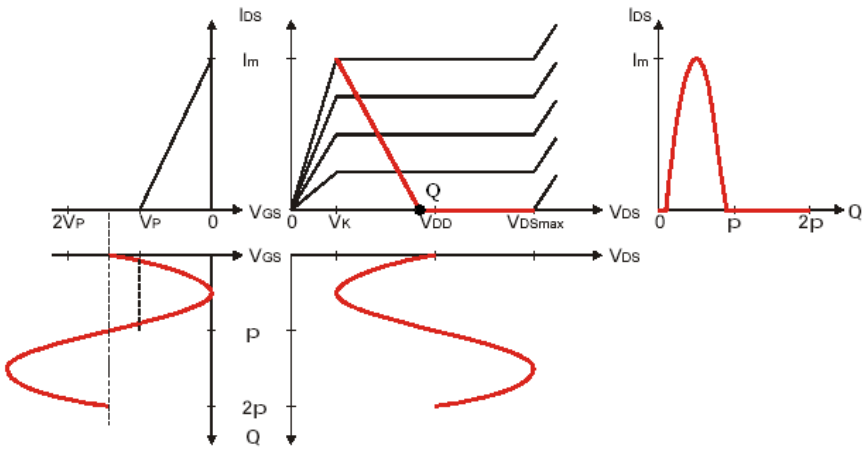

Fig 2.9- Class-C V_{DS}- I_{DS} transfer characteristic.

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2.3-5 Other High-Efficiency Classes

There are other high-efficiency amplifiers such as D, E, F, G, H, and S. These classes use different techniques to reduce the average collector or drain power, which, in sequence, increase the efficiency. Classes D, E, F and S use a switching technique, while classes G and H use resonators and multiple power-supply voltage to reduce the collector current-voltage product.

Designers select the class type to be used based on the application requirements. Classes-A, AB, and B amplifiers have been used for linear applications such as amplitude modulation (AM), single-sideband modulation (SSB), and quadrate amplitude modulation (QAM). Also it can be used in linear and wide band applications such as the multi–carrier power amplifier. Classes C, D, E, F, G, and H have satisfied the need for narrowband tuned amplifiers of higher efficiency. Such applications include amplification of FM signals [Saad Al-Shahrani, 2001].

Table 2-0 brings together comparisons for different classes in terms of quiescent point and conduction angle for amplifier classes A, B, AB and C.

Table 2.0- Quiescent point and conduction angle for amplifier classes A, B, AB and C.

Classes	q-point (Vq)	Quiescent current	Conduction Angle	Max Efficiency
A	0.5	0.5	2π	50%
B	0	0	π	78%
AB	0-0.5	0-0.5	π-2 π	50%-78%
C	<0	0	0- π	Approaches to 100%

2.4 LDMOS Power Amplifier

LDMOS power amplifiers used in transceiver circuits exhibits varying degrees of nonlinearity, depending on its class of operation. The output current's harmonic content varies with the DC bias at the gate of the LDMOS device, while maintaining a constant RF input signal. In certain applications, it may be desirable to have the transistor conducting for only a certain portion of the input signal. The portion of the input RF signal for which there is an output current determines the class of operation of a power amplifier [Vani Viswanathan, 2004].

2.5 Z-Match

Z-Match is a software implementation of the well known paper Smith Chart developed by Philip Smith at Bell Laboratories in 1939. It retains all of the graphical advantages of the original Smith Chart while incorporating many features to eliminate repetitive calculations and to make the chart more accessible to all users. Z-Match brings the power and versatility of the Smith Chart to the professional user and novice alike. (http://www.ohioautomation.com/simulation_products.html).

2.6 Advanced Design System (ADS) version 2004A

Advanced Design System is a powerful electronic design automation software system. It offers complete design integration to designers of products such as cellular and portable phones, pagers, wireless networks, and radar and satellite communications systems [Helpfile, Agilent Technologies].

ADS version 2004A, is the latest version, now in final testing and quality assurance, offers significantly improved ease-of-use and productivity as compared with any previous ADS release. This is especially true for the most common circuit design tasks: linear simulation, tuning, and the basic operations in schematic, simulation setup, data display, and layout. [(Helpfile, Agilent Technologies].)

2.7 Characteristics of Power Amplifier

Performance of amplifier is measured based on three crucial aspects. The aspects emphasized are efficiency, gain, operation at 1dB Gain Compression Point (power output) and noise.

2.7-1 Efficiency

The efficiency of an amplifier is measured in two ways. Power-added efficiency (PAE) is calculated as the output power minus the input power, divided by the DC power.

$$\eta_{PAE} = \frac{P_{OUT-} P_{IN}}{P_{DC}} \qquad (2.0)$$

Drain efficiency is calculated as the output power divided by the DC power. The definition of the drain efficiency can be represented in an equation form as

$$\eta = \frac{P_{OUT}}{P_{DC}} \qquad (2.1)$$

2.7-2 Gain

There are different definitions of the gain. The most useful is transducer gain, which is the ratio between the power delivered to the load and the power available from the source. Transducer gain can be expressed by:

$$G = \frac{P_S}{P_L} \qquad (2.2)$$

PS is the RF drive power and PL is the output RF power. The typical value of the transducer gain for a RF PA is 10-15 dB (assumed one-stage structure) [Grigouri Doudorov, 2003].

~~2.7.3~~2.7-3 1dB Gain Compression Point (power output)

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The point (on the P_{OUT} versus P_{IN} plot) at which the power gain of the transistor, due to non-linearities, is reduced by 1 dB from its small signal linear power gain value~~,~~ [Matthew M. Radmanesh, 2001].

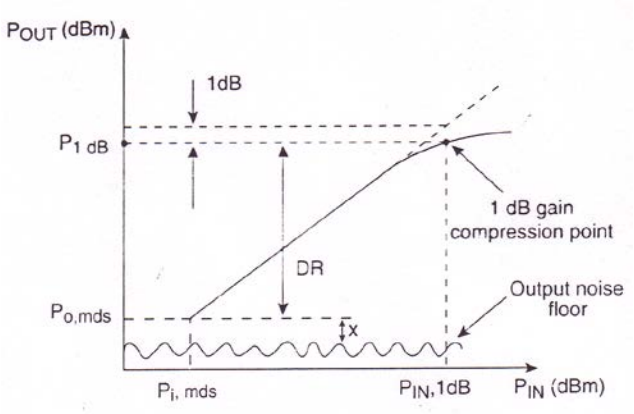

Figure 2.10- Pout vs. Pin, 1dB compression point.

At low drive levels, the output power is proportional to the input power. However, as the power goes beyond a certain point, the gain of the transistor decreases, and eventually the output power reaches saturation. The point where the gain of the amplifier deviates from the linear, or small-signal gain by 1 dB (about 1% distortion) is called the 1 dB compression point and it is used to characterize the power handling capabilities of amplifiers. $P_{IN,1dB}$, at the 1 dB compression point is related to corresponding output power, by $P_{OUT,1dB}$ by,

$$P_{OUT,1dB} = P_{IN,1dB}(dBm) + G_{1dB}(dB) \tag{2.2}$$

where G_{1dB} is the gain at the compression point.

2.7-4 Noise

The noise is defined with the Noise Factor (N). The Noise Factor is linear and equal the signal-to-noise ratio at the output divided by the signal-to-noise ratio at the input. Thus it is a figure of merit for how much noise that is added by the system itself. In the ideal case, when the system is completely noiseless the noise factor equals unity. The Noise figure (NF) is an expression of the noise factor in dB. Noise is less important for PAs, since it is the last active device in the transmitter building block chain. The Fries formula for the total noise factor for a cascaded system shows the importance of first stages [Grigouri Doudorov, 2003].

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{2.2}$$

The last statement in this formula, typically, is for the PA. The gain from previous stages decreases the noise impact of the PA.

CHAPTER 3

DESIGN METHODOLOGY

3.0 Introduction

This chapter discusses the research methods of this project that would be carried out. The discussion will cover the explanation of the procedure and the instruments used in this project.

Furthermore, the simulation power amplifier techniques were described in this chapter. The topic includes the method used on non-linear model provided by Motorola to get high optimum efficiency. The software application used throughout the whole simulation process is the Advanced Design System (ADS) version 2003A and 2004A from Agilent Technologies.

The block diagram of Figure 3.0 represents a typical circuit of single stage amplifier circuit considered in the simulation modification process. There are Input Matching Network (IMN) and Output Matching Network (OMN), and characteristic impedances of the input and output ports are assumed to be 50 Ohm.

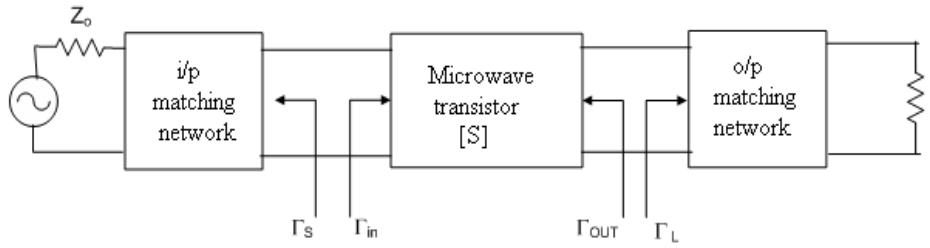

Fig 3.0– A single stage amplifier circuit

3.1 Supporting Software

3.1-1 Software Specifications

All simulations and analysis were performed using two types of software, Z-Match and Advanced Design System.

Using software Z-Match where Smith Chart tools can be used to get value of lumped components for matching networks is easier compared to constructing the model physically because the Smith Chart tools allows the designer to design ladder networks directly from the Smith chart. It is easier to control the drawing of lines as the cursor is moved, change parameters, changes between impedance and admittance chart, changes the mode of the screen displays, sets design parameters and redraws the chart

Advanced Design System (ADS) version 2004A was useful as it enables designers to easily access the functionality of ADS for common circuit-design tasks, including basic operations in schematic, simulation setup, linear simulation, tuning and viewing results. Results (in dB) were compared after application of matching, optimizing and tuning to see the improvement in minimizing power reflection of input and output matching network.

3.2 S-Parameter Simulation

The S-parameter simulations were implemented here to choose the topology for the matching networks. ~~Below~~ Table 3.1 ~~are~~contains S-parameter values of non-linear model at frequency 520 MHz: Results of simulation for both models; S11, S12, S21 and S22 in dB are shown in Figure A-1, and A-3 and in magnitude and angular, are shown in Figure A-2 and A-4 (Appendix A).

Table 3.1 - S-parameter value of both non-linear models at frequency 520 MHz

Models	S11 (dB)	S22 (dB)	S21 (dB)	S12 (dB)
RD01MUS1	0.819<-169.73	0.538<-151.888	6.161<66.927	0.044<-25.853
RD07MVS1	0.968<177.366	0.900<177.464	1.008<63.654	0.007<-32.501

~~*Table 3.0 - S-parameter value of non-linear model RD01MUS1 at frequency 520 MHz*~~

~~S11~~		~~S21~~		~~S12~~		~~S22~~	
~~(mag)~~	~~(ang)~~	~~(mag)~~	~~(ang)~~	~~(mag)~~	~~(ang)~~	~~(mag)~~	~~(ang)~~
~~0.837~~	~~-156.502~~	~~4.411~~	~~62.128~~	~~0.052~~	~~-31.328~~	~~0.634~~	~~-131.184~~

~~*Table 3.1 - S-parameter value of non-linear model RD07MVS1 at frequency 520 MHz*~~

~~S11~~		~~S21~~		~~S12~~		~~S22~~	
~~(mag)~~	~~(ang)~~	~~(mag)~~	~~(ang)~~	~~(mag)~~	~~(ang)~~	~~(mag)~~	~~(ang)~~
~~0.951~~	~~178.679~~	~~0.982~~	~~44.765~~	~~0.010~~	~~-51.928~~	~~0.893~~	~~-178.519~~

~~3.3~~Stability Condition of Transistor

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