DESIGN OF DIGITAL TO ANALOG CONVERTER (DAC) FOR INTEGRATED BLUETOOTH APPLICATIONS USING 0.18µm CMOS TECHNOLOGY

Oleh

Low Pit Xing

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ABSTRAK

Penukar isyarat digital ke analog (digital to analog converter, DAC) merupakan salah satu elemen yang penting dalam bidang perhubungan. Dalam projek ini, satu litar penukar isyarat digital ke analog yang beroperasi pada bekalan voltan 1.8V telah diimplementasikan berdasarkan proses teknologi Silterra CMOS 0.18µm. Penukar isyarat digital ke analog yang dibina ini adalah litar penukar masukan selari 8-bit jenis *R*-2*R*. Penukar isyarat digital ke analog ini berfungsi dengan satu voltan rujukan (V_{ref}) dan mengeluarkan keluaran arus. Satu penguat kendalian (operational amplifier, op-amp) disambungkan pada hujung keluaran rangkaian *R*-2*R* untuk menukarkan arus keluaran ini kepada voltan keluaran yang sesuai. Litar penguat kendalian yang digunakan ini adalah jenis "cermin-arus" (current mirror) yang mempunyai gandaan voltan gelung terbuka 24.64dB. Di samping itu, penguat kendalian ini mempunyai lebar jalur 21.5MHz, dengan lesapan kuasa 0.85mW. Voltan rujukan kepada litar penukar pula dibekalkan oleh blok litar lain yang dikenali sebagai litar rujukan sela jalur (bandgap reference). Litar rujukan sela jalur ini terdiri transistor, penguat kendalian, perintang dan diod CMOS. Secara keseluruhannya, litar penukar isyarat digital ke analog itu mempunyai "settling time" 8ns, bermaksud kadar pensampelan data sebanyak 125MHz, dengan lesapan kuasa sebanyak 31.356mW. Skematik dan penyelakuan (atau simulasi) bagi seluruh litar adalah dilakukan dengan perisian komputer yang dikenali sebagai, Cadence, Virtuoso dan Spectre.

ABSTRACT

Digital to analog converter (DAC) is one of the important elements in the communication circuits. In this project, a digital to analog converter which operates with 1.8V voltage supply is implemented based on 0.18μm Silterra CMOS process technology. The implemented digital to analog converter is an 8-bit parallel inputs *R*-2*R* architecture converter. The digital to analog converter operates with a reference voltage and provides a current output. An operational amplifier is connected at the output end of the *R*-2*R* network to convert the output current to suitable output voltage. This operational amplifier is a current mirror op-amp with open loop dc voltage gain of 24.64dB. Besides, this op-amp achieves bandwidth of 21.5MHz, with the power consumption of 0.85mW. The mentioned reference voltage is established by another circuit block which known as bandgap reference voltage circuit. This bandgap reference voltage circuit is simply composed of CMOS transistors, op-amp, resistors and diodes. The overall D/A converter circuit has the settling time 8ns, which means the data sampling rate of 125MHz, with power consumption of 31.356mW. The schematic entry and simulation of the whole DAC circuits is done using the software Cadence, Virtuoso and Spectre.

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CHAPTER 1

INTRODUCTION

1.1 Project Background

For recent years, wireless local area network is gaining more attention as candidate for flexible connection among multi-media device. Bluetooth is an up-coming wireless standard operating at 2.4GHz ISM (Industrial, Scientific, and Medical) band.

The Bluetooth standard defines short-range wireless connection between mobile phones, mobile PCs and other portable devices (Bluetooth, 2001). It specifies a 2.4-GHz frequency-hopped spread-spectrum system that enables the users to easily connect to a wide range of computing and telecommunication devices without the need for wires or cabling of any kind. Space and cost considerations are among the primary motivators for the drive toward a single-chip radio solution. Bluetooth uses the unlicensed 2.4-GHz ISM band, and supports a moderate data rate of 1 Mb/s at 10m distance. The modulation scheme is Gaussian binary FSK (GFSK), with frequency deviations of ±160 kHz around the carrier. The transceiver uses a time division duplexing system. A Bluetooth device must satisfy some certain requirements. It should be low cost and low power to integrate with other portable devices efficiently, and yet it must have a robust performance to function properly along with interferers.

Let's refers to the simple block diagram of a direct conversion transceiver given in (Seung-Wook Lee et al., 2001). All functional blocks from LNA to ADC in receiver block and DAC to Pre-Amp in transmitter block are included in the transceiver.

The idea of this project is to design a DAC which are compatible and will integrated into a transmitter uses direct conversion architecture, to achieve low power consumption, and high level integration.

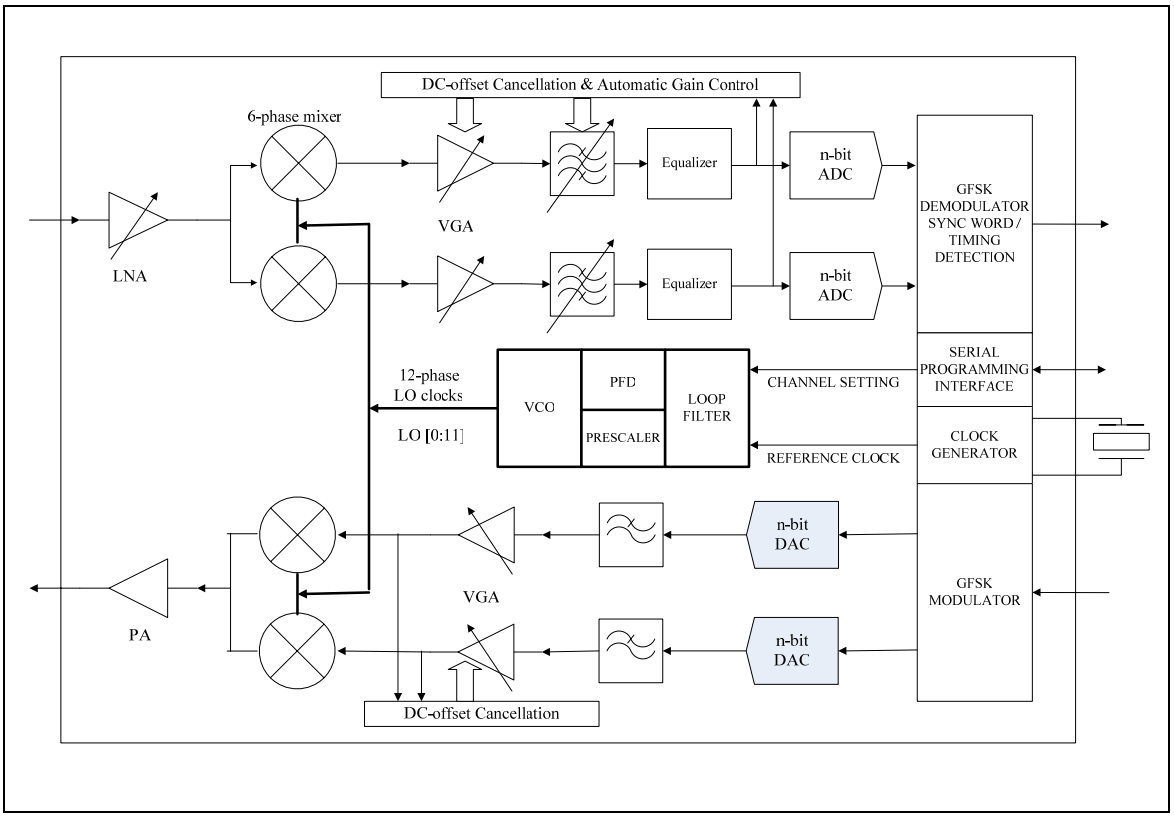


Figure 1.1: Bluetooth transceiver architecture.

1.2 Project Objective

The purpose of this project is to implement an 8-bit parallel input digital to analog converter with *R*-2*R* architecture using 0.18μm Silterra CMOS process technology. The DAC circuit is aim to operate with 1.8V voltage supply and having a sampling rate of 100MHz. The DAC circuit will convert the digital data from an input system to analog signal output before the signals go to the filter, amplifier, mixer and transmitter.

1.3 Project Scope

The scope of this project include the literature review in understanding and choosing the architecture of the DAC circuit and others circuit blocks like op-amp and bandgap reference voltage circuit. The whole circuit is design and simulate from the aspects of dc, ac and transient response using the Cadence software. The characteristic

of the whole DAC circuit such as linearity, power consumption, stability and noise performance is then observe and investigate.

1.4 Report Guide

In general this report is divided into & chapters. Chapter 1 is an introduction intends to provide a short review for the project. Objectives and scope of the project is specified in this chapter as to clarify the purpose of this thesis.

Chapter 2 gives some introduction about the operation theory of the DAC. It also gives some overview on three basic types, architectures of D/A converter circuits.

Chapter 3 explain the choosing of type of D/A converter as the object of this project, and also dives some introduction to the building blocks of the whole D/A converter circuit which is going to be implemented. op-amp and bandgap reference voltage circuits based on literature.

Chapter 4 and 5 will further explain the circuit and operation of the building blocks inside the D/A converter circuit, which is the bandgap reference circuit and output stage op-amp, respectively.

Chapter 6 are divided into several sections, each section will present the simulation result of the different circuit blocks. And the final section will shows the simulation result of the whole D/A converter, integrated of all building blocks.

Chapter 7 draws the final conclusion of this work and suggests the future work as the continuation of this work.

1.5 Methodology

Literature review is done based on various sources, especially the journals, technical reports, thesis, reference books and internet. After reviewing various architecture of the DAC circuit, the most suitable circuit structure, architecture and design approach for high speed data conversion is chose. The schematic entry is done using software Cadence, Virtuoso. And then the circuit is simulated using Spectre simulation host. After the correct output waveform and voltage level is obtained through simulation, the performance of the circuit is then investigated from various aspects.

CHAPTER 2

DIGITAL TO ANALOG CONVERTER

2.1 Introduction

Data converters are crucial building blocks in modern communications systems where DSPs are extensively used. A D/A converter is usually needed at the transmit side and A/D converter is usually needed at the receive side.

The digital to analog conversion circuits, which are also called D/A converters, or DACs, can be considered as decoding devices that accepts digitally coded signals and provide analog outputs in the form of currents or voltages. In this manner, they provide an interface between the digital signals of the computer systems and continuous signals of the analog world.

Figure 2.1 illustrates how digital to analog (D/A) converters are used in data systems.

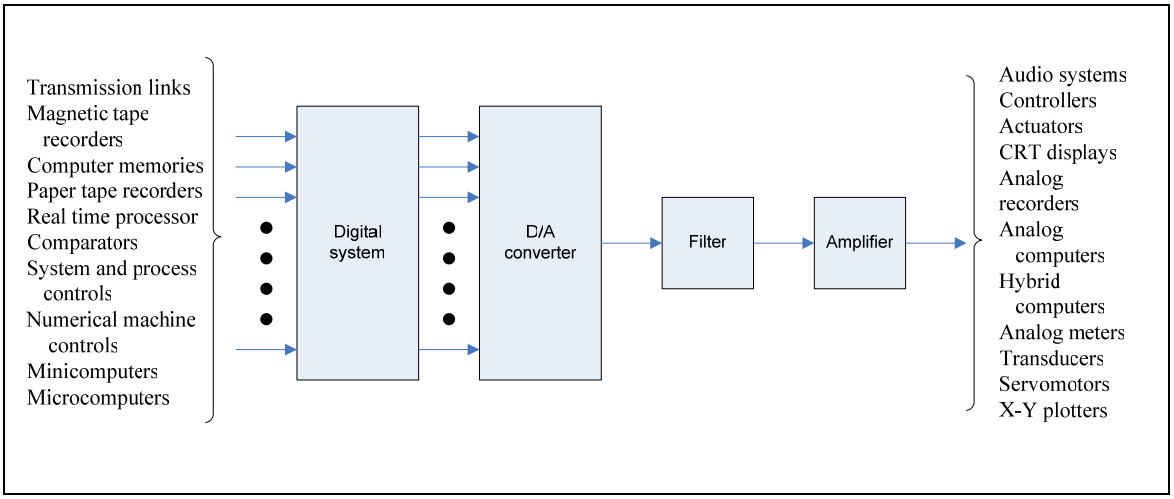


Figure 2.1: DACs in signal processing systems.

Figure 2.2 shows a conceptual functional block diagram of a basic D/A converter system. The input to a D/A converter is a digital word D, of N bits (b_1, b_2, b_3,…, b_N), and a reference signal, V_{ref}. The output analog quantity A, which can be a voltage or a current, is related to the input as

$$A = KV_{ref} D \tag{2.1}$$

where K is a scale factor, V_{ref} is a reference voltage, and D is the digital word of a given number of bits. D can be represented as

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \ldots + \frac{b_N}{2^N} \tag{2.2}$$

where N is the total number of bits, and b_1, b_2, b_3,… are the bit coefficients, which are quantized to be either a 1 or a 0. Thus, the transfer function of an N-bit D/A converter can be written as

$$A = KV_{ref} \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \ldots + \frac{b_N}{2^N} \right) \tag{2.3}$$

or

$$A = KV_{ref} \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_N 2^{-N} \right)$$

$$= KV_{ref} \sum_{j=1}^{N} b_j 2^{-j} \tag{2.4}$$

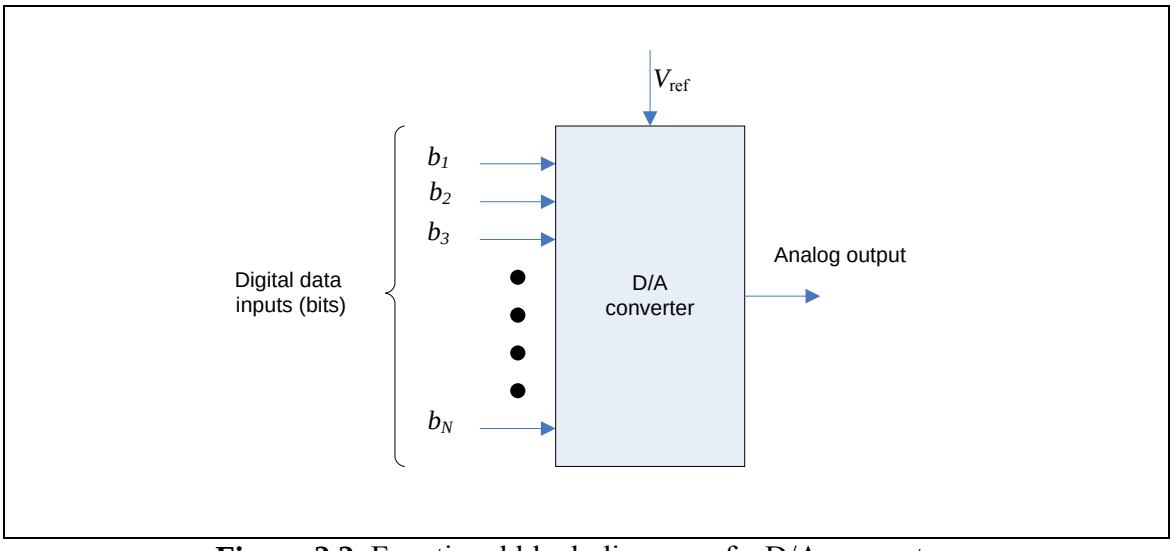


Figure 2.2: Functional block diagram of a D/A converter.

In its most commonly used form, the basic D/A converter system of Figure 2.2 consists of four separate blocks, as shown in Figure 2.3: a reference voltage source which generates V_{ref}, a set of binary switches which set the binary bit coefficients (b_1 through b_N), a scaling network convert the digital word as either voltage or current

signal, and the output amplifier converts this signal to a voltage signal that can be sampled without affecting the value of the conversion.

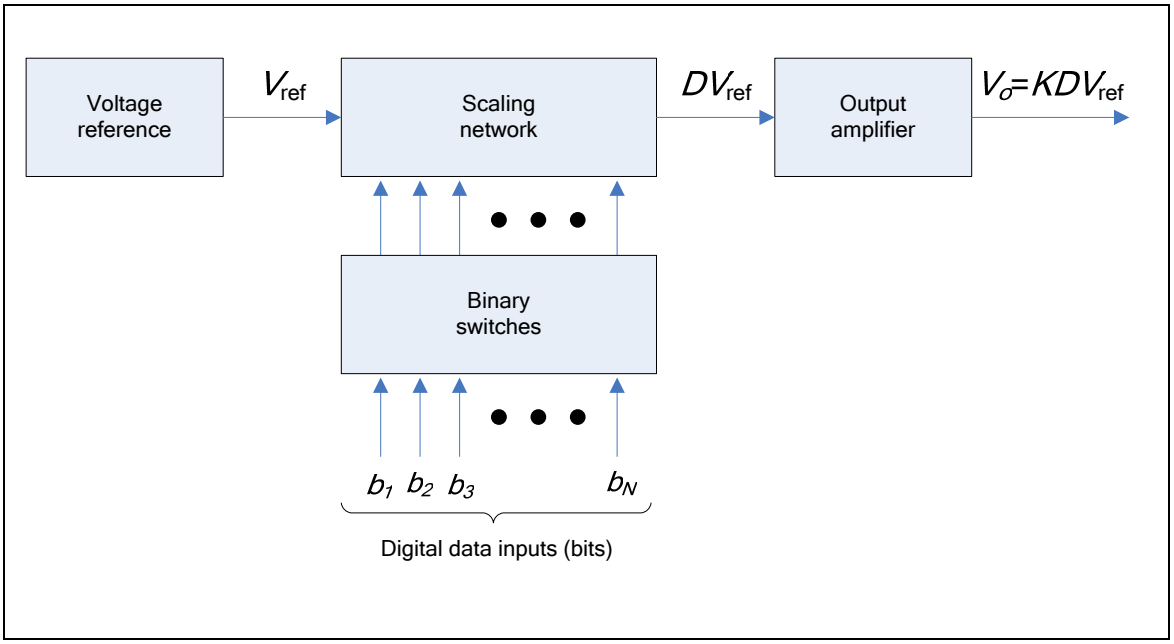


Figure 2.3: Internal blocks of a D/A converter.

Assuming a voltage output, the transfer function of an N-bit D/A converter can be written as

$$V_o = V_{FS}\left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_N 2^{-N}\right) \tag{2.5}$$

where V_{FS} is the full scale output voltage, which is equal to KV_{ref} of Eq. (2.4). As a function of the input binary word which determines the bit coefficients, the output exhibits 2^N discrete voltage levels ranging from zero to a maximum value of

$$\left(V_o\right)_{\max} = V_{FS}\frac{2^N - 1}{2^N} \tag{2.6}$$

with a minimum step change ΔV_o given as

$$\Delta V_o = \frac{V_{FS}}{2^N} \tag{2.7}$$

In practical implementations of the circuit, as shown in the block diagram of Figure 2.3, the digital input signal activates the binary switches within the converter, which in turn set the values of the bit coefficient b_1 through b_N. The bit coefficient b_1 is

called the most significant bit (MSB) since it carries the highest numerical weight. In a binary-weighted converter whose transfer function is given in Eq. (2.5), 1 MSB change creates an analog output level shift equal to $V_{FS}/2$.

The bit coefficient b_N associated with the last bit of an N-bit input word carries the least numerical weight and is called the least significant bit (LSB). It is designates the smallest analog step size available at the output [see Eq. (2.7)] and is equal to $V_{FS}/2^N$.

Note that in a binary weighted D/A converter circuit, as described by the Eq. (2.5), the output is zero when all binary bit coefficients are equal to zero, and is 1 LSB less than of the full scale output when all bit coefficients are equal to 1.

In the process of D/A conversion, the digital input can be applied either in parallel format (as shown in Fig 2.3) or serially, that is, one bit at a time, starting with the MSB. In almost all cases, parallel input is preferred since it greatly speeds up the conversion process.

The resolution of the converter is the smallest analog change that can be produced by a D/A converter. Resolution is commonly expressed in the number of bits, N, where the converter has 2^N possible states. The finite resolution of converters causes an inherent uncertainty in digitizing an analog value. This uncertainty is called the quantization noise and has a value of up to ± 0.5 LSB or $\pm\ V_{FS}/2^{N+1}$.

The full scale range (FSR) is the difference between the maximum and minimum analog values and is equal to V_{FS} as N approaches infinity. The dynamic range (DR) of a noiseless converter is the ratio of the V_{FS} to the smallest difference it can resolve. Thus, the DR can be given as

$$\mathrm{DR} = 2^N \tag{2.8}$$

or in terms of decibels as

$$DR(dB) = 20\log_{10}(2^N) = 6.02N \tag{2.9}$$

2.2 Basic D/A Converter Circuit

A large number of D/A conversion techniques have been developed and are well covered in the literature. Some of the very basic converter configuration will be shown in this section. The basic D/A converter circuits suitable for monolithic IC designs fall into three basic categories, based on their principles of operation: (1) current scaling circuits, (2) voltage scaling circuits, and (3) charge scaling circuits.

2.2.1 Current Scaling D/A Converter Circuits

In D/A converters operating on the current scaling principle, the conversion is achieved by generating a set of binarily weighted currents within the circuit, which are then selectively summed to provide an analog output. Figure 2.4(a) shows the general principle of the current scaling D/A converters, and Figure 2.4(b)&(c) shows two basic circuit configurations for generating and summing a set of binary weighted current I_1, I_2, I_3,…, I_N. The currents are generated by connecting a binary weighted resistor network across the voltage reference V_{ref}. The positions of the switches S_1, S_2, S_3,…, S_N simulate the values of the bit coefficients b_1, b_2, b_3,…, b_N in Eq. (2.5). The output current I_o is then summed at the virtual ground point, that is, at the inverting input of the operational amplifier A; and results in an output voltage,

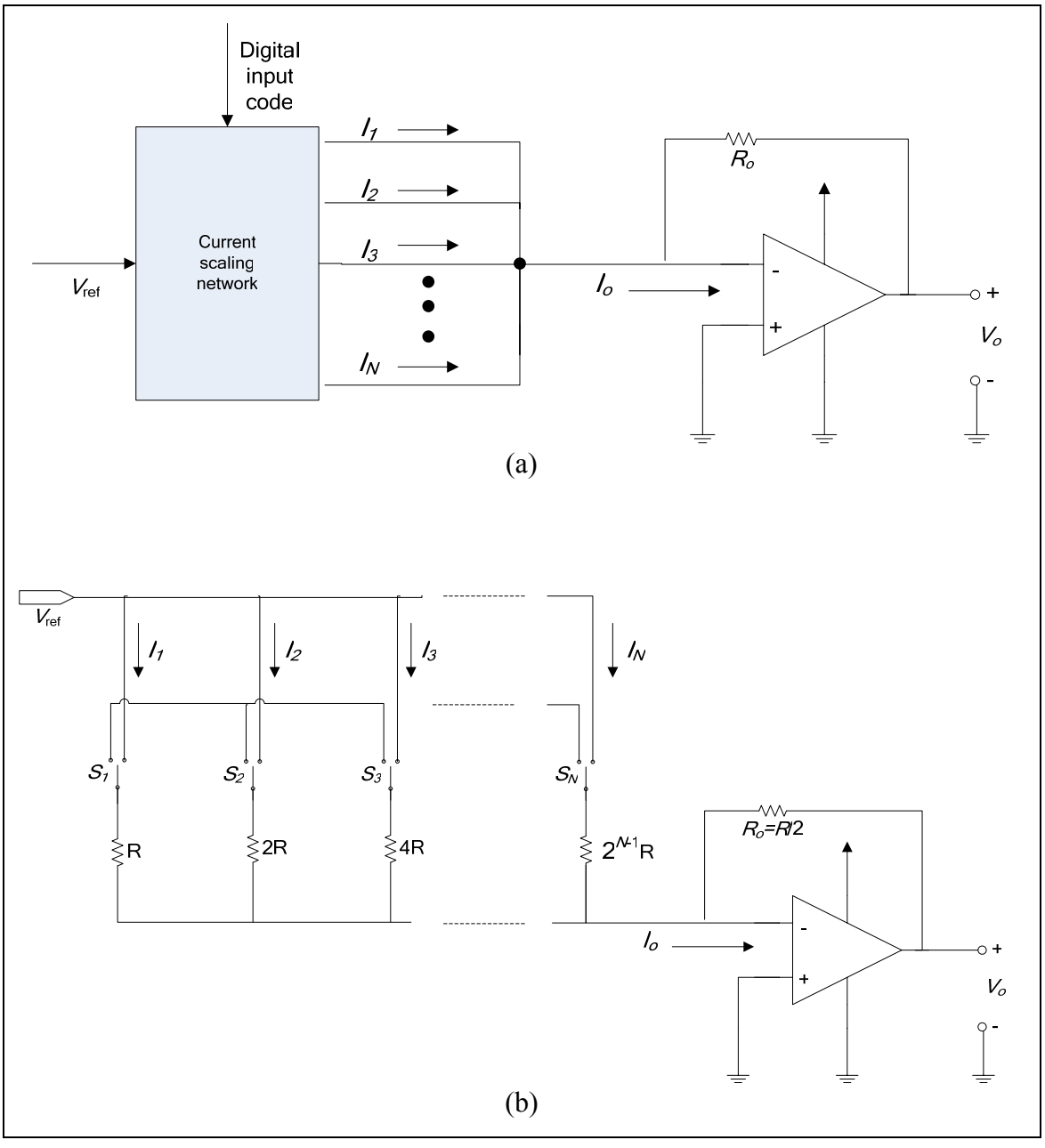
$$\begin{aligned} V_o &= -I_o R_o = -I_o \frac{R}{2} \\ &= -V_{ref}\left(\frac{b_1}{R}+\frac{b_2}{2R}+\frac{b_3}{4R}+\ldots+\frac{b_N}{2^{N-1}R}\right)\frac{R}{2} \\ &= -V_{ref}\left(b_1 2^{-1}+b_2 2^{-2}+b_3 2^{-3}+\ldots+b_N 2^{-N}\right) \end{aligned} \qquad (2.10)$$

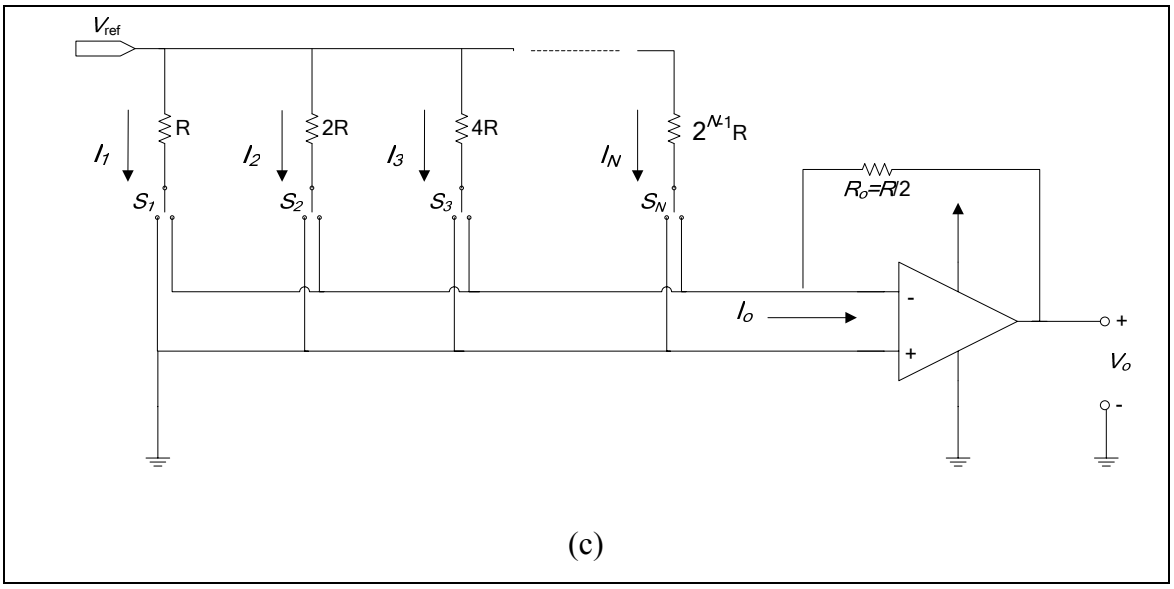
where the operational amplifier feedback resistor R_o, which sets the scale factor, is chosen to be equal to $R/2$ for convenience.

The binary bit coefficients are determined by the positions of the corresponding switches in the figure. One has the option of switching either a voltage or a current in the circuit, as a function of the digital input. In the circuit of Figure 2.4(a), voltage switching is employed where the voltage across any one of the weighting resistor is

switched either to ground or to V_{ref}. Figure 1.4b shows an alternate switching arrangement for the same circuit. In this case, one terminal of each of the resistors remains connected to V_{ref}, the other terminal is switched between the actual ground and the virtual ground formed at the operational amplifier input. This method of switching is called current switching.

In most applications, and particularly in integrated circuits, current switching is normally preferred over voltage switching because it offers significant speed advantages. (Alan B. Grebene, 1984).





(c)

Figure 2.4: (a) Conceptual illustration of a current scaling D/A converter, (b) Implementation with voltage switching, (c) Implementation with current switching.

In the D/A converter configurations shown in Figure 2.4 (a) & (b), the current weighting function is achieved by using N parallel, independent branches in the weighting network, which have respective impedance levels of R, $2R$, $4R$, $8R$ … In this type of resistor network, the spread of resistor values increases very rapidly as the numbers of bits increases, such that the resistance of the MSB branch is related to that of the LSB branch as

$$\frac{R_{MSB}}{R_{LSB}} = \frac{1}{2^{(N-1)}} \tag{2.11}$$

Thus, for example, for 8-bit resolution one needs a set of precision resistors covering a range of resistor values from R to $128R$. In monolithic circuits, such wide range of resistor values is difficult to obtain with sufficient precision without resorting to expensive trimming processes.

An alternate resistor array configuration which eliminates the large component spread of the binary weighted resistor network is the R-$2R$ ladder network shown in Figure 2.5. In this type of network, the binary division of the currents I_1, I_2, I_3…, I_N is achieved by successive partitioning of current between the shunt ($2R$) and series (R) branches. Thus, the branch currents still satisfy the binary relationship

$$I_1 = 2I_2 = 4I_3 = \ldots = 2^{N-1} I_N \tag{2.12}$$

while maintaining the resistor values within an easily attainable 2:1 ratio. The *R*-2*R* ladder requires twice as many resistors as the binary weighted resistor network and must be properly terminated by a termination resistor (see Figure 2.5).

For monolithic D/A converters, the *R*-2*R* ladder is generally preferred over the binary weighted ladder for circuits of 6-bit or higher complexity, because it offers a lesser spread of component values.

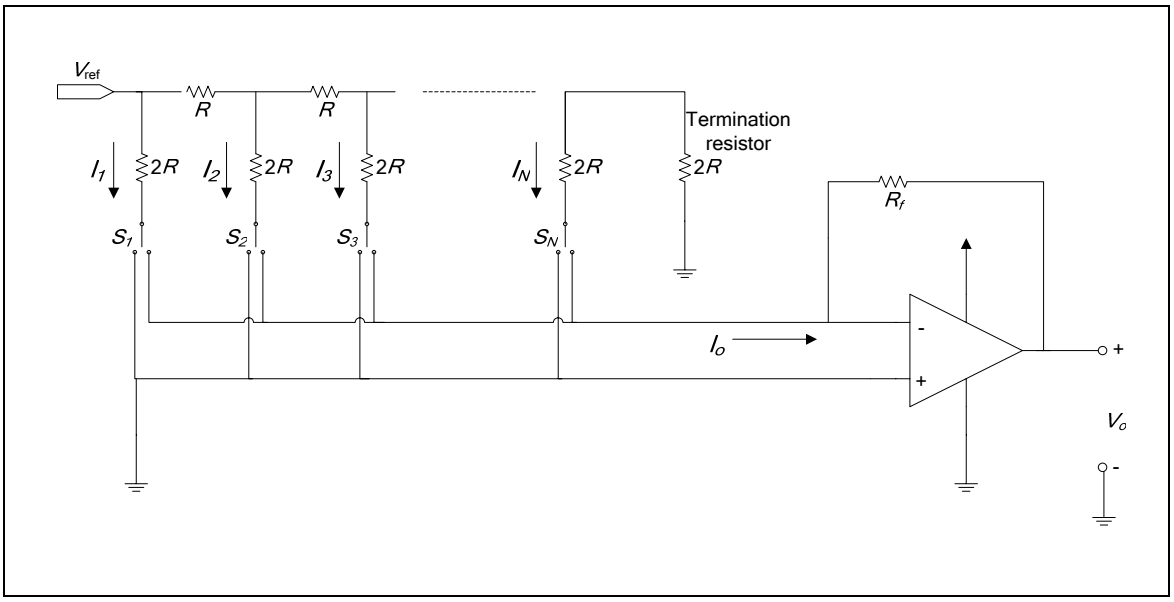


Figure 2.5: Current scaling D/A converter using *R*-2*R* ladder.

2.2.2 Voltage Scaling D/A Converter

Voltage-scaling D/A converters produce an analog output voltage by selectively "tapping" a voltage divider resistor string connected between the reference voltage and ground. For an *N*-bit converter circuit, the resistor string is made up of 2^N identical segments connected in series, and it is used as a potentiometer where the voltage levels between the resistor segments are sampled by means of binary switches.

Figure 2.6 shows the conceptual diagram of a 3-bit D/A converter operating on the voltage scaling principle. The resistor string is comprised of eight identical resistors, connected between V_{ref} and ground. The voltage drop across each resistor section is equal to 1 LSB of the output voltage change, or $V_{FS}/2^N$. The output is sampled by means of a decoding switch matrix, and is sensed by a high impedance buffer amplifier.

With reference to Figure 2.6, the operation of the switch matrix which decodes the input logic signal into an analog voltage can be described as follows. The analog switches marked *A*, *B*, and *C* are driven by the input logic lines corresponding to the input bits b_1, b_2, and b_3, where b_1 corresponds to the MSB and b_3 corresponds to the LSB. The switches designated $\overline{A}$, $\overline{B}$ and $\overline{C}$ are driven by the complements of the input logic levels.

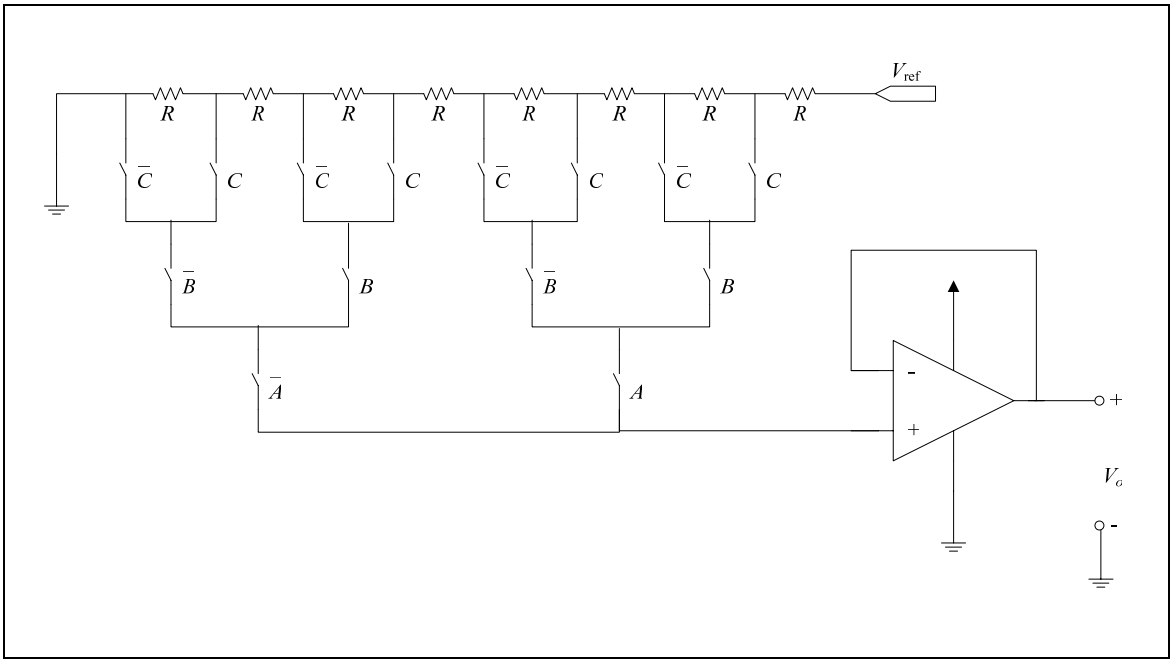


Figure 2.6: 3-bit converter example using voltage scaling principle.

An advantage of this architecture is that it guarantees monotonicity, since any tap on the resistor string must have a lower voltage than its upper, neighbor tap. Also, the accuracy of this D/A converter depends on the matching precision of *R* in the resistor string (David John, Ken Martin, 1997). One main drawback of the circuit for high bit count D/A conversion is the excessive number of components required. For *N*-

bit conversion, $2N$ resistors and approximately 2^{N+1} analog switches and $2N$ logic drive lines would be required.

2.2.3 Charge Scaling D/A Converter

Charge scaling D/A converters generate an analog voltage by scaling the total charge applied to a capacitor array. Their principle of operation can be illustrated by the simple circuit example of Figure 1.7. In the circuit, C_A is connected to ground, and C_B is periodically switched between ground and an internal reference voltage V_{ref}. Assume that, initially, both switches S_0 and S_1 are connected to ground. In this so called reset mode, both capacitors are discharged, and the output voltage V_X is equal to zero. Next, assume that S_0 is opened and S_1 is connected to a reference voltage V_{ref}. If the output is measured during this so called sample mode, one obtains an output voltage V_X

$$V_X = V_{ref} \frac{C_B}{C_A + C_B} \tag{2.13}$$

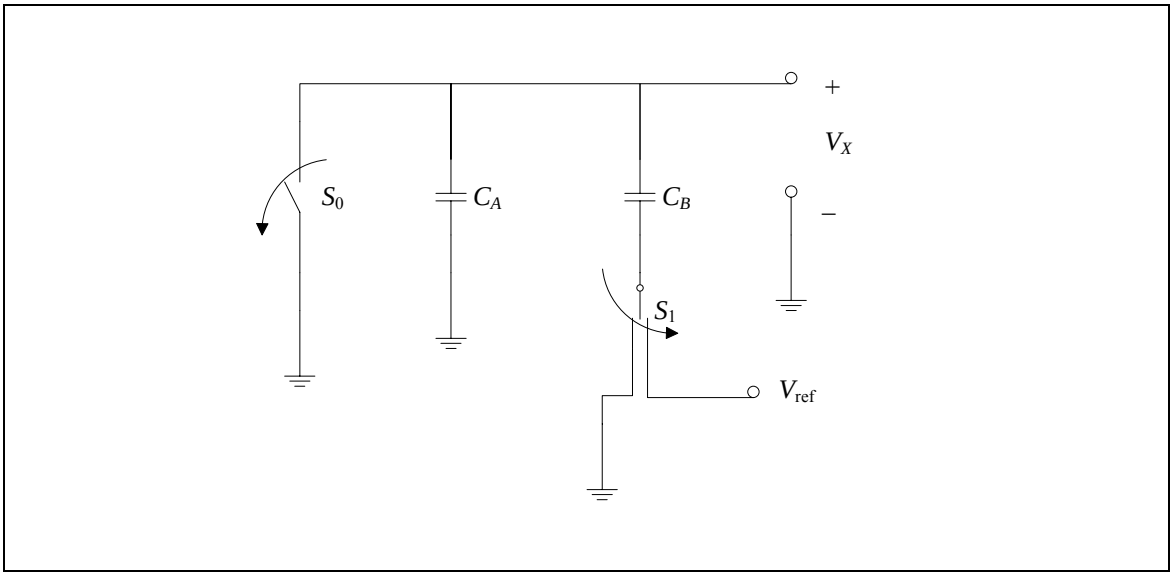


Figure 2.7: Illustration of charge scaling principle.

This same principle can be applied to the binary weighted capacitor array shown in Figure 2.8, where during the reset mode, all switches, including S_0, would be connected to ground; during the sample mode, S_0 would be opened and S_1 through S_N would be controlled by the binary bit coefficients associated with an N-bit digital input

signal. A logic 1 would cause the corresponding switch to be connected to ground. Under this condition, the output voltage would be given from Eq. (2.13) as

$$V_o = V_{ref} \frac{C_{eq}}{C_{tot}} \tag{1.14}$$

where C_{eq} is the sum of all capacitors connected to V_{ref} and C_{tot} is the total capacitance in the array.

C_{eq} is determined by the choice of individual coefficients b_1, b_2, b_3, … b_N, which set the switch positions in Figure 2.8. Thus, it can be expressed as

$$C_{eq} = b_1 C + \frac{b_2 C}{2} + \frac{b_3 C}{4} + ... + \frac{b_N C}{2^{N-1}} \tag{2.15}$$

where C is the largest capacitor in the binary weighted array, corresponding to the MSB data input. Similarly, the total capacitance C_{tot} in the array is

$$C_{tot} = C + \frac{C}{2} + \frac{C}{4} + ... + \frac{C}{2^{N-1}} + \frac{C}{2^{N-1}} = 2C \tag{2.16}$$

Combining Eqs. (2.14) through (2.16), one can express the output voltage during the sample mode as

$$V_o = V_{ref} \left(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + ... + b_N 2^{-N} \right) \tag{2.17}$$

which is the desired analog output corresponding to the N-bit binary input word.

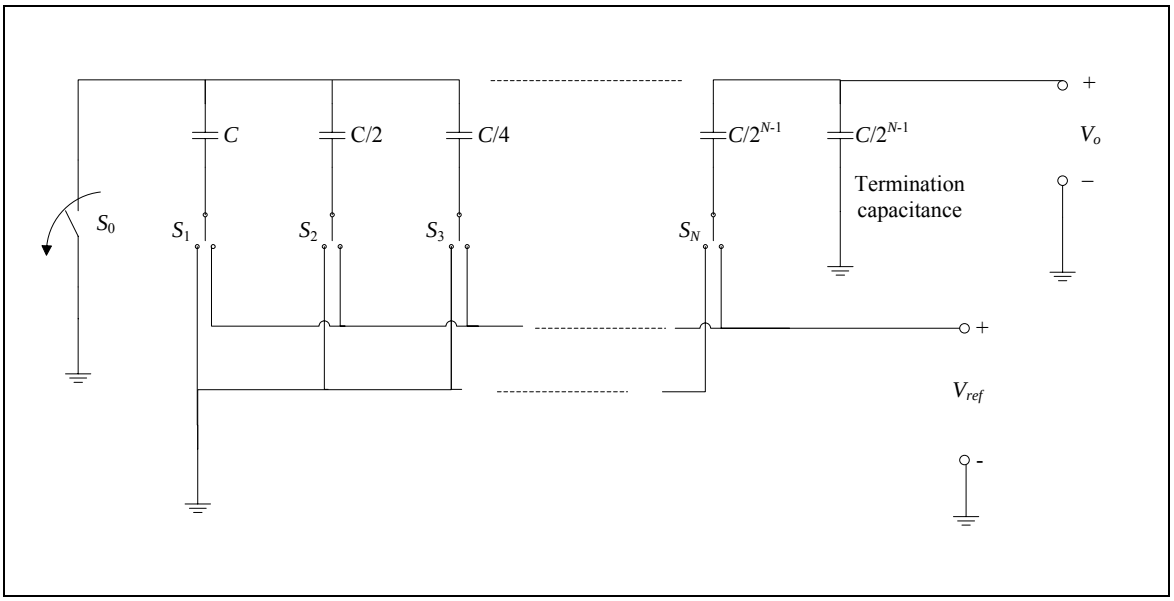


Figure 2.5: Simplified diagram of charge scaling D/A converter.

The accuracy of the capacitors and the area required are both factors that limit the number of bits used. The accuracy of the D/A converter is seen to depend totally on the capacitor ratios and any parasitics (Geiger et al., 1990). The only drawback of the circuit is the large capacitor ratios required for high bit count conversion. Similar to the case of binary weighted resistor ladders, the capacitor ratio between MSB and LSB capacitors is

$$\frac{C_{MSB}}{C_{LSB}} = 2^{N-1} \tag{2.18}$$

2.2.4 Overview Of Basic D/A Conversion Circuits

Although a wide range of D/A conversion techniques is available, the three basic D/A conversion methods outlined above are by far the most commonly used in monolithic IC design. The others types of D/A converter include serial DAC, algorithmic DAC, thermometer coded DAC, encoded DAC, hybrid DAC and etc. Table 1.1 gives a summary of these D/A converter (Alan B. Grebene, 1984; David John et al., 1997; Geiger et al., 1990; Mikael Gustavsson et al., 2002).

Table 2.1: Comparison of some D/A conversion techniques.

D/A converters	Advantage	Disadvantage
Current scaling, binary weighted	Fast; insensitive to switch parasitics	Large element spread; nonmonotonic
Current scaling, *R*-2*R* ladder	Fast; small element spread	Nonmonotonic; sensitive to switch parasitics
Voltage scaling	Monotonic	Large area; sensitive to parasitic capacitances
Charge scaling	Fast	Large element spread; nonmonotonic
Serial, charge redistribution	Simple; minimum area	Slow; requires complex external circuits
Serial, Algorithmic	Simple; minimum area	Slow; requires complex external circuits
Thermometer coded DAC	Monotonic; improved DNL and INL	Increase complexity, especially at high resolution
Encoded DAC	Monotonic; improved DNL and INL	For high speed, difficult opamp design, resistors' matching is crucial

CHAPTER 3

THE 8-BIT CMOS D/A CONVERTER

3.1 Selecting The D/A Architecture For The Project

In this project, it is aim to design a high speed DAC which is suitable to use in a communication system, integrate into the on chip Bluetooth transceiver circuit. As reported in (Bang-Sup Song et al., 2002; Min Chen et al., 2003; Sangjin Byun et al., 2003), the DAC used is type of parallel input current steering. Thus, an 8-bit current scaling *R*-2*R* D/A converter have been chosen as the object for this project (Alan B. Grebene, 1984; intersil AD7520, 2002; Analog Device AD7533,).

3.2 The 8-Bit CMOS D/A Converter

This DAC is essentially a resistor array with CMOS binary switches. The basic circuit configuration is shown in Figure 3.1. The DAC operates with a voltage references and provides a current output. An operational amplifier is used to convert the output current into an output voltage.

The digital-input buffer stages and the differential bit switches are implemented using CMOS transistors. Figure 3.2 shows the basic circuit diagram of one of the current switch stages, along with its driver. The driver stage is essentially a three-stage inverter chain. A small amount of internal positive feedback is provided from the output of the second stage to the first stage through the transistor Q_3, which increases the switching speed of the driver stage and adds a small amount of hysteresis to the logic threshold. The logic threshold is set to around 1.0V above ground, by proper scaling of the W/L ratio of Q_1 and Q_2.

The use of CMOS devices as current switches has the advantage of avoiding nonlinearity due to base current mismatches in bipolar transistor switches. However, since the switches are in series with the ladder network and ground, their series resistance is critical. The effect of this resistance is minimized by choosing high value for the ladder resistors (i.e., *R*).

When the digital input bit is 1, it will produce a high voltage level at the gate of Q_B, and switch on the transistor to let the current from the R-$2R$ ladder flow through it. On the other hand, the voltage at the gate of Q_A will be low, causing the transistor to switch off. When the digital input bit is 0, the situation will be reverse. That is, the voltage level at the gate of Q_A will be high, to switch on the transistor, and passing through the current. Meanwhile, the voltage level at the gate of Q_B will be low, causing the transistor to be switched off, and prevent the current to flow through it.

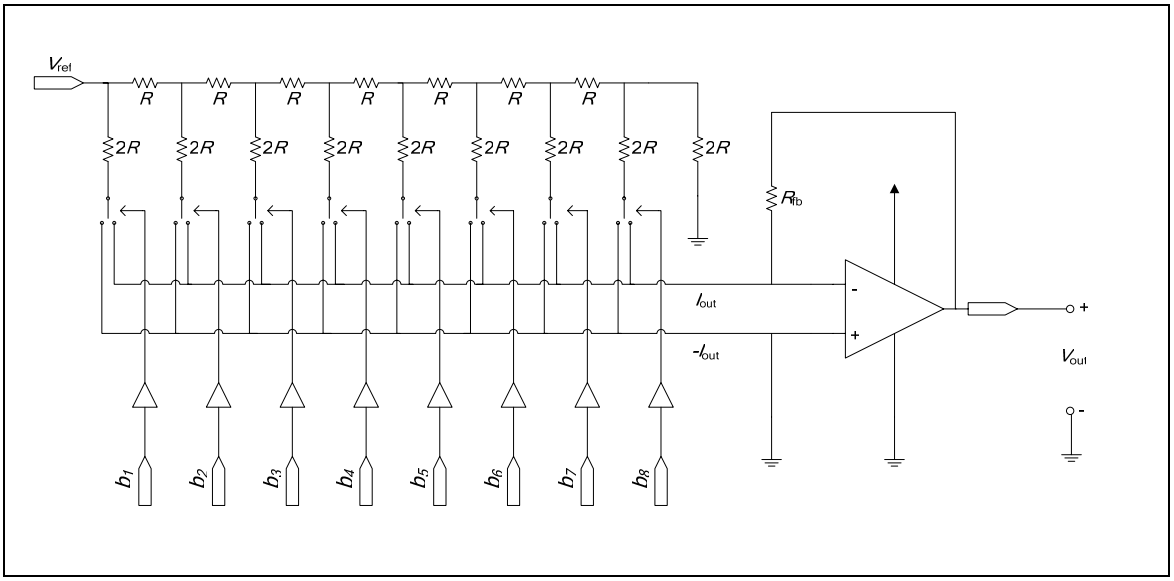


Figure 3.1: Simplified circuit diagram of the 8-bit CMOS D/A converter.

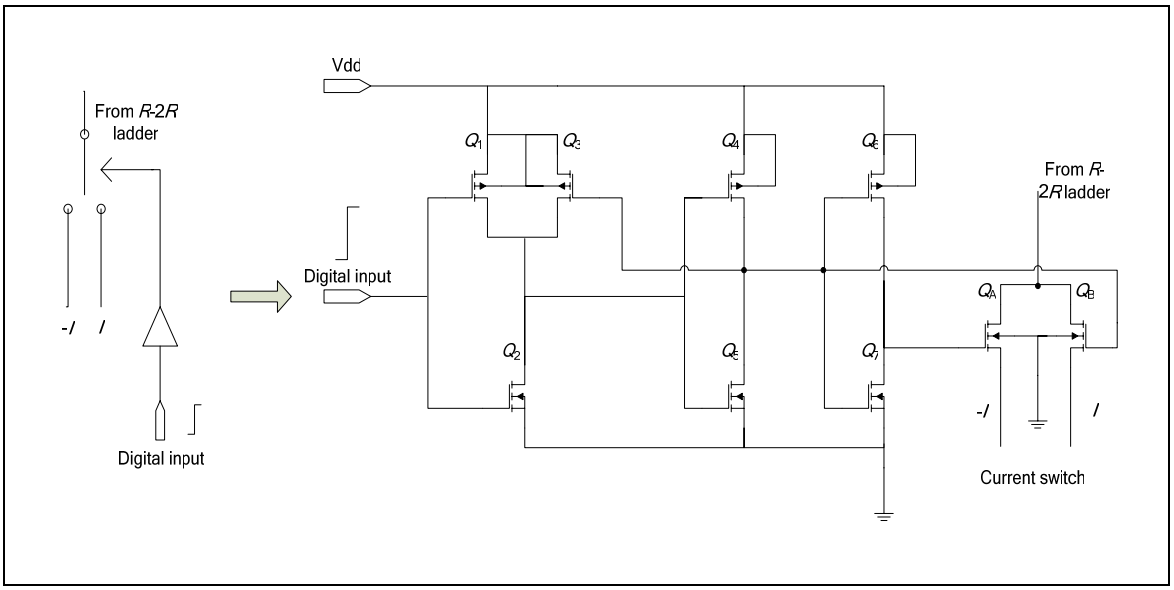


Figure 3.2: Circuit schematic of CMOS drivers and current switches in the D/A converter.

CHAPTER 4

THE CMOS BANDGAP REFERENCE

4.1 Introduction

Voltage reference is one of the important analog building blocks, especially in data acquisition systems. Ideally, this block will supply a fixed dc voltage of known amplitude that does not change with temperature.

4.2 The Bandgap Reference Circuit And Operation

The bandgap voltage reference circuit is to supply a constant voltage to the DAC. The circuit used in this project, shown in Figure 4.1, is adapted from (Hironori Banba et al., 1999). A similar architecture of this bandgap reference circuit also reported in (T. Ytterdal, 2003; Ilkka Nissinen et al., 2004; Adil Aldokhaiel, 2004, Andrea Boni, 2002).

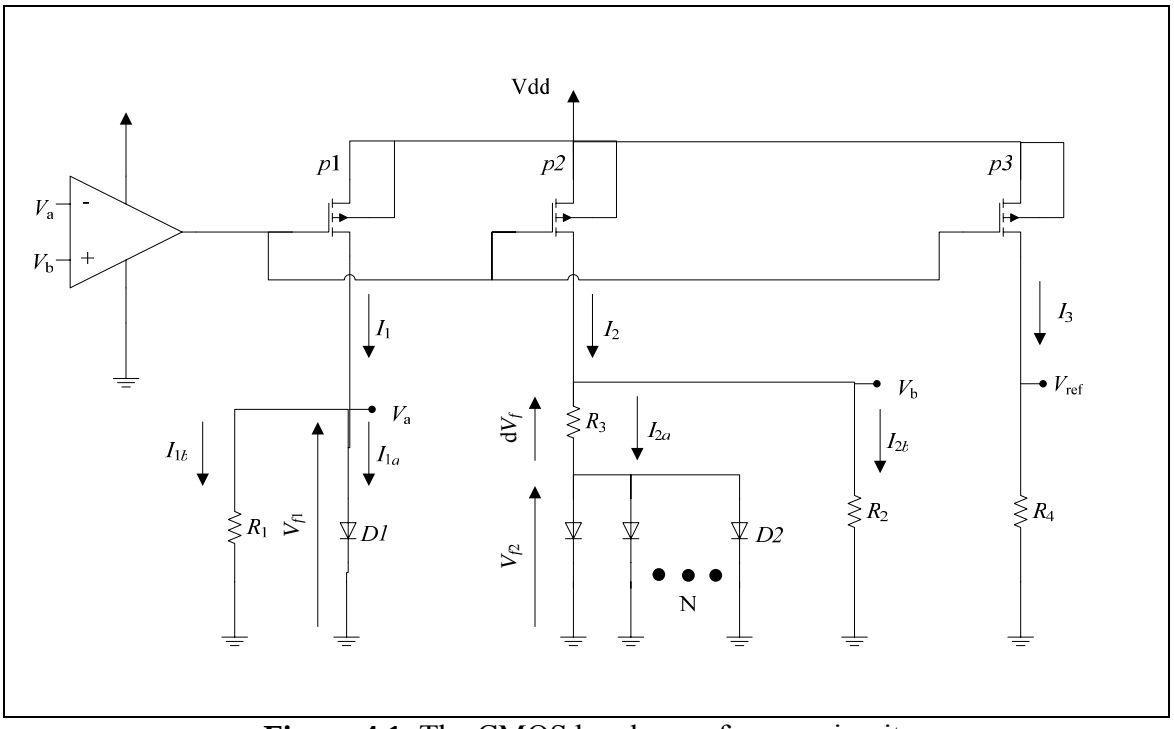


Figure 4.1: The CMOS bandgap reference circuit.

As shown in Figure 4.1, the bandgap reference circuit is composed of a CMOS op-amp, diodes and resistors. It is essential that the bandgap reference circuit be

designed without bipolar transistors. A general diode current versus voltage relation is expressed as

$$I = I_S(e^{V_f/V_T} - 1) \tag{4.1}$$

where the voltage V_T is a constant called the thermal voltage, given by

$$V_T = \frac{kT}{q} \tag{4.2}$$

For appreciable current I in the forward direction, specially for $I>>I_S$, Eq. 4.1 can be approximated by the exponential relationship

$$I = I_S e^{V_f/V_T} \tag{4.3}$$

This relationship can be expressed alternatively in the logarithmic form

$$V_f = V_T \ln\frac{I}{I_S} \tag{4.4}$$

where k is Boltzmann's constant (1.380658×10^{-23} J/K) and q is electronic charge (1.6022×10^{-19} C).

In the circuit, a pair of input voltages for the op-amp, V_a and V_b, are controlled to be the same voltage. dV_f is the forward voltage difference between one diode *D1* and N diodes *D2*.

The concept of the bandgap reference is that two currents, which are proportional to V_f and V_T, are generated by only one feedback loop. The PMOS transistor dimensions of $p1$, $p2$ and $p3$ are the same, and the resistance of R_1 and R_2 is the same

$$R_1 = R_2 \tag{4.5}$$

The op-amp is so controlled that the voltages of V_a and V_b are equalized

$$V_a = V_b \tag{4.6}$$

Therefore, the gates of $p1$, $p2$ and $p3$ are connected to a common node so that the current I_1, I_2 and I_3 becomes the same value due to the current mirror

$$I_1 = I_2 = I_3 \tag{4.7}$$

In this case,

$$I_{1a} = I_{2a} \text{ and } I_{1b} = I_{2b} \tag{4.8}$$

$$dV_f = V_{f1} - V_{f2} = V_T \ln (N) \tag{4.9}$$

I_{2a} is proportional to V_T

$$I_{2a} = \frac{dV_f}{R_3} \tag{4.10}$$

I_{2a} is proportional to V_{f1}

$$I_{2b} = \frac{V_{f1}}{R_2} \tag{4.11}$$

Here, I_2 is the sum of I_{2a} and I_{2b}, and I_2 is mirrored to I_3

$$I_3 = I_2 = I_{2a} + I_{2b} \tag{4.12}$$

Therefore, the output voltage of the bandgap reference circuit, V_{ref}, becomes

$$V_{ref} = R_4 \left(\frac{V_{f1}}{R_2} + \frac{dV_{f1}}{R_3} \right) \tag{4.13}$$

4.3 Diode Model

A key element in a bandgap circuit is the diode. In this work a PMOS diode connected elements have been used. The drain, gate and source of the PMOS tied together to form the Anode and the body of the PMOS forms the Cathode. Figure shows the PMOS diode used in the design (Adil Aldokhaiel, 2004).

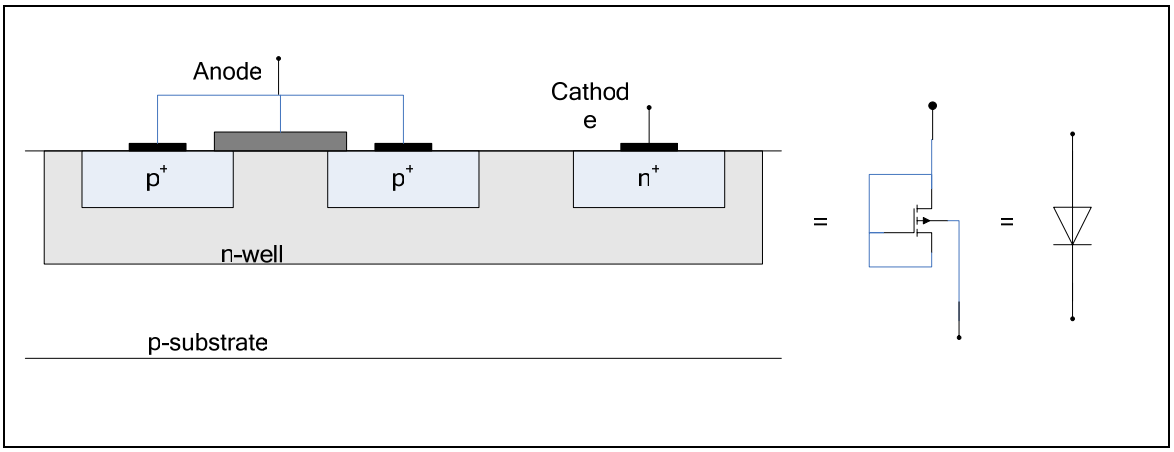


Figure 4.2: Forming a diode in a PMOS transistor.

The PMOS diode has been simulated, and the results show:

- Exponential relationship of current to the voltage across holds.
- PMOS diode exhibits a negative temperature coefficient similar to regular diodes.
- The number of parallel components N affects the cut-in voltage.

4.4 The Op-Amp For The Bandgap Reference Circuit

The op-amp use in the bandgap reference circuit is an two stage CMOS op-amp which adapted from (David Johns et al., 1997). The two-stage circuit architecture is traditionally the most popular approach for both bipolar and CMOS op-amps, where a complementary process that has reasonable n-type and p-type devices is available. "Two-stage" refers to the number of' gain stages in the op-amp. Refer to Figure 4.3, the first gain stage is a differential-input single ended output stage. The p-channel differential input pair is actively loaded with the n-channel current mirror formed by Q_3 and Q_4. The second stage consists Of Q_7, which is a common-source amplifier actively loaded with the current-source transistor Q_6.

The gain of each gain stage is given by:

$$A_{v1} = -g_{m1}\left(r_{ds2} \,||\, r_{ds4}\right) \tag{4.14}$$

$$A_{v2} = -g_{m7}\left(r_{ds6} \,||\, r_{ds7}\right) \tag{4.15}$$

The third stage is a common-drain buffer stage. This stage is often called a source follower, because the source voltage follows the gate voltage of Q_8, except for a level shift.

When an n-well process is used, the gain of the buffer stage is given by:

$$A_{v3} = \frac{g_{m8}}{G_L + g_{m8} + g_{s8} + g_{ds8} + g_{ds9}} \tag{4.16}$$

where G_L is the load conductance being driven by the buffer stage, g_s is the body-effect conductance and is given by

$$g_s = \frac{g_m \gamma}{2\sqrt{V_{SB} + 2\phi_F}} \tag{4.17}$$

Voltage V_{SB} is the source-to-substrate (or bulk) voltage, γ is the body-effect constant, and $2\phi_F$ is twice the difference between the Fermi levels in the bulk.

A simple equation can be used to find the approximate unity-gain frequency:

$$\omega_{ta} = \frac{g_{m1}}{C_c} \tag{4.18}$$

The slew rate is the maximum rate at which the output changes when input signals are large.

$$SR \equiv \left.\frac{dV_{out}}{dt}\right|_{\max} = \frac{I_{C_c}\big|_{\max}}{C_c} = \frac{I_{D5}}{C_c} \tag{4.19}$$

where we used the charge equation

$$q = CV \tag{4.20}$$

which leads to

$$I = \mathrm{d}q/\mathrm{d}t = C(\mathrm{d}V/\mathrm{d}t) \tag{4.21}$$

Since

$$I_{\mathrm{D5}} = 2I_{\mathrm{D1}} \tag{4.22}$$