DESIGN OF A 200WATTS, 12VOLTS OUTPUT VOLTAGE BUCK-BOOST DC-DC CONVERTER FOR PHOTOVALTAIC APPLICATION

Oleh

Lau Phooi San

Disertasi ini dikemukakan kepada
UNIVERSITI SAINS MALAYSIA

Sebagai memenuhi sebahagian daripada syarat keperluan
untuk ijazah dengan kepujian

SARJANA MUDA KEJURUTERAAN (KEJURUTERAAN ELEKTRIK)

Pusat Pengajian Kejuruteraan
Elektrik dan Elektronik
Universiti Sains Malaysia

Mac 2005

ABSTRACT

Solar energy becomes a very important source of power energy as the other power sources especially petroleum is decreasing. This brings to development of photovoltaic applications. To widen the usage of photovoltaic application, buck-boost converter is an important device to stabilize performance of photovoltaic application that is depends on intensity of the sunshine. A buck-boost converter with 200W and 12V DC output voltage has been designed in this project to help in mentioned problem. This project included design of buck-boost converter, simulation of the circuit and building of hardware. SG 3524 is selected as the SMPS controller for the buck-boost converter. To generate square-wave from SG 3524, simple control circuit had to be designed and connected to the chip. Two types of switch, which are MOSFET and BJT, have been used to decide the most suitable configuration to drive a buck-boost converter. From experiments, PNP BJT is chosen as switch and drives the converter successfully. The output meets expected 12V DC output from varying input between 6V and 20V. Efficiency of this converter is varying between 91% and 47% depends on the varying input voltage. With this buck-boost converter, the input voltage can be stabilized at level 12V by controlled of duty cycle of switching waveform.

ACKNOWLEDGEMENTS

I would like to take a chance here to thank especially to my supervisor, Dr. Ir. Syafrudin Masri who had leads me, instructs and guides me during I worked for this project. Thanks for his trust to allow me completed my project under his supervision. His patient encouragement gave me confidence to continue every time I faced with problems. Not forgotten help from Mr. Shauki and Mr. Nasir, technician and assistant who work in Power Laboratory, Universiti Sains Malaysia. They helped me a lot when I did experiments in lab. Meanwhile, I want to express thanks to Mr. Naim in Electronics Laboratory. He always gave his hand to me went I met problems about components. Acknowledgements also drive to all technicians and master students in School of Electrical and Electronics, Universiti Sains Malaysia, who had helped me in lab, gave me advice and shared their experiences with me. Their kindness will be remembered. Lastly, I want to thank to my family and friend for their patience, wisdom, tolerance and support.

I am grateful to all people who shared of their time, information and talent to help make this project success. Without them, I will never complete this project.

TABLE OF CONTENTS

APPENDIX C: PICTURES

LIST OF FIGURES

ABSTRACT

Solar energy becomes a very important source of power energy as the other power sources especially petroleum is decreasing. This brings to development of photovoltaic applications. To widen the usage of photovoltaic application, buck-boost converter is an important device to stabilize performance of photovoltaic application that is depends on intensity of the sunshine. A buck-boost converter with 200W and 12V DC output voltage has been designed in this project to help in mentioned problem. This project included design of buck-boost converter, simulation of the circuit and building of hardware. SG 3524 is selected as the SMPS controller for the buck-boost converter. To generate square-wave from SG 3524, simple control circuit had to be designed and connected to the chip. Two types of switch, which are MOSFET and BJT, have been used to decide the most suitable configuration to drive a buck-boost converter. From experiments, PNP BJT is chosen as switch and drives the converter successfully. The output meets expected 12V DC output from varying input between 6V and 20V. Efficiency of this converter is varying between 91% and 47% depends on the varying input voltage. With this buck-boost converter, the input voltage can be stabilized at level 12V by controlled of duty cycle of switching waveform.

Title: Design of a 200Watts, 12Volts Output Voltage Buck-Boost DC-DC Converter for Photovoltaic

Name: Lau Phooi San

Matrix No.: 66176

ABSTRAK

Tenaga solar menjadi salah satu sumber tenaga elektrik yang penting kerana sumber tenaga lagi terutamanya petroleum semakin berkurangan. Keadaan ini telah membuka jalan bagi pembangunan penggunaan fotovolta. Untuk meluaskan penggunaan fotovolta, penukar turn-naik adalah satu peranti yang penting untuk menstabilkan pretasi penggunaan fotovolta yang bergantung kepada keamatan cahaya matahari. Satu penukar turun-naik dengan keluaran 200W and 12V DC telah direkabentuk dalam projek ini untuk menyelesaikan masalah yang telah disebutkan. Projek ini termasuk rekabentuk penukar turun-naik, simulasi litar dan membina perkakasan yang telah direka. SG 3524 telah dipilih sebagai pengawal SMPS bagi penukar turn-naik. Untuk menjanakan gelombang segi empat daripada SG 3524, litar pengawal yang mudah telah direkabentuk dan disambung ke racik. Dua jenis suis, iaitu MOSFET dan BJT, telah diguanakan untuk menentukan konfigurasi yang paling sesuai untuk memacu penukar turun-naik. Daripada uji-kaji, PNP BJT telah dipilih sebagai suis dan berjaya memacu penukar. Keluaran menemui 12V DC yang dijangka daripada masukan yang bertukar dari 6V ke 20V. Kecekapan bagi penukar ini pula berubah di antara 91% dan 47%, bergantung kepada masukan yang berubah-ubah. Dengan penukar turun-naik ini, voltan keluaran boleh distabilkan pada aras 12V dengan mengawal kitar tugas gelombang pensuisan.

CHAPTER 1

INTRODUCTION

1.1 Background

Nowadays, solar energy becomes a more and more important source of power energy as the other power sources especially petroleum is decreasing.

However, the usage of photovoltaic products is limited. This is because the photovoltaic generator is a special source of finite energy with non-linear current-voltage characteristics. The induced power is varying with the intensity of sunshine. Thus, performance of linear electrical circuits and system supplied by conventional source must be re-valuated when a PV generator is using as energy source. This problem is limited the usage and the development of the solar energy. Thus, a dc-dc buck-boost converter with constant output is important to help in widen the usage of solar system or photovoltaic products.

The dc-dc converters are widely used in regulated switch-mode dc power supplies and in dc motor drive applications. Switch-mode dc-to-dc converters are used to convert the unregulated dc input to a controlled dc output at a desired voltage level. The buck-boost converters can be used to regulated dc power supplies, where can step up or step down the input to a desired output level. The power transistor is chosen as the switching device to control the output voltage for the photovoltaic applications because of high switching frequency is needed for constant operation of buck-boost converter.

Actually, the converter for use in photovoltaic application is available in the market. But most of them is using step up topology that is buck converter. Some of buck-boost converters in market are having lower range of input and output voltage. For example, LTC 3441 is having input range of 2.4V to 5.5V and output range of 2.4V and 5.25V.

Therefore, the goal of this project is to design a buck-boost converter for photovoltaic application with 12V constant output and the input range is 6V up to 20V.

1.2 Objectives

Objective of this project is to design a DC-DC buck-boost converter for photovoltaic application with rating of 200Watts and 12Volts constant output. The input voltage is varying between 6Volts to 20Volts. This converter is using power transistor as the switch to control the level of output voltage. The switching frequency for the switch is 100 kHz.

1.3 Scope of Study

Buck-boost topology from the dc-dc converter family has been built. To operate the buck-boost converter and giving a desiring output as designed, switching method and driving method of the power switch are the most important issues. The scope of this project is to design a buck-boost converter, running simulation and build up hardware of converter.

In this dissertation, Chapter 1 consists of introduction, objectives of the project, scope of study and methodology. Chapter 2 will discuss about operation of the buck-boost converter. Then, power switches and control of the converter will be discussed in Chapter 3. Chapter 4 is all about the design of the buck-boost converter that the hardware will be built up. After that, Chapter 5 will discuss the results of the project. Finally, Chapter 6 is the conclusion and suggestion of the project.

1.4 Methodology

After understood the title, information and knowledge about this project was gathered from various sources, such as internet, reference books and journal IEEE. Then, all the theories and circuits of the buck-boost converter are studied to get a clear picture of design.

With knowledge of dc-dc buck-boost converter that gained through study, the buck-boost converter circuit that will going to build up for this project was designed. Then, the circuit that has been designed is stimulated by PSIM. Simulation of the circuit should give the desired output. Or else, circuit will be studied again and the design will be improved. Process of study and correction will be repeated until simulation gives the correct output. The next step was list out components that needed then order the components through the school.

When components were received, the buck-boost converter was built and was tested it in power laboratory. If failed to get the expected result during the testing, circuit and connection was studied and did necessary corrections. Different experiments were run to get optimum output. Study and testing were repeated until the objectives of this project ware reached.

Dissertation was written to report every details in this project and the draft of dissertation was submitted along the built up buck-boost converter hardware. Finally, the viva will be attended to present this project.

All the steps to reach the objective of this project are clearly shown in flow chart below:

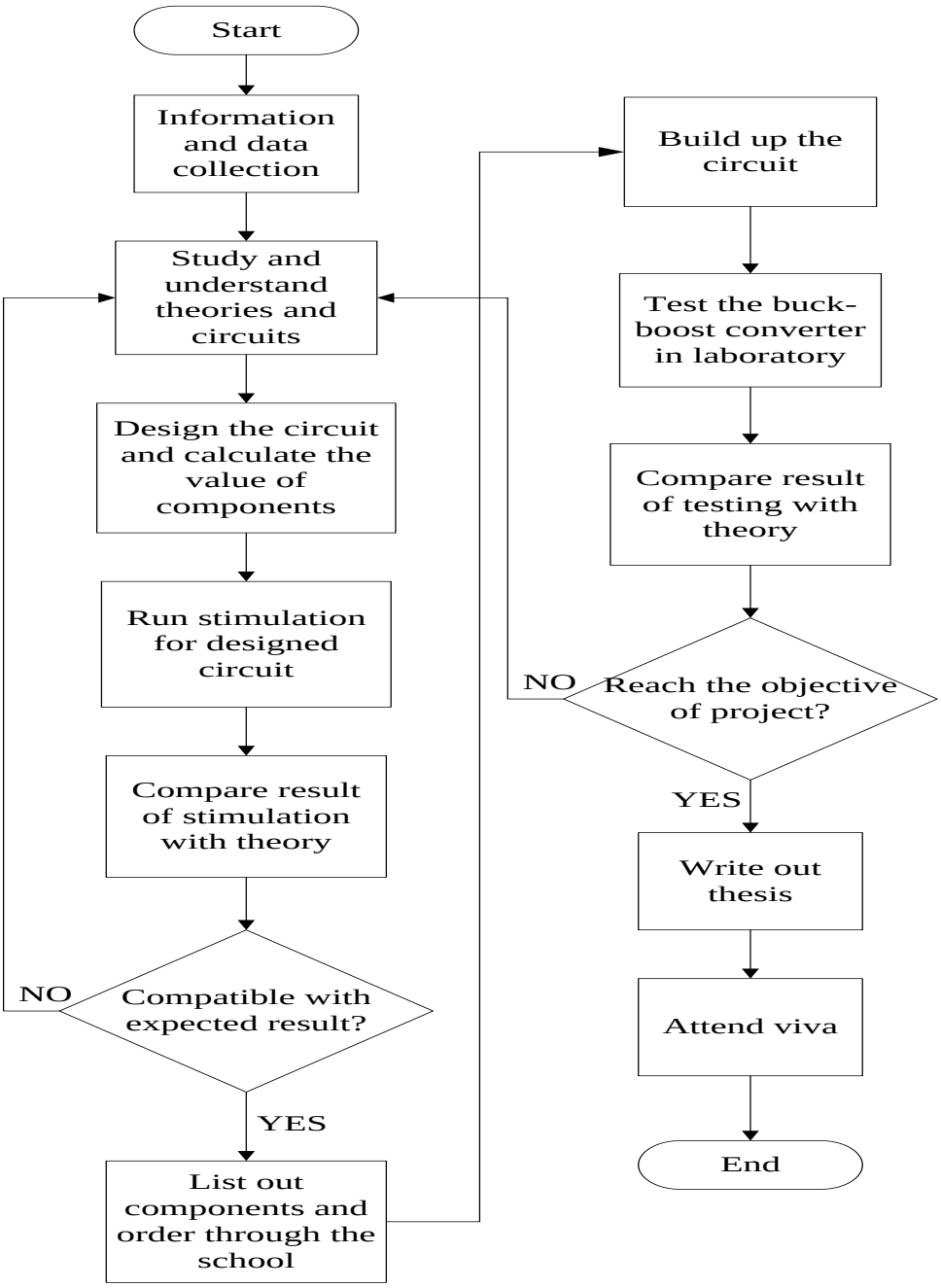


Figure 1.1: Flow chart of the steps to reach the objective of project

CHAPTER 2

DC-DC BUCK-BOOST CONVERTER

2.1 Introduction

The three basic switching power supply topologies in common use are the buck, boost, and buck-boost. The input and output of these topologies are sharing a common ground. Thus, these topologies are non-isolated.

These three topologies are differed by connection of the switches, output inductor, and output capacitor. Each topology has different properties. These properties include the steady-state voltage conversion ratios, the nature of the input and output currents, and the character of the output voltage ripple. Another important property is the frequency response of the duty-cycle-to-output-voltage transfer function. (Texas Instruments, March 1999)

The buck-boost is a popular non-isolated, inverting power stage topology. This topology normally is chosen because of the output voltage of the buck-boost converter is inverted from the input voltage, and the output voltage can be either higher or lower than the input voltage. The topology gets its name from producing an output voltage that can be higher (like a boost power stage) or lower (like a buck power stage) in magnitude than the input voltage. However, the output voltage polarity is opposite with the input voltage polarity. The input current for a buck-boost power stage is discontinuous or pulsating due to the power switch (Q1) current that pulses from zero to I_L every switching cycle. The output current for a buck-boost power stage is also discontinuous or pulsating. This is because the output diode only conducts during a portion of the switching cycle. The output capacitor supplies the entire load current for the rest of the switching cycle. (Ned Mohan, Tore Undeland, William Robbins, 1998)

Figure 2.1 shows a simplified schematic of the buck-boost converter with a drive circuit block included. The power switch, Q1, is an n-channel MOSFET. The output diode is CR1. The inductor, L, and capacitor, C, is the effective output filter. The resistor, R, represents the load seen by the power stage output.

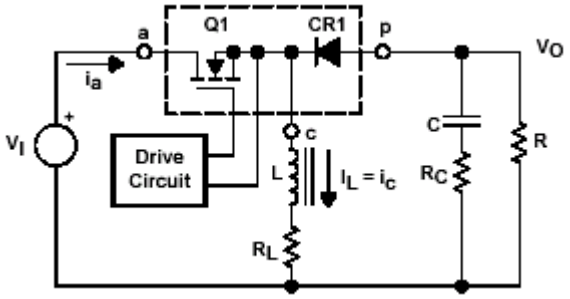


Figure 2.1: Buck-boost converter schematic

During normal operation of the buck-boost power stage, Q1 is repeatedly switched on and off with on pulse of off pulse generating by drive circuit. This switching action gives rise to a train of pulses at the junction of Q1, CR1, and L. The inductor, L, is connected to the output capacitor, C; only when CR1 conducts. L acts as source and delivers power to output load. Capacitor is acting as effective output filter. It filters the train of pulses to produce a DC output voltage.

2.2 Continuous Conduction Mode Analysis

In continuous conduction mode, the buck-boost converter assumes two states per switching cycle. The ON State is when Q1 is ON and CR1 is OFF. The OFF State is when Q1 is OFF and CR1 is ON. A simple linear circuit can represent each of the two states where the switches in the circuit are replaced by their equivalent circuit during each state. The circuit diagram for each of the two states is shown in Figure 2.2.

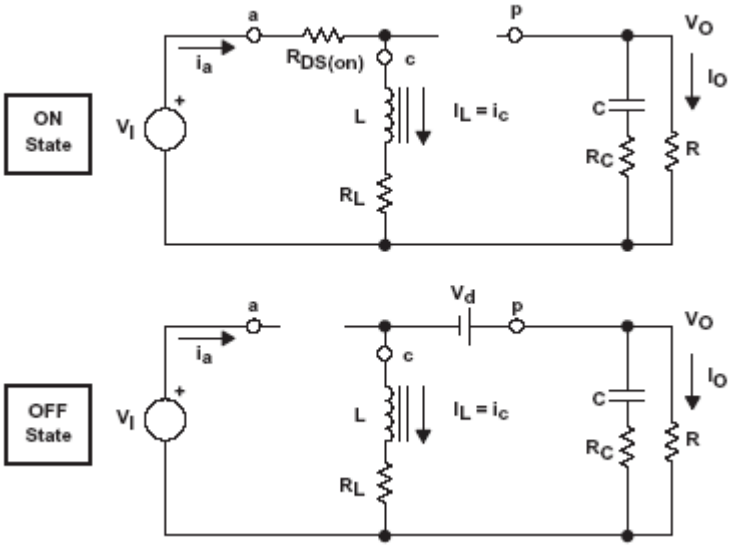


Figure 2.2: ON State and OFF State of continuous conduction mode

The duration of the ON state is $D \times T_s = T_{ON}$ where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, Ts. The duration of the OFF state is called T_{OFF}. Since there are only two states per switching cycle for continuous conduction mode, T_{OFF} is equal to $(1–D) \times T_S$. The quantity (1–D) is sometimes called D'. These times are shown along with the waveforms in Figure 2.2.

Referring to Figure 2.2, during the ON state, Q1 presents a low resistance, $R_{DS}(on)$, from its drain to source and exhibits a small voltage drop of $V_{DS}=I_L \times R_{DS}(on)$. There is also a small voltage drop across the dc resistance of the inductor equal to $I_L \times R_L$. Thus, the input voltage, V_I, minus losses, $(V_{DS} + I_L \times R_L)$, is applied across the inductor, L. CR1 is OFF during this time because it is reverse biased. The inductor current, I_L, flows from the input source, V_I, through Q1 and to ground. During the ON state, the voltage applied across the inductor is constant and equal to $V_I – V_{DS} – I_L \times R_L$. Polarity convention is assuming for the inductor current as shown in Figure 2.2, the inductor current increases as a result of the applied voltage. Also, since the applied voltage is essentially constant, the inductor current increases linearly.

This increase in inductor current during T_{ON} is shown in Figure 2.3.

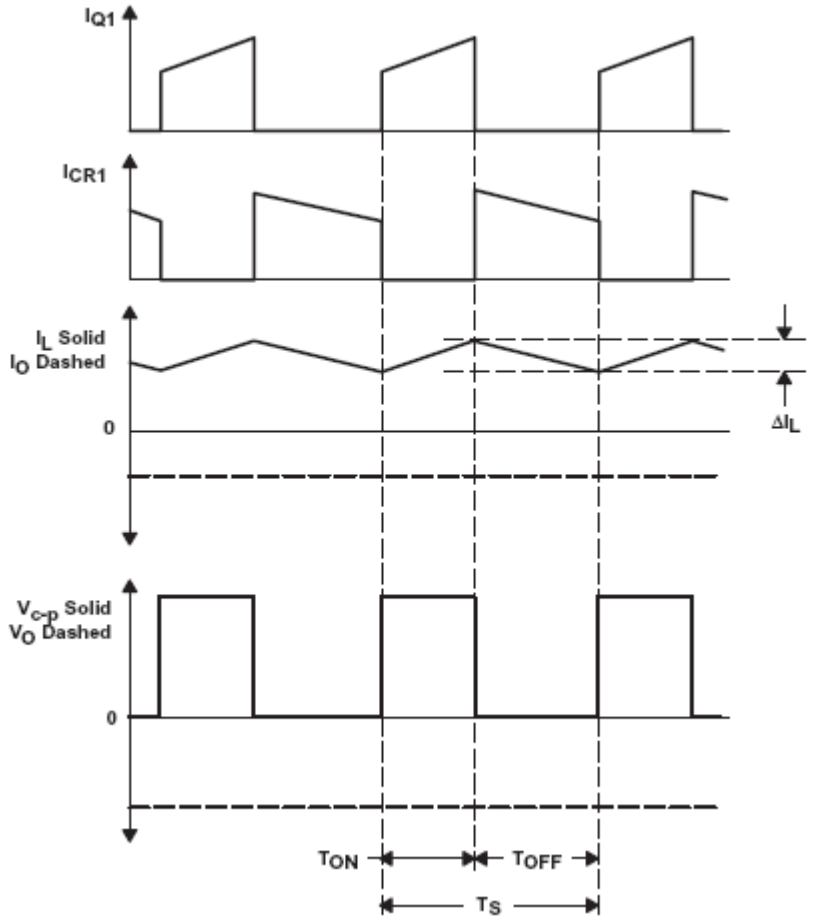


Figure 2.3: Continuous mode waveforms of buck-boost converter

The amount that the inductor current increases can be calculated by using formula:

$$V_L = L \times \frac{di_L}{dt}$$

$$\Delta I_L = \frac{v_L}{L} \times \Delta T \quad \text{……..……..} \quad (2.1)$$

Where V_L,v_L = inductor voltage

L = inductance

ΔI_L = inductor ripple current

ΔT = period for inductor ripple current

The inductor current increase during the ON state is given by:

$$\Delta I_L(+) = \frac{V_I - (V_{DS} + I_L \times R_L)}{L} \times T_{ON} \quad \text{……..…} \quad (2.2)$$

Where $\Delta I_L(+)$ = inductor current increase during the ON state

V_I = input voltage

V_{DS} = drain-source voltage

I_L = inductor current

R_L = dc resistance of the inductor

L = inductance

T_{ON} = period of ON state

ΔI_L is referred to the inductor ripple current. During this period, all the output current is supplied by the output capacitor.

Referring to Figure 2.2, when Q1 is OFF, it presents high impedance from its drain to source. Therefore, since the current flowing in the inductor L cannot change instantaneously, the current shifts from Q1 to CR1. Due to the decreasing inductor current, the voltage across the inductor reverses polarity until rectifier CR1 becomes forward biased and turns ON. The voltage applied across L becomes ($V_O - V_d - I_L \times R_L$) where the quantity, V_d, is the forward voltage drop of CR1.

The inductor current, I_L, now flows from the output capacitor and load resistor combination through CR1 and to ground. Notice that the orientation of CR1 and the direction of current flow in the inductor means that the current flowing in the output capacitor and load resistor combination causes V_O to be a negative voltage. During the OFF state, the voltage applied across the inductor is constant and equal to ($V_O - V_d - I_L \times R_L$). Maintaining same polarity convention, this applied voltage is negative (or opposite in polarity from the applied voltage during the ON time), because the output voltage V_O is negative. Hence, the inductor current decreases during the OFF time. Also, since the applied voltage is essentially constant, the inductor current decreases linearly. This decrease in inductor current during T_{OFF} is illustrated in Figure 2.3.

The inductor current decrease during the OFF state is given by:

$$\Delta I_L(-) = \frac{-(V_O - V_d - I_L \times R_L)}{L} \times T_{OFF} \quad \text{...} \quad (2.3)$$

Where $\Delta I_L(-)$ = inductor current decrease during the OFF state

V_o = output voltage

V_d = voltage across diode

T_{OFF} = period of OFF state

In steady state conditions, the current increase (ΔI_L (+)) during the ON time and the current decrease during the OFF time (ΔI_L (–)) must be equal. Otherwise, the inductor current would have a net increase or decrease from cycle to cycle which would not be a steady state condition. Therefore, these two equations can be equated and solved for V_O to obtain the continuous conduction mode buck-boost voltage conversion relationship:

Solving for V_O by equating (2.2) and (2.3):

$$V_O = -\left[(V_I - V_{DS}) \times \frac{T_{ON}}{T_{OFF}} - V_d - I_L \times R_L \times \frac{T_{ON} + T_{OFF}}{T_{OFF}}\right] \quad \text{.............................} \quad (2.4)$$

Substituting $T_S = T_{ON} + T_{OFF,}$ $D = T_{ON}/ T_S$ and $(1\text{-}D) = T_{OFF} / T_S$, the steady-state equation for V_O is:

$$V_O = -\left[(V_I - V_{DS}) \times \frac{D}{1-D} - V_d - \frac{I_L \times R_L}{1-D}\right] \quad \text{..} \quad (2.5)$$

$T_{ON} + T_{OFF}$ is assumed to be equal to T_S. This is true only for continuous conduction mode.

In the above equations for $\Delta I_L(+)$ and $\Delta I_L(–)$, the output voltage was implicitly assumed to be constant with no AC ripple voltage during the ON time and the OFF time. This is a common simplification and involves two separate effects.

First, the output capacitor is assumed to be large enough that its voltage change is negligible. Second, the voltage due to the capacitor ESR is also assumed to be

negligible. These assumptions are valid because the AC ripple voltage is designed to be much less than the DC part of the output voltage. The above voltage conversion relationship for V_O illustrates the fact that V_O can be adjusted by adjusting the duty cycle, D. This relationship approaches zero as D approaches zero and increases without bound as D approaches unity. A common simplification is to assume V_{DS}, V_d, and R_L are small enough to ignore. Setting V_{DS}, V_d, and R_L to zero, the above equation simplifies considerably to:

$$V_O = -V_I \times \frac{D}{1-D} \quad \text{..... (2.6)}$$

Where Vo = output voltage

V_I = input voltage

D = Duty Cycle = $\frac{T_{ON}}{T_{ON} + T_{OFF}}$

A simplified, qualitative way to visualize the circuit operation is to consider the inductor as an energy storage element. When Q1 is on, energy is added to the inductor. When Q1 is off, the inductor delivers some of its energy to the output capacitor and load. The output voltage is controlled by setting the on-time of Q1.

By increasing the on-time of Q1, the amount of energy delivered to the inductor is increased. More energy is then delivered to the output during the off-time of Q1 resulting in an increase in the output voltage.

The average of the inductor current is not equal to the output current. To relate the inductor current to the output current, referring to Figures 2.2 and 2.3, note that the inductor delivers current to the output only during the off state of the power stage. This current averaged over a complete switching cycle is equal to the output current because the average current in the output capacitor must be equal to zero.

The relationship between the average inductor current and the output current for the continuous mode buck-boost power stage is given by:

$$I_{L(avg)} \times \frac{T_{OFF}}{T_S} = I_{L(avg)} \times (1-D) = -I_O \quad \text{..... (2.7)}$$

Or

$$I_{L(avg)} = \frac{-I_O}{1-D} \quad \text{..... (2.8)}$$

Where $I_{L(avg)}$ = average inductor current

$T_S = T_{On} + T_{OFF}$

I_O = output current

2.3 Discontinuous Conduction Mode Analysis

If the output current decreases, the inductor current will also be decreased. If the output load current is reduced below the critical current level, the inductor current will be zero for a portion of the switching cycle. This should be evident from the waveforms shown in Figure 2.3, since the peak to peak amplitude of the ripple current does not change with output load current. In a buck-boost converter, if the inductor current attempts to fall below zero, it just stops at zero (due to the unidirectional current flow in CR1) and remains there until the beginning of the next switching cycle. This operating mode is called discontinuous conduction mode. A power stage operating in discontinuous conduction mode has three unique states during each switching cycle as opposed to two states for continuous conduction mode. The inductor current condition where the power stage is at the boundary between continuous and discontinuous mode is shown in Figure 2.4. This is where the inductor current just falls to zero and the next switching cycle begins immediately after the current reaches zero.

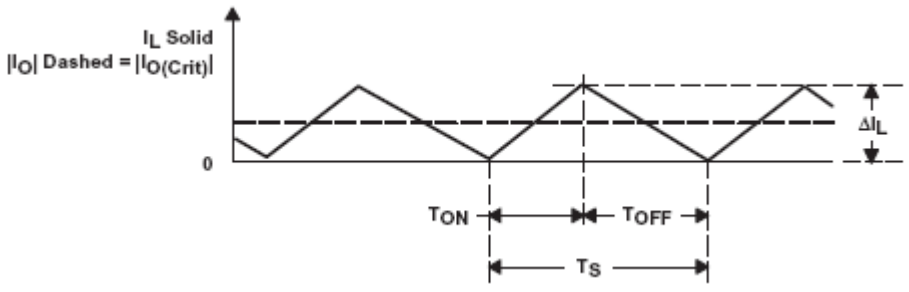


Figure 2.4: Boundary between continuous and discontinuous mode

If output load current decreases continuously, the buck-boost converter will goes into discontinuous conduction mode. Discontinuous current mode is shown in Figure 2.5.

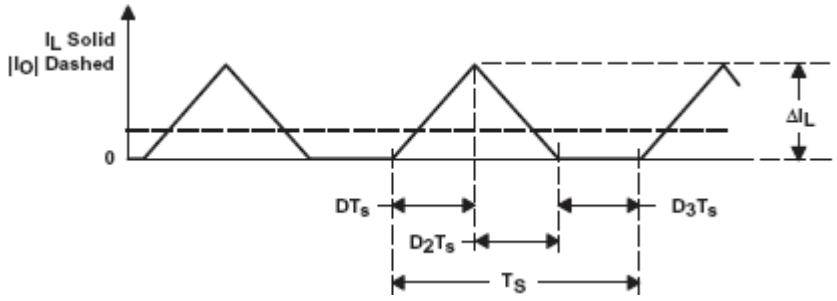


Figure 2.5: Discontinuous current mode

There are three unique states that the converter assumes during discontinuous conduction mode operation:

I. The ON state is when Q1 is ON and CR1 is OFF.
II. The OFF State is when Q1 is OFF and CR1 is ON.
III. The IDLE state is when both Q1 and CR1 are OFF.

The first two stages are identical to the cases that happen in continuous mode. Thus, circuit in Figure 2.2 is applicable. The only difference is T_{OFF} is not equal to (1-D) $\times$ T_S.

The duration of the ON state is $T_{ON} = D \times T_S$ where D is the duty cycle, set by the control circuit, expressed as a ratio of the switch ON time to the time of one complete switching cycle, Ts. The duration of the OFF state is $T_{OFF} = D_2 \times T_S$. The IDLE time is the remainder of the switching cycle and is given as $T_S - T_{ON} - T_{OFF} = D_3 \times T_S$. These times are shown with the waveforms in Figure 2.6.

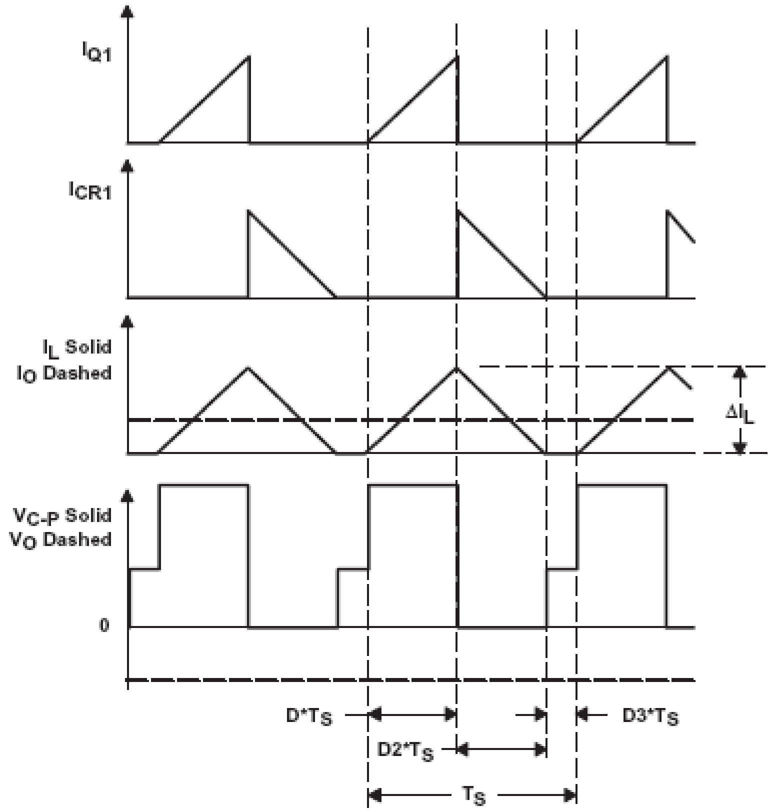


Figure 2.6: Discontinuous conduction mode buck-boost converter waveforms

The inductor current increase during the ON state is given by:

$$\Delta V_L(+) = \frac{V_I}{L} \times T_{ON} = \frac{V_I}{L} \times D \times T_S = I_{PK} \quad \text{......} \quad (2.9)$$

Where I_{PK} = Peak inductor current

The ripple current magnitude, $\Delta I_L(+)$, is equal to the peak inductor current, I_{PK}. It is because in discontinuous mode, the current starts at zero each cycle.

The inductor current decrease during the OFF state is given by:

$$\Delta V_L(-) = \frac{-V_O}{L} \times T_{OFF} = \frac{-V_O}{L} \times D_2 \times T_S \quad \text{......} \quad (2.10)$$

As in the continuous conduction mode case, the current increase, $\Delta I_L(+)$, during the ON time is equal to the current decrease during the OFF time, $\Delta I_L(-)$. Therefore,

these two equations can be equated and solved for V_O to obtain the first of two equations to be used to solve for the voltage conversion ratio:

$$V_O = -V_I \times \frac{T_{ON}}{T_{OFF}} = -V_I \times \frac{D}{D_2} \quad \text{..... (2.11)}$$

The output current (the output voltage V_O divided by the output load R) is the average over one switching cycle of the inductor current during the time when CR1 conducts ($D_2 \times T_S$).

$$\frac{V_O}{R} = I_O = \frac{1}{T_S} \times \left[\frac{-I_{PK}}{2} \times D_2 \times T_S \right] \quad \text{..... (2.12)}$$

Where R = output load

Substituting relationship for $I_{PK}(\Delta I_L(+))$ into (2.12):

$$\frac{V_O}{R} = I_O = \frac{1}{T_S} \times \left[\frac{1}{2} \times -1 \times \left(\frac{V_I}{L} \times D \times T_S \right) \times D_2 \times T_S \right] \quad \text{..... (2.13)}$$

$$\frac{V_O}{R} = \frac{-V_I \times D \times D_2 \times T_S}{2 \times L} \quad \text{..... (2.14)}$$

Solving (2.11) with (2.14):

$$V_O = -V_I \times \frac{D}{\sqrt{K}} \quad \text{..... (2.15)}$$

Where K is defined as:

$$K = \frac{2 \times L}{R \times T_S} \quad \text{..... (2.16)}$$

The above relationship shows one of the major differences between the two conduction modes. For discontinuous conduction mode, the voltage conversion relationship is a function of the input voltage, duty cycle, power stage inductance, the switching frequency, and the output load resistance. For continuous conduction mode, the voltage conversion relationship is only dependent on the input voltage and duty cycle.

In typical applications, the buck-boost power stage is operated in either continuous conduction mode or discontinuous conduction mode. For a particular application, one conduction mode is chosen and the power stage is designed to maintain the same mode. In this project, continuous current conduction mode is chosen.

CHAPTER 3

POWER SWITCHES AND CONTROL METHOD

3.1 Introduction

Power switch using in the buck-boost converter is a very important component. The capability and controlling of the power switch is a decisive factor for the operation and efficiency of the buck-boost converter. Controllable switches including BJT and MOSFET can be turned on and turned off by control signals. This switching characteristic makes controllable switches becomes the most suitable device to use in dc-dc buck-boost converter.

In this project, power MOSFET and power BJT is chosen as the switch is the buck-boost converter. P-channel and N-channel MOSFET and PNP BJT have been using in the designed hardware and the experiment has been conduct to decide the most suitable device using in design to give the optimum efficiency.

3.2 Power MOSFET

3.2.1 Introduction

Power MOSFETs (**M**etal **O**xide **S**emiconductor, **F**ield **E**ffect **T**ransistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of or reduction of the second-breakdown failure mechanism, the ability to be paralleled and stable gain and response time over a wide temperature range. (Fairchild, October 1999)

There are two type of MOSFET: depletion type and enhancement type, and each have N-channel and P–channel type. (Fairchild, November 1999)The depletion type is normally on, and operates as JFET as seen from Figure 3.1.

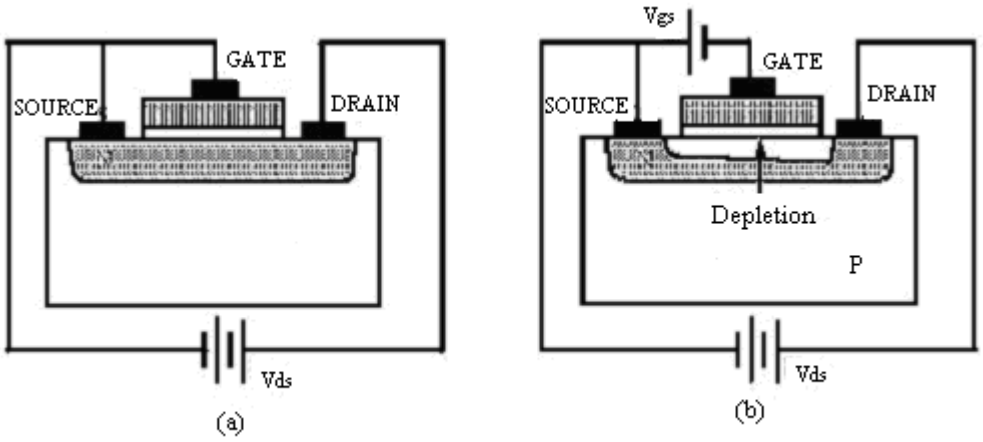


Figure 3.1: The structure of depletion type MOSFET and its operation

(a) When V_{GS} (gate-to-Drain) has not been supplied

(b) When V_{GS} (gate-to-Drain) has been supplied

The enhancement type is normally off, which means that the drain-to-source current increases as the voltage at the gate increases. And no current flows when there is no voltage supplied at the gate as shown in Figure 3.2.

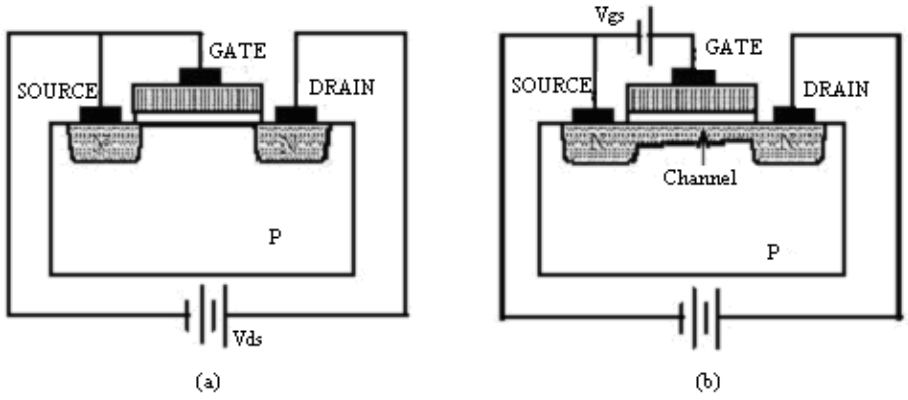


Figure 3.2: The structure of enhancement type MOSFET and its operation

(a) When V_{GS} (gate-to-Drain) has not been supplied

(b) When V_{GS} (gate-to-Drain) has been supplied

The circuit symbol for these two types of MOSFET is shown in Figure 3.3. The direction of the arrow on the lead that goes to the body region indicates the

direction of current flow if the body-source pn junction were forward biased. (Ned Mohan, Tore Undeland, William Robbins, 1998)

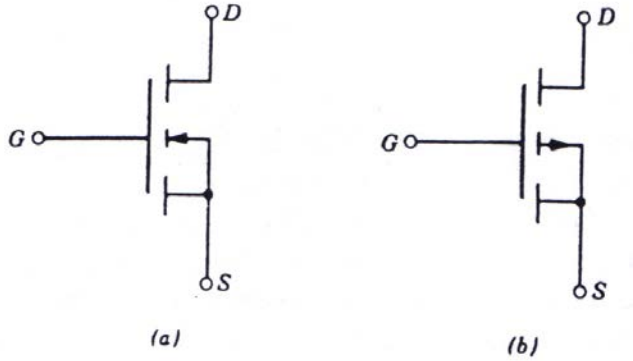


Figure 3.3: Circuit symbols for (a) n-channel and (b) p-channel MOSFET

3.2.2 I-V Characteristics of MOSFET

Power MOSFET is a voltage-driven device whose gate terminal, Figure 3.4(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an N-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Figure 3.4(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface inversion phenomenon, then, the operation of a MOSFET is entirely different from that of a bipolar transistor, which always retain its n-p-n characteristic.

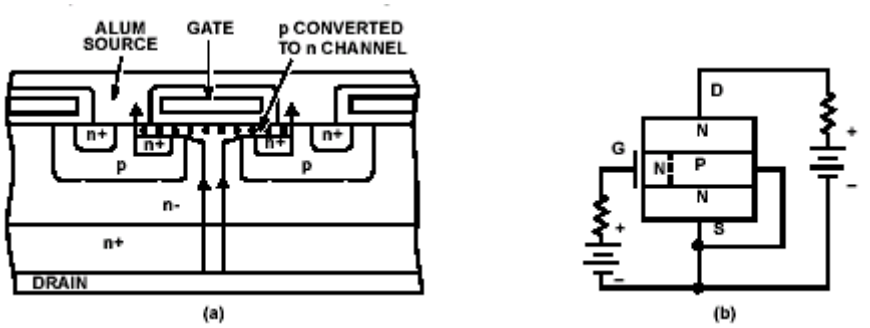


Figure 3.4: (a) Lateral N-channel MOSFET cross-section

(b)Surface-inversion phenomenon

With no electrical bias applied to the gate G, no current can flow in either direction underneath the gate because there will always be a blocking PN junction. When the gate is forward biased with respect to the source S, as shown in Figure 3.5, the free hole-carriers in the p-epitaxial layer are repelled away from the gate area creating a channel, which allows electrons to flow from the source to the drain. Note that since the holes have been repelled from the gate channel, the electrons are the "majority carriers" by default. This mode of operation is called "enhancement" but it is easier to think of enhancement mode of operation as the device being "normally off", that is, the switch blocks current until it receives a signal to turn on. The opposite is depletion mode, which is a normally "on" device. (National Semiconductor, December 1988)

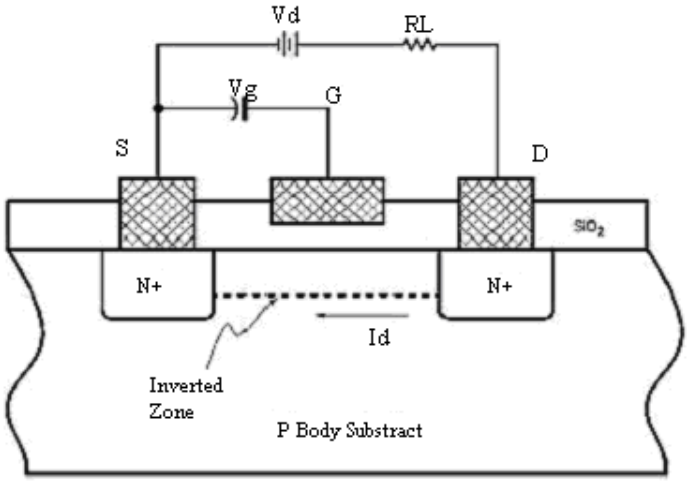


Figure 3.5: Lateral MOSFET biased for forward current

The output characteristics, drain current i_D as a function of drain-to-source voltage V_{GS} as a parameter for an n-channel MOSFET, are shown in Figure 3.6.

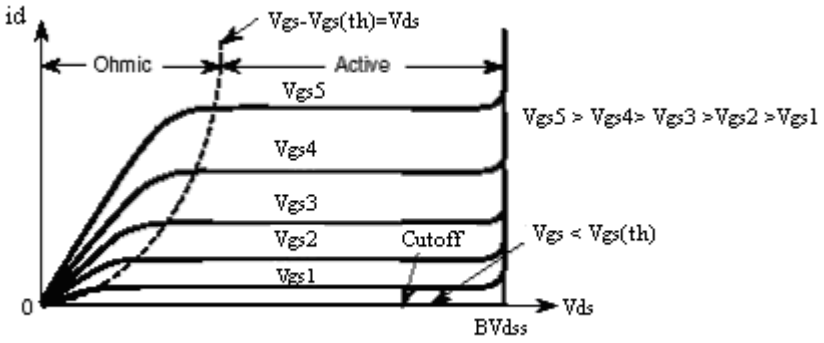


Figure 3.6: Current-voltage characteristics of an n-channel enhancement mode MOSFET (output characteristics)

It could be divided as the ohmic region, the saturation (=active) region, and the cut-off region.

- **Ohmic region**: Constant resistance region. If drain-to-source voltage is zero, the drain current also becomes zero regardless of gate–to-source voltage. This region is at the left side of $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line ($V_{GS} - V_{GS(th)} > V_{DS} > 0$), and in this region, even if the drain current is very large, the power dissipation could be maintained by minimizing the $V_{DS(on)}$.

- **Saturation region:** Constant current region. It is at the right side of $V_{GS} - V_{GS(th)} = V_{DS}$ boundary line, and in this region, the drain current differs by the gate-to-source voltage, not by the drain-to-source voltage. Here, the drain current is called saturated.
- **Cut-off region:** It is called cut-off region, when the gate-to-source voltage is lower than $V_{GS(th)}$ (threshold voltage). The device is an open circuit and must hold off the power supply voltage applied to circuit.

3.2.3 Switching Behavior of MOSFET

Power MOSFETs are well known for their ease of drive and fast switching behavior. Being majority carrier devices means they are free of the charge storage effects which inhibit the switching performance of bipolar products. How fast a Power MOSFET will switch is determined by the speed at which its internal capacitances can be charged and discharged by the drive circuit. The switching characteristics of the Power MOSFET are determined by its capacitances. These capacitances are not fixed but are a function of the relative voltages between each of the terminals. Junction capacitance is thus dependent on applied voltage with an inverse relationship.

When a small positive gate-to-source voltage is supplied to the gate electrode, the depletion region will be formed, as shown in Figure 3.7.

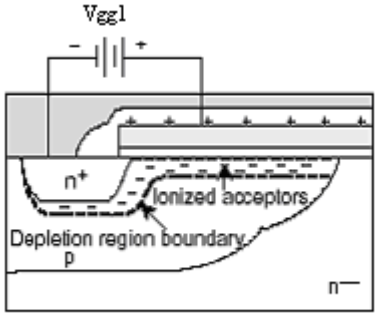
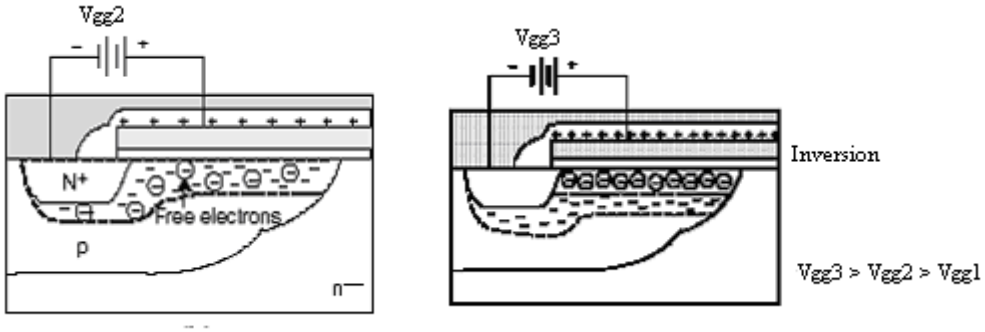


Figure 3.7: Formation of depletion region

Positive charge induced in the gate electrode; induct the same amount of negative charge at the oxide – silicon interface (P–-body region, which is underneath the

gate oxide), and here the holes are pushed into the semiconductor bulk by the electric field, and the depletion region is formed up by the acceptors charged with negative.

As the positive gate-to-source voltage increases, inversion layer will be formed, as shown in Figure 3.8. The depletion region gets wider towards the body, and it begins to drag the free electrons to the interface. These free electrons have been created by the thermal ionization. And the free holes created with the free electrons, are pushed into the semiconductor bulk. The holes that haven't been pushed into the bulk are neutralized by the electrons that have been dragged by the positive charges of the holes from the n+ source. If the supplied voltage keeps increasing, the density of the free holes of the body and the density of the free electrons of the interface becomes equal. At this point, the free electron layer is called inversion layer. And this inversion layer enables the current flow as it becomes the conductive pass (=channel) of the drain and the source of the MOSFET.



(a) (b)

Figure 3.8: Formation of the inversion layer

Drain current (I_D) changes due to the drain-to-source voltage (V_{DD}) increase. (V_{GS} is constant) In the MOSFET, when the channel has formed up and the V_{DD} is supplied, I_D starts to flow. When the V_{GS} is a constant value, and the V_{DD} is increased, the I_D also increases linearly, But shown in the graph of the MOSFET output characteristics, when the real V_{DD} goes over certain level, the increase rate of I_D decreases slowly. And eventually, it becomes a constant value independent of V_{DD}, and becomes dependent of V_{GS}.

To understand the characteristics, as shown in Figure 3.9, attention must be paid to the voltage drop at the $V_{CS(x)}$ due to the ohmic resistance when there is I_D flowing at the inverse layer. $V_{CS(x)}$ is the channel-to-source voltage from the source at the distance of x. This voltage is equal to the $V_{GS}-Vox(x)$ at each x points (Vox(x) is the gate-to-body voltage crossing the gate oxide from the source at the distance of x), and it has the maximum value, V_{DS} at x=L (the drain end of the channel). As shown in Figure 3.9(a), when the low voltage $V_{DD}=V_{DD1}$ is supplied, low $I_D(=I_{D1})$, which has almost no voltage drop of $V_{CS(x)}$, flows. So as the $Vox_{(0)}\sim Vox_{(L)}$ is constant, the thickness of the inversion layer remains in uniform. As higher V_{DD} is supplied, I_D increases, and the voltage drop of $V_{CS(x)}$ occurs, and the value of Vox(x) decreases, and these reduces the thickness of the inversion layer starting from x=L. And because of this, the resistance increases, and the graph of I_D starts to become flat, where it use to increase with the increment of the V_{DD}. When $Vox_{(L)}=V_{GS}-V_{DS}=V_{GS(th)}$, as I_D increases, the inversion layer at x=L does not disappear due to the high electric field ($J=\sigma E$) formed by the reduction of thickness, and maintains the minimum thickness. The high electric field not only maintains the minimum thickness of the inversion layer, it saturates the velocity of the charge carrier at $Vox_{(L)}=V_{GS}-V_{DS}=V_{GS(th)}$. The reverse process of the turn-on transient is turn-off transient.

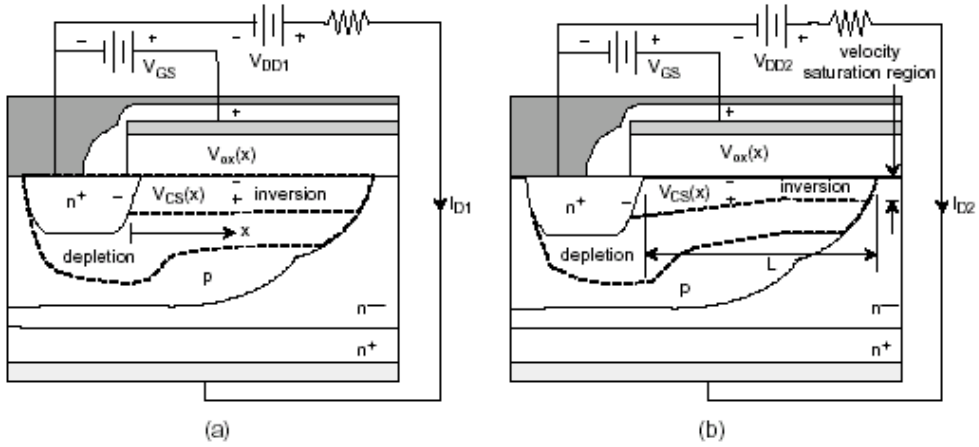


Figure 3.9: Inversion layer thickness changes due to the increase of the drain-to-source voltage (V_{DD}). Where, $V_{DD1} < V_{GS} - V_{GS(th)}$, $V_{DD2} > V_{GS} - V_{GS(th)}$, I_{D2} (saturation current) > I_{D1}