DESIGN AND TRADEOFF CHARACTERIZATIONS OF HIGH FREQUENCY BALANCED AMPLIFIER FOR RF INTEGRATED SYSTEM

Oleh

Tai Wen Qi

Disertasi ini dikemukakan kepada
UNIVERSITI SAINS MALAYSIA

Sebagai memenuhi sebahagian daripada syarat keperluan
untuk ijazah dengan kepujian

SARJANA MUDA KEJURUTERAAN (KEJURUTERAAN ELEKTRONIK)

Pusat Pengajian Kejuruteraan
Elektrik Dan Elektronik
Universiti Sains Malaysia Mac 2005

ABSTRAK

Laporan ini merangkumi rekabentuk, analisis dan implementasi penguat seimbang berfrekeunsi tinggi yang beroperasi pada 1.9 GHz. Rekabentuk sistem dan litar dijalankan dengan bantuan Agilent's Advanced Design System (ADS 2003A). Penguat seimbang adalah sejenis penguat yang menggabungkan dua penguat tunggal yang sama menjadi satu unit tunggal, di mana penguatan isyarat RF dapat dijalankan. Terdapat dua jenis penguat tunggal iaitu penguat yang menggunakan rangkaian elemen 'lumped' dan 'microstrip'. Dalam projek ini, kedua-dua jenis penguat telah direka dan dibina. Analisis dan perbandingan yang dibuat kepada dua topologi ini disertakan di dalam laporan ini. Rekacipta awalan menggunakan komponen ideal memberikan struktur asas dan litar keseluruhan penguat. Pada tahap permulaan, langkah-langkah rekabentuk termasuk pengiraan matematik dan analisis. Langkah rekabentuk terperinci yang menggantikan komponen ideal dengan model sebenar dijalankan setelah struktur litar didapati. Pelbagai jenis simulasi menggunakan ADS dijalankan untuk mendapatkan prestasi penguat seimbang. Dengan bantuan ADS, nilai dalam rekaan dioptimasikan untuk mendapatkan prestasi yang dikehendaki. Penguat seimbang diimplementasikan secara perisian dan perkakasan. Rekaan bentangan litar menggunakan fungsi Layout ADS merupakan sebahagian daripada implementasi perkakasan. Litar penguat dibina di atas papan cetakan litar (PCB). Perkakasan yang dibina diuji dengan menggunakan 'network analyzer' dan 'spectrum analyzer' untuk mendapatkan sifat dan spesifikasi litar yang dikehendaki. Bacaan daripada ujian perkakasan dibandingkan dengan keputusan simulasi. Perbezaan yang wujud dibincangkan dalam laporan ini.

ABSTRACT

This report included design, analysis and implementation of high frequency balanced amplifier operate at center frequency of 1.9 GHz. System and circuit design are carried out with the aid of a powerful design tool - Agilent's Advanced Design System (ADS 2003A). Balanced amplifier is a type of amplifier that combines 2 similar single-ended amplifiers into single unit, which can perform amplification of input RF signal. There are two common types of single-ended amplifier: amplifier with lumped element and microstrip matching network. In this project, both types of amplifier are designed and built. Analysis and comparison carried out on this two different topology are included in this report. Initial design using ideal component provided the basic structure and complete circuit of the amplifiers. In the beginning stage, the design steps included mathematical calculations and analysis. Detailed design steps with replaced actual model are carried out after the structure of circuits are obtained. Different types of simulation using ADS are done to observe performances of the balanced amplifiers. Using features of ADS, the values of design are optimized to obtain required performances. Result of simulations are included in this report. The balanced amplifier design are implemented in both software and hardware. Circuit's layout design using ADS's features is part of hardware implementations. The amplifier circuits are built on printed circuit board (PCB). The hardwares built are tested with network and spectrum analyzer in to obtain required characteristics and specifications. Measurements taken from hardware test are compared to results from simulations. Variations that existed from both results are discussed in this report.

ACKNOWLEDGEMENT

I would like to express my gratitude to many people who have made my undergraduate studies possible and made it such a rewarding experience. First and foremost, my greatest honor and appreciation go to Mr. Basir Saibon, my supervisor as well as lecturer, for his tireless dedication and effort in guiding me in completing this project. His guidance, encouragement and suggestions have greatly influence the success of this project, not to mention his timely sense of humors which had brought great pleasure and relief weary hours. It has been a great privilege to be a part of his group.

Special thanks to Mr. Abdul Latip Abdul Hamid, main technicians in RF & Microwave lab for his continuous assistant and co-operation, especially during process of building project's hardware, testing and measurement. Thanks to my lecturer, Dr. Mohd. Fadzil bin Ain, for his time and guidance which inspire me in working on my project. My appreciation also goes to technicians in Intel's lab, Mr. Khairul Anuar and Miss Sahida Hussain for their willingness to provide assistant during the hours of implementing my hardware. Many thanks to Mr. Mohd Nurul Azrol for his help and effort especially in PCB board etching of my project. Thanks to senior technician, Mr. Mohd Naim Abdullah who had assisted me to obtain required hardware components of my project.

Next, I would like to thank my family and friends who have supported me throughout these years. Thanks to my mother and father, who had always encouraged me especially in academic field.

My acknowledgments would not be complete without expressing my appreciation to all members of University Science Malaysia. I felt very fortunate to have had the opportunity to study in this world from the vantage point of science and engineering, and am truly amazed at what a marvelous place it is.

LIST OF FIGURES

LIST OF TABLES

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION

1.1 Background of project

The radio frequency integrated circuit (RFIC) market showed a remarkably growth during the last few years. Especially wireless devices, e.g. cellular and cordless phones, pagers, global positioning system (GPS) devices, etc., are rapidly becoming indispensable tools for our daily life. Increasing the data rate of communications channels within a fixed bandwidth forces an increase in amplifier linearity requirements. Modulation and coding schemes are often used to provide the increase, but the corresponding system requirements for instantaneous amplifier bandwidth and linearity have been hard to achieve. The balanced configuration offer the linearity and output power needed to satisfy these requirements. Balanced amplifier is a type of amplifier that combines 2 similar single-ended amplifiers into single unit, which can perform amplification of input signal. Combining two amplifiers in a balanced configuration will improve power output at 1dB compression point and third order modulation point by 3 dB, and provide redundancy, so that the system will continue to operate if a device fails.

The balanced amplifier configuration is a practical method for obtaining a broadband amplifier with output power equal to twice that of a single amplifier. A balanced amplifier has been widely used in low noise and power amplifications in the microwave frequency spectrum because of its better performances in noise, input and output return losses, and stability comparing to a single-ended amplifier. The balanced amplifier does have the following disadvantages:

a) difficult integration because of double the component counts for power divider and combiners;
b) more expensive because of more components.

However, due to higher performance and more subject to the environmental and production conditions, the balanced amplifier is best for high-end amplification such as in the infrastructure applications.

1.2 Objective and scope of project

RF Integrated System is a system with integrated circuits operating in the band of frequency ranging from few hundreds Mega hertz to Giga hertz. In fact, the emerging field of wireless communications had embarked the importance of RF circuit design. One of the most important RF circuit in an integrated system is low noise amplifier. The primary goals for any low noise amplifier used in RF Integrated Systems are low noise figure, adequate gain and stable.

For the case of balanced amplifier, input and output with good matching networks are also required. The balanced topology has several important features:

1) 3 dB higher compression and third order intercept point than a single stage
2) 50 ohm input and output match
3) redundancy which minimizes a hard failure

The use of balanced configuration provides good input and output match, and helps to ensure stability. Finally, the bandwidth should be high enough to include the up-link (mobile device to base-station) frequencies for CDMA standards of 1.9 GHz.

Thus, the goal of this project is to design two balanced amplifiers, each contains 2 single ended low noise amplifier on a printed circuit board (PCB) with center frequency **1.9 GHz**. As far as concern, 1.9 GHz is considered very high frequency. The amplifier should have characteristics as below:

(a) 50 ohm input and output match
(b) noise figure below 5 dB
(c) unconditional stability
(d) high linearity with 1 dB compression point and third order intercept point more than 10 dBm
(e) adequate gain of $\geq$ 10 dB

Design specifications for the balanced amplifier designs are shown in **Table 1.1**. The major focus of the balanced amplifier design is on its noise and linearity characteristics. Thus, requirement for amplifier's gain is less important and need to be tradeoff accordingly to improve noise, stability or linearity performance throughout the project.

Table 1.1: Design specifications of balanced amplifier

PARAMETERS	REQUIRED VALUE	DESIRED VALUE
Center Frequency	1.9 GHz	1.9 GHz
Optimum operating bandwidth	40 MHz 1.88 GHz – 1.92 GHz	200 MHz 1.80 GHz – 2.00 GHz
Output 3rd order interception (IP3) (at f = 1.9 GHz)	15.8 dBm	17.8 dBm
Noise Figure (at f = 1.9 GHz)	< 5 dB	< 4 dB
Output power at 1dB compression	11.0 dBm	13.0 dBm
Input Return Loss	-10 dB	-12 dB
Output Return Loss	-15 dB	-17 dB
Small Signal gain	5 dB	10 dB
DC power consumption	< 800 mW	< 500 mW

Generally, there are many different types of topology used for low noise amplifier design, especially at the input and output matching counterpart. In this project, 2 types of balanced amplifier with different input and output matching topology are designed. One with lumped element matching network and another with microstrip stub matching network. Both designed are completed and implemented on printed circuit board (PCB) to be analyzed and characterized accordingly for benchmarking.

1.3 Project Methodology

In this project, the design of balanced amplifiers is divided into 6 phases or stages:

(1) System and Circuit Design

(2) Simulation, Tuning and Optimization

(3) Layout Design

(4) Hardware Implementation

(5) Hardware Testing and Measurement

(6) Characterization for Benchmarking Tradeoff

The first stage is to design amplifier circuits using ideal components. Ideal components are general components used in design tools that only consist of value but no other supplemental information (etc. characteristic such as parasitic and S-parameter variations). This process includes dc bias circuit design, noise and impedance matching, as well as 3 dB hybrid coupler design. In this stage, several mathematical calculations and some assumptions are involved.

In the second stage, **Agilent's Advanced Design System (ADS 2003A),** a powerful RF/Microwave CAD and simulation tools are used. Simulations had been run on the amplifier circuits to obtain the characteristic and performance of the initial design. The component's variable in the basic circuits are tuned and optimized to meet the project's requirements. During the process of optimization and tuning, ideal components in the amplifier circuits are replaced by actual model from ADS component library to obtain more accurate results.

Obtaining optimal balanced amplifier circuits, layouts are designed using the features of ADS. Hardware implementation, testing and characterization are done after the layout is finalized. The amplifier circuits are built on Taconic Duroid PCB boards. In this stage, surface mount technology (SMT) are used to connect each components to the etched transmission line on the PCB board. The hardware of balanced amplifier are tested with Hewlett Packard's network and spectrum analyzer equipped in the RF & Microwave Lab. Using these equipments, required measurements and results are taken for analysis and characterization.

1.4 Structure of the report

Chapter 1 is an introduction intends to provide a short review of balanced amplifier background in the market of RF integrated system. A brief discussion of balanced amplifier's application is presented. Objectives and scopes of the project are specified in this chapter to clarify the purpose of this thesis.

Chapter 2 provides a short insight into the basic structure of a balanced amplifier. Introduction and short explanation about the functional building blocks of an amplifier in balanced configuration are included. The advantage of a balanced amplifier over a single-ended amplifier also presented in tabulated form so that the readers of this thesis are able to understand and appreciate it.

Chapter 3 contains the text regarding the system design of the balanced amplifier. System design means the design of functional modules and structures of the balanced amplifier in system level. In this project, 2 types of single-ended amplifier are designed, one with lumped element matching network and another one with microstrip matching network. This chapter is divided into 3 sections consists of system design of both balanced amplifier topology, as well as the integration of single-ended amplifier in balanced configuration. Design steps, configurations and methods used in each building block are briefly discussed. Explanations of the principle operations of each element in the design are also given.

Chapter 4 provides further design steps of the balanced amplifiers, as a continuation of the design in last chapter. In this chapter, building blocks of a balanced amplifier include low noise amplifier with both lumped element and microstrip matching network and 3-dB branch line coupler are designed in detail. Graphical illustrations and mathematical calculations of this design stage are enclosed. The single-ended low noise amplifiers are integrated using two 3-dB branch line couplers to obtain balanced configuration.

Chapter 5 presents the simulation results of the balanced amplifier designed in previous chapters. In advance, these results review the performances of the amplifier circuits in ideal conditions. Discussion and explanations of these results are made to

clarify whether the designs at this stage met the required specifications. This chapter also provides the comparisons of both type of balanced amplifier according to results from simulations.

Chapter 6 show the steps involved in layout design and hardware implementation. This chapter stated several points that being considered while designing the layout. Processes involved in building the hardware of balanced amplifiers are explained.

Chapter 7 consists of results obtained from hardware test and measurements. These results are compared to simulations results in Chapter 5. The balanced amplifiers are characterized based on results from the measurements. Differences occurred between these two results are discussed. Factors of variations are explained in details at the end of this chapter.

Chapter 8 draws the final conclusion of this project and suggests the future work as the continuation of this project. Methods to improve the performances of the balanced amplifier and efficiency of the works are also included.

CHAPTER 2 LITERATURE REVIEW

2.1 Microwave transistor single-ended amplifier

Single-ended amplifier consists of an active device, which is a transistor. In definition, active device is a device that requires a source of energy for its operation, and has an output that is a function of present and past input signals. In term of RF amplifier, input to the device is RF signal, while is amplified RF signal represents output of the device. The amplification represents the gain and function of input signals. The required source of energy is provided by dc bias of the active device.

In this project, the transistor used is Agilent Technologies' ATF-34143 GAsFET pHEMT device. Housed in a 4-lead SC-70 (SOT-343), this device is a high dynamic range, low noise figure dual-voltage GAsFET built on Agilent Technologies' proven pHEMT process. (See Appendix A for the technical data of this device). The device is designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. Based on its featured performance, ATF-34143 is ideal for the first stage of base station LNA due to the excellent combination of low noise figure and high linearity. The device is also suitable for applications in Wireless LAN, MMDS and other systems requiring super low noise figure with good intercept in the CDMA standard frequency range.

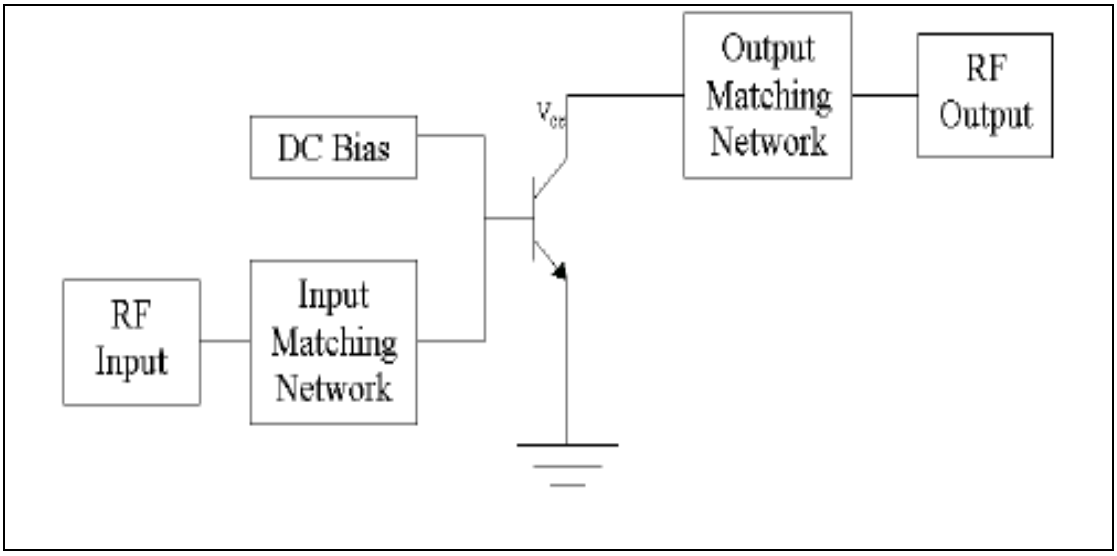

Figure 2.1: Circuit Block Diagram of Single-Ended Amplifier

Figure 2.1 shows the complete block diagram of the single-ended amplifier design. The amplifier consists of a microwave transistor, DC bias circuit, input and output matching networks. RF inputs are fed into the active device through input matching network. The devices are biased through the DC bias circuit. The amplified RF signal are then being output through output marching network Details of DC bias circuit and matching networks are explained in the sections below.

2.2 DC bias circuit

RF/Microwave transistors require some form of circuit to set the correct bias conditions for a particular RF performance. The main purpose of the bias circuit is to maintain the drain current regardless of any drift in the DC current gain of the FET device. In the case of a GAsFET pHEMT device, overtime the transconductance, g_m falls, with a resulting drop in the bias current. The S-parameters of a device are fixed and do not age so long as the correct bias current is maintained. A drop in bias current, over lifetime, will cause the RF device gain and output power to fall.

There are two main types of bias circuit, an active current mirror and a passive bias circuit. In this project, passive bias circuit is used. This technique uses an inductor to feed voltage to the drain of the RF device. What is required is a low DC resistance but a high RF resistance to ensure that the RF circuit is not loaded and RF signals do not flow onto the supply lines (where the RF signals could find their way back onto the input of the RF device causing gain ripple and possibly instability). At high frequencies, the RF bias consists of an inductor followed by a shunt capacitor. The inductor 'chokes' any RF signal, in other words the RF circuit see's an open circuit looking into the inductor. The capacitor shorts out any RF leakage through the inductor. However, at very low frequencies where RF devices have high gain the inductor will appear as a short circuit, i.e. it appears invisible to the RF circuit. What the RF circuit sees however the short circuit of the capacitor is. A short circuit applied to the RF circuit may cause instability as devices are only guaranteed to be stable in a 50-ohm system. This can be improved by adding a 50-ohm resistor in series with the inductor so that at low frequencies the RF circuit will see at least 50 ohms. **Figure 2.2** shows the bias circuit configurations. The resistor provides a 50 ohm load to the RF transistor at low frequencies. (www.rfic.co.uk)

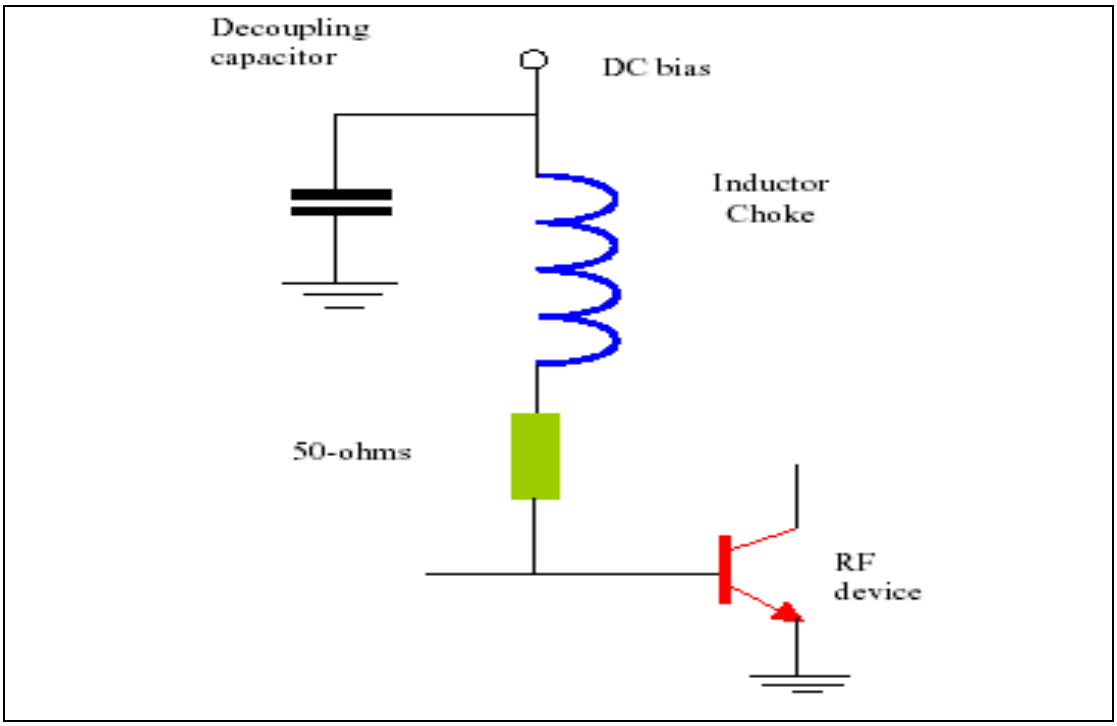

Figure 2.2: RF amplifier bias circuit arrangement

2.3 Input and Output impedance matching network

Impedance matching is a critical step in designing microwave amplifiers for use in practical systems. Impedance matching networks perform the important function of transforming input and output impedances of the microwave device to the 50 ohm load that represents transmission line's impedance. Matching the impedance of a network to the impedance of a transmission line has two principal advantages. First, all the incident power is delivered to the network. As such, a matched circuit or load causes maximum power transfer from input to output. Second, the generator is usually designed to work into impedance close to common transmission line impedances. If it does so it is better behave, the load impedance has no reactive part which can pull the generator frequency. Furthermore, the VSWR on the line is unity or close to unity so that line length is immaterial and the line connecting the generator to the load is non-resonant.

In this project, both lumped element and microstrip network are used for input and output matching. For the first topology using lumped element network, passive LC networks are used to match impedance between the device and 50 ohm load. These matching networks are designed using combinations of inductors and capacitors. There are two types of simple LC impedance matching networks: two element LC high-pass

and LC low-pass networks. In this design, the high-pass network that consist of series C and shunt L are used.

For the second topology using microstrip matching networks, microstrip single stub matching is used to match input/output impedance to the 50 ohm load. Stubs are shorted or open circuit lengths of transmission line intended to produce a pure reactance at the attachment point, for the line frequency of interest. Open circuit stubs are used in this project for constructional reasons. The length of stub is kept as short as possible for wider bandwidths.

The matching network must apply conjugate complex impedance to the needed impedance to match impedance to 50Ω. This method of matching is called conjugate matching. The impedance which can be seen by looking into a device is named S_{11} and the impedance which can be seen by looking from the device into the matching circuit is named Γ. Both impedances have the same magnitude and a conjugate angle. An open stub with variable length acts as variable parallel capacitor which adjusts the magnitude of the reflection coefficient on the 20mS circle. A 50Ω line with variable length to the device adjusts the phase.

(Knut Brenndorfer, 1996)

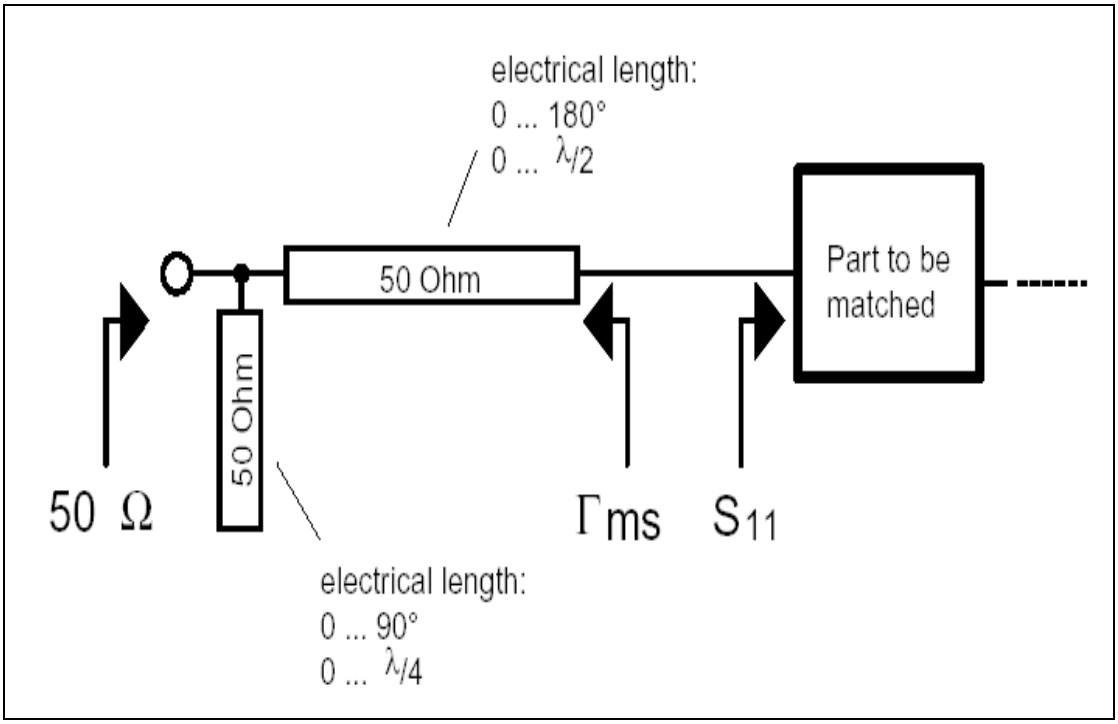

Figure 2.3: Microstrip open stub matching

2.4 Balanced amplifier

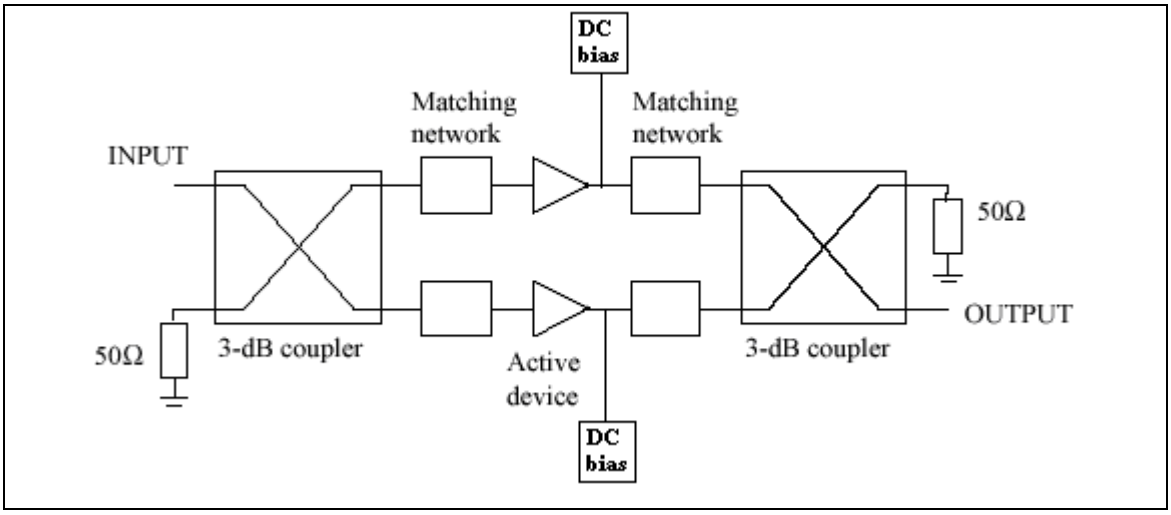

Figure 2.4: Building block of a balanced amplifier

Figure 2.4 shows basic structure of a balanced amplifier. Two similar single-ended amplifiers are in parallel connected in each branch as shown. The single-ended amplifiers mentioned are built of microwave transistors which act as an active device. Microwave transistors typically don't match well with 50Ω. This causes poor input and output matching with the transistor. However, a balance amplifier circuit can overcome this problem. The balanced amplifier cancels the input and output reflections of two identical transistors by using two 3 dB 90 degree hybrid couplers. The first 90 degree hybrid coupler (refer to **Figure 2.5** for coupler's dimension and **Figure 4.6** for coupler's specifications) splits the input signal into two signals of equal power that are 90 degrees out of phase. These two out of phase signals are then used to drive the two amplifiers. These signals are amplified and sent to another 90 degree hybrid coupler. This coupler then recombines the amplified signals as a single output signals.

Furthermore, due to the fact that the inputs and outputs of the two transistors are out of phase, the reflections at these inputs and outputs due to poor match of the amplifiers will be channeled back through the input and output terminal to 50 ohm load where they will be absorbed. Therefore if we look into the amplifier we will effectively 'see' the 50 ohm loads and will therefore present a good match.

In addition this configuration will give us an extra 3dB's of output power (less the insertion loss of the coupler) and also the 1 dB compression points will be approximately 3dB higher (In other words the circuit will be able to handle double the

power without distortion). The main drawback of this circuit is the power required for two amplifiers.

Some other advantages of a balanced amplifier are:

- Redundancy – if one of the amplifier stages fails, the balanced amplifier will still operate with reduced gain and linearity. The circuit provides a degradation of a -6 dB loss in gain if a single amplifier section fails.
- Good input and output VSWR (< 1.5:1).
- Easily cascaded – each unit is isolated by the coupler
- High degree of stability. The balanced amplifier has better stability since each branch amplifier is terminated with a fix load, close to either 50 Ω or 75 Ω.
- The individual amplifiers can be designed for flat gain, noise figure, and so on (even if the individual amplifier VSWR is high), with the balanced amplifier input and output VSWR dependent on the coupler (i.e. ideally the VSWR is 1 if the amplifiers are identical).
- The individual amplifier stages can be optimized for gain flatness or noise figure, without concern for input and output matching.
- High isolation between the two sides of the device. Common mode reflections caused by poor VSWR from the transistor and its matching network, are transferred to the isolated port where they are terminated. Therefore, the amount of reflected power that can cause integration problems, from the input and output ports is greatly reduced.
- Bandwidth can be an octave or more, primarily limited by the bandwidth of the coupler.
- The overall output power requirement is shared between two transistors. This is desirable from a thermal management point of view, as the waste heat generated can be spread across a larger area.

The disadvantages of the balanced amplifier configuration are that the unit uses two amplifiers, consumes more dc power, and is larger. Also, in practice, there is a finite insertion loss of > 0.1 dB associated with the amplifiers. (Guillermo Gonzalez, 1997)

2.5 3-dB branch line coupler

Following from section above, the used of 3 dB coupler is to split the input signals and recombine output signals from two single-ended amplifiers. In balanced configuration, power divider played an important role in improving isolation and reducing reflections. Power division and combination are generally accomplished by the use of power divider or a hybrid coupler. Many kinds of power divider or hybrid coupler can be use for balanced configuration – Lange couplers, Wilkinson power divider, branch line coupler etc. Although power dividers can be used in this design, low loss 3 dB hybrid couplers prove to be superior for several reasons. One of the main reasons is, hybrid couplers are four port devices characterized by good match and isolation, and by a fixed 90 degree phase shift between the output ports.

In this project, branch line 90 degree hybrid coupler is selected due to its simple layout and ease in integrating with the amplifier layout. The geometry of the branch-line coupler is shown in **Figure 2.5**. A branch-line coupler is made of two main transmission lines shunt-connected by two secondary (branch lines). It has a symmetrical four port. First port is input port, second and third ports are output ports and fourth port is the isolated port. It is obvious that due to the symmetry of the coupler any of these ports can be used as the input port but at that time the output ports and isolated port changes accordingly.

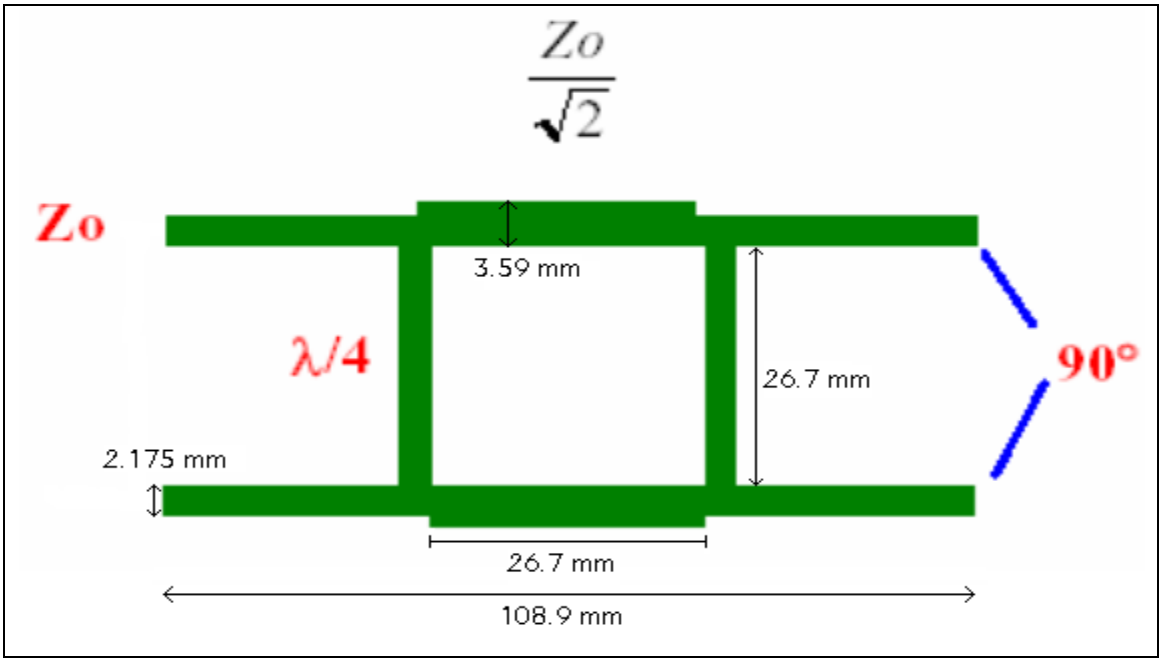

Figure 2.5: Branch Line Coupler

2.6 Comparison of single-ended amplifier and balanced amplifier

Table 2.1 summarizes the merits and disadvantages of the balanced amplifier compared to the single-ended amplifier.

Table 2.1: Balanced amplifier versus single-ended amplifier

ITEM	SINGLE-ENDED AMPLIFIER	BALANCED AMPLIFIER
Input/Output Return Losses, S_{11}, S_{22} (frequency 1.9 GHz with PHEMT devices)	< 10 dB	> 15 dB
* Optimum Noise Figure Source Matching with Better Input Return Losses (frequency 3 - 4 GHz and noise figure <0.5 dB with FET device)	< 2 dB	> 17 dB
** Performance Stability in Temperature Changes (-20°C to 85°C)	Poor and depend on the selected components	Excellent
* Unconditionally stable (Stability factor, k: 1 GHz to 5 GHz with FET device)	0.2 – 1.5	1.0 – 4.0
* Performance Stability With Component Variation	Poor ± 40 dB	Excellent ± 20dB
Third order intermodulation product (IP3)	31.5 dBm	3 dB higher
Output power at 1dB Gain Compression	20 dBm	3 dB higher
Total Power Consumption	3 dB less	--
Reliability	Depends on device used	2 time higher
Cost	2 time less	--
Tuning	More works needed	Excellent
Integration	-	Difficult
Size	> 3.15 cm^2	2 time larger

* Detail of comparison will be further evaluated in section below.

** if stability factor, k is more than 1, the amplifier is unconditionally stable, which is a desired characteristic of all amplifier design.