DESIGN AND ANALYSIS OF CMOS RFIC IF LOWPASS FILTER 1.9GHz RANGE FOR CDMA APPLICATIONS

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CHAPTER 1

INTRODUCTION

In this century, the world's is starting to bloom by the wireless communication. 3rd generation (3G) communication requirement is a must in the recent market demand and 4th generation (4G) is on its way. Portable wireless communication systems require many complex transceiver components. Many design techniques have been proposed for monolithic filters as they are key components of the transceiver systems. Since cost, reliability, performance, size and power consumption are main concerns of these components, they should ideally be realized as integrated circuits wherever possible. More challengingly, the whole system is implemented as of system on chip (SOC), which also known as radio frequency integrated circuit (RFIC).

Due to high frequency, radio frequency (RF) filters are often discrete components rather than on chip. But, analog filter is preferred in the design of high-performance electronic circuits for the intermediate frequency (IF) stage with low cost and low power consumption for high-speed applications. At baseband, filters are mostly digital filter due to programmability. In general, filters can appear in three places:

1) RF stage : RF filters are mostly discrete components.
2) IF stage : IF filters are analog integrated components.
3) Baseband : Digital filters are typically applied.

1.1 Objectives and Goals

This research sets out to design a completely integrated tunable low pass filter (LPF) with a bandwidth of 200 MHz utilizing Silterra 0.18μm submicron (SM) complementary metal oxide semiconductor (CMOS) technology. The application of this filter is narrowed down to perform as an IF filter in a superheterodyne receiver.

Currently there are a few reported examples of this type of fully integrated CMOS filter. The main goals in the research will be to design and analyze the various types of filter architecture construction and choose one of the best of them to implement on integrated circuit layout base on their performance.

1.2 Dissertation Organization

Generally, this dissertation has 6 chapters and it is organized as followed. The overview of Code Division Multiple Access (CDMA), types of receiver and theory of analog filters will be reviewed in Chapter2. In Chapter 3, operational amplifier (op-amp) and transconductance (Gm) cell are designed and analyzed to review the pros and cons of their performance for further design in analog filter using active-RC methods for the former and Gm-C technology for the latter respectively. 1^{st} and 2^{nd} order of active-RC filter are designed meanwhile 1^{st} ,2^{nd}, 3^{rd} and 4^{th} order of the Gm-C filter are also designed and the analysis of their performances are carried out in Chapter 4, just before the conclusion is being drawn in the same chapter. Chapter 5 shows the implementation and issues regarding the filter circuit layout. Finally, Chapter 6 presents conclusions and provides suggestions for further study. Due to the limitation of space, test bench circuits and logs are placed at Appendix.

CHAPTER 2

OVERVIEW AND THEORY

2.1 Overview of CDMA

CDMA with abbreviation of Code Division Multiple Access is a form of *spread-spectrum* because every communicator will be allocated the entire spectrum all of the time. CDMA uses unique spreading codes to spread the baseband data before transmission in a channel. Signals are distinguished not by time or frequency but by a code attached to each signal. At the receiving end, the signal is distinguished from all other signals by its code and is extracted from them. Fig. 2.1 shows the comparison with other type of multiple access schemes.

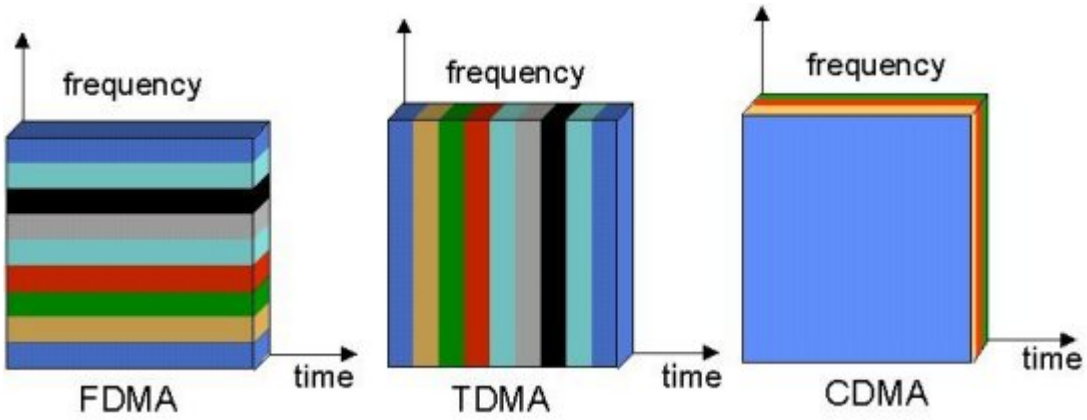

Figure 2.1: Multiple access schemes

From history, originally there were two motivations for using CDMA: either to resist enemy efforts to jam the communications, or to hide the fact that communication was even taking place. In March 1992, the Telecommunications Industry Association (TIA) established the TR-45.5 subcommittee with the charter of developing a spread-spectrum digital cellular standard. In the July of 1993, the TIA gave its approval to the CDMA IS-95 standard [C.D.G. 1999]. In the mid-1990s, the International Telecommunication Union (ITU) initiated an effort to develop a framework of standards and systems that will provide wireless and ubiquitous telecommunications services to

users anywhere at anytime. Subsequently, International Mobile Telecommunications-2000 (IMT-2000), a subgroup of the ITU, published a set of performance requirements of 3G. In recent times, CDMA has gained widespread international acceptance by cellular radio system operators as an upgrade that will increase both their system capacity and the service quality [Yang S.C. 2004]. In CDMA2000-3X, the spreading rate is 3 times the CDMA2000-1X standard which means the channel bandwidth is triple of 1.25MHz, i.e. 3.75MHz as shown in Fig. 2.2.

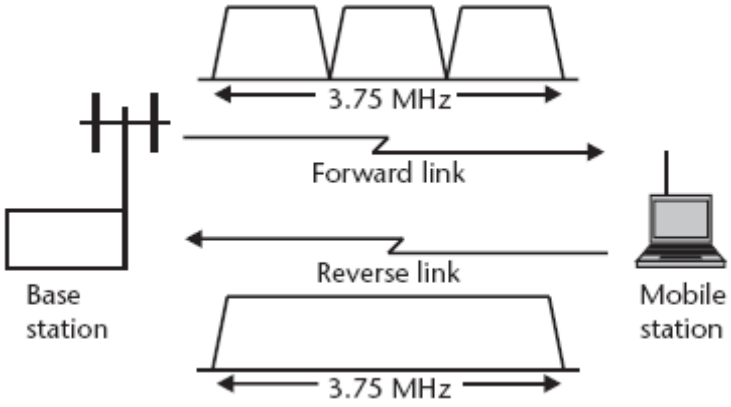

Figure 2.2: CDMA2000-3X bandwidth per channel

This project is designed to cover the entire channel for CDMA2000-3X front-end receiver using the standard specified for 3G communication system.

Specification [John B.2000, Johan J.2002]:

Channel bandwidth	: 3.75 MHz
Guard band[1]	: 625 KHz
Total 45 channels bandwidth	: 197.5 MHz
Center frequency	: 1.9 GHz
Modulation	: QPSK/O-QPSK

[1] Guard band is necessary to harmonize with other 3G systems such as UMTS [YangSC2004].

2.2 Overview of Transceiver

There are three different receiver architectures, i.e. the heterodyne, homodyne receiver or known as zero-IF or direct-conversion receiver and the superheterodyne.

2.2.1 Heterodyne receiver

The receiver core consists of *n* image-suppressing down-mixing stages that are converting the signal from the RF to a high IF, and then to a lower IF, as shown in Fig. 2.3. This type of receiver heavily relies on many high quality factor (Q) filters to perform both the mirror signal suppression and the channel selection which are expensive. Integrating these high Q filters on silicon is not workable because the power consumption of an active filter is proportional to the square of its quality-factor [Johan J. 2002].

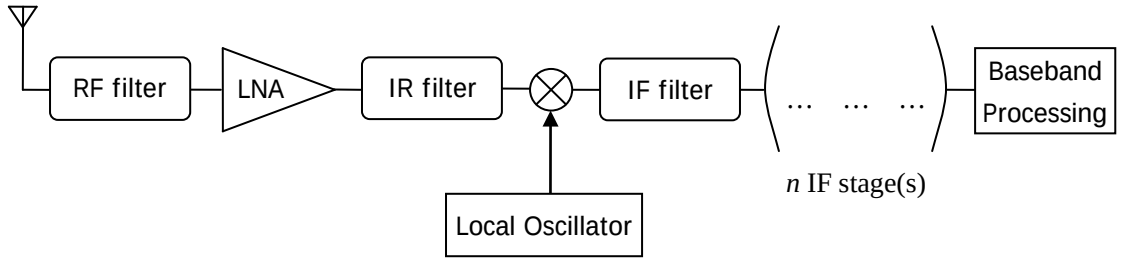

Figure 2.3: Heterodyne front end receiver

2.2.2 Homodyne receiver

The direct conversion receiver topology shown in Fig. 2.4 is more suited to integration than the heterodyne because it eliminates the image reject (IR) and IF filters, only the RF filter remains. After filtering by the RF filter and amplification by the low noise amplifier (LNA), the entire RF band is mixed directly to baseband with a local oscillator (LO). Since the mixed signal is directly to baseband, there is no image component. Direct conversion topologies have been employed in pager applications which have relatively low performance requirements [Abidi A. 1995]. However, this architecture introduces the problems of DC offset and flicker noise from the mixer and baseband processing circuits [Razavi B. 1998].

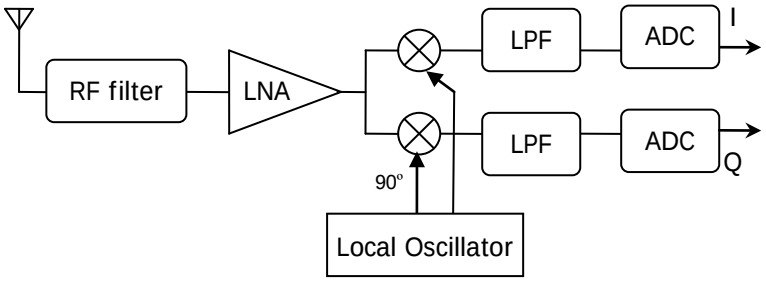

Figure 2.4: Homodyne front end receiver

2.2.3 Super-heterodyne receiver

This architecture have utilized feature from direct conversion receiver in maintaining the same level of integration meanwhile low IF have been used to eliminates the problems associated with direct conversion receivers. Due to its high performance, most commercial RF communication transceiver today uses the super-heterodyne receiver architecture [Lee T.H. 2001]. As shown in Fig. 2.5, the receiver uses a collection of components of various technologies for each of the block.

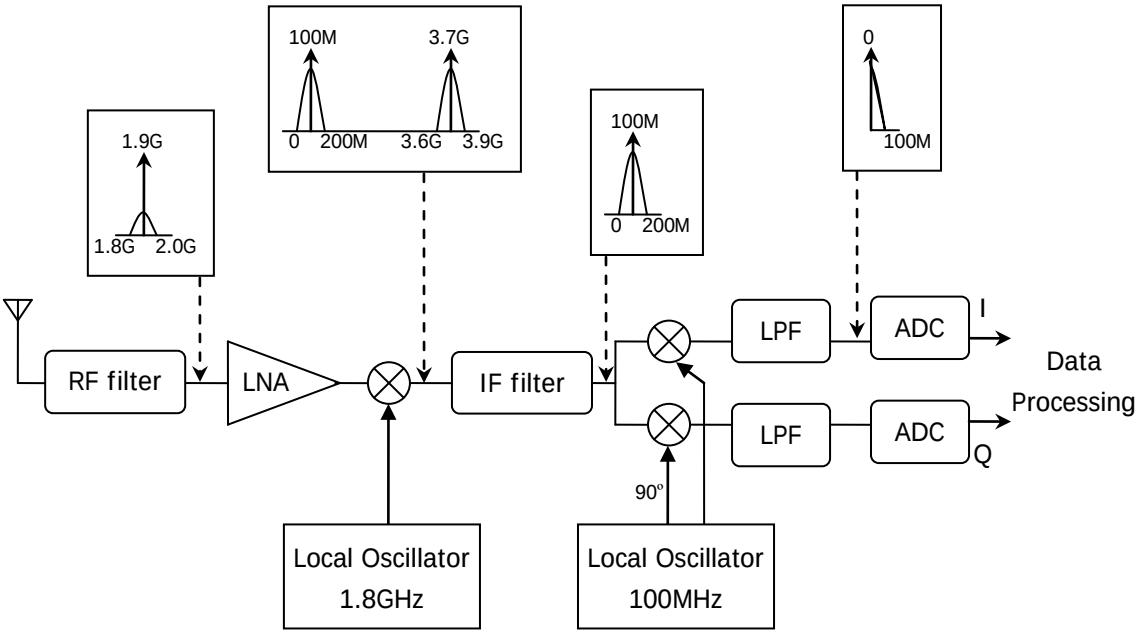

Figure 2.5: Superheterodyne front end receiver

From antenna, the noisy RF signal first passes through a RF bandpass filter to suppress all out of band signals while relaxing the required dynamic range for passband signal around 1.9GHz. The signal is then amplified by the LNA. The main function of the LNA is to provide enough gain to overcome the noise of the following stages such as the mixer. Moreover, the LNA should add minimum noise as noise introduced by the LNA has a large effect of the overall noise performance of the receiver. LNA should also accommodate large signals without distortion or having good linearity.

After amplification of the received signals by the LNA, both the desired signal and undesired noise are translated down to a fixed IF which is 100MHz by a down-conversion mixer utilizing a 1.8GHz LO. The mixer has system requirements such as good conversion gain, low noise figure, low power consumption and high linearity. Initially, a high Q filter is needed at the output of the mixer to remove out of band interference. However, since the signal bandwidth is located at low IF, i.e. from 0 to 200MHz, a lowpass filter with 200MHz bandwidth and low Q can be employed as IF filter. As discussed before, lower IF receiver needs only low Q IF filter compare to higher IF. The output of the IF filter is further processed by a demodulation block where baseband information is extracted from the IF signal with the help of 100MHz LO. The baseband signal is further filtered by LPF and then digitized by an analog to digital converter (ADC) for data processing.

2.3 Overview of Filter

The basic concepts of the electric filter were developed in 1915 by Wagner in Germany and feedback theory by Bode in 1930 has ignited the evolution of signal processing [Schaumann R. 2001]. An electrical filter can be considered as a network which consists of an interconnection of components, such as resistors, capacitors, inductors, and active devices (transistors, amplifiers, controlled sources). The filter processes applied electrical signals which are referred to as the input. The product of the processing by the network is referred to as the output. However, the output will differ

according to the type of filtering performed by the network. In depth, this network changes the signal amplitude and phase as a function of the frequency, and no new frequency components are added to the signal. Since the application and the operating frequency of the filter are at IF, continuous-time filter is preferable.

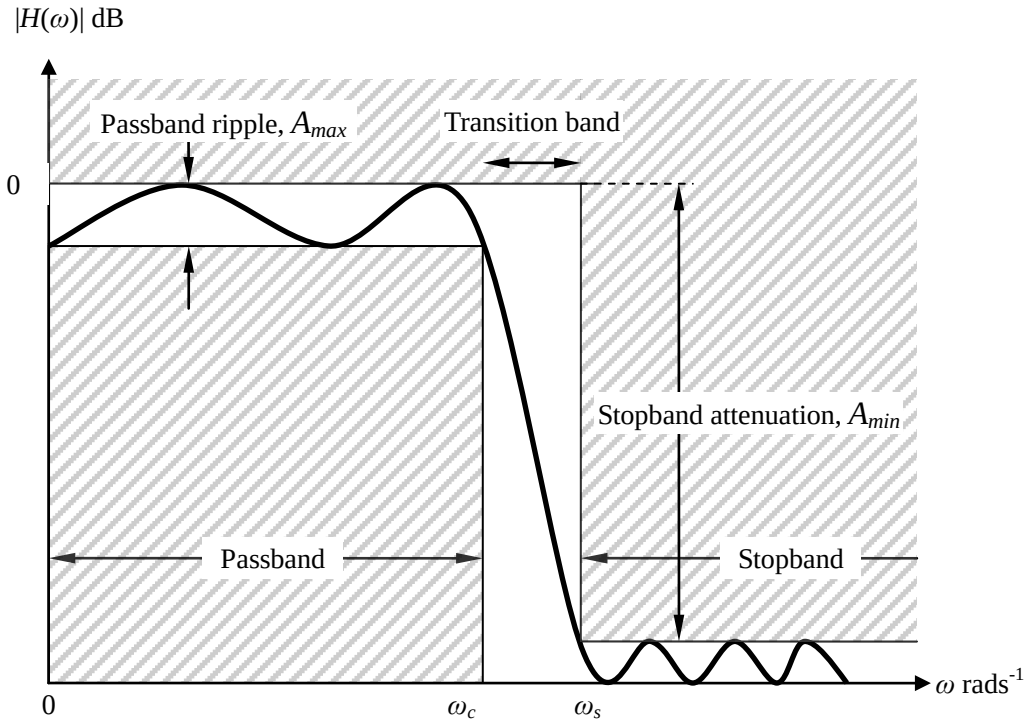

Figure 2.6: Lowpass filter transmission characteristics

For a low pass filter, its function is to pass low frequency from dc to some desired cutoff frequency as known as passband (PB) and to attenuate high frequency which is known as stopband (SB). The filter is specified by its cutoff frequency ω_c, stopband frequency ω_s, passband ripple A_{max}, and stopband attenuation A_{min}. Ideally, selectivity ratio must be unity, i.e. cutoff frequency and stopband frequency should be the same, no ripple, exactly a rectangular shape of magnitude response. However, in practice, there is a transition band and ripple in the frequency response as shown in Fig. 2.6. Compromises and trade-offs must always be reached in filter design, some arising from fundamental limitation and some from practical realities [Toumazou C. et al. 2002].

2.3.1 Approximation Methods

An ideal lowpass filter can be approximated to a more general prototype lowpass function such as Butterworth, Chebyshev, Bessel and Elliptic as shown in Table 2.1 and Fig. 2.7, depending on each design specification. In IF filter design, the output of processed IF signal should get as clean as possible within the passband while maintaining the same amplitude and phase as close as possible to the ideal lowpass filter. For implementation, maximally flat response corresponds to a clean passband without ripple and flat stopband attenuation due pole only response. Meanwhile the order of the filter determines the sharpness of the rolloff or in another words, the difference in ω_c and ω_s. Since there is no strict specification for IF filter, in addition to the discussion on low IF receiver, only low Q filter is required. Thus, Butterworth approximation with overall Q=0.707 is chosen. However, the number of order will be determined in latter chapter during filter performance comparison.

Table 2.1: Approximation function comparison

	Butterworth	**Bessel**	**Chebychev**	**Elliptic**
Pole Location	on unit circle	on ellipse	on ellipse	on ellipse
Magnitude Response	maximally flat	flat	ripples in passband	ripples in passband & stopband
Phase Response	linear	linear	less linear	poor
Filter order for flat stopband attenuation	high	very high	medium	low

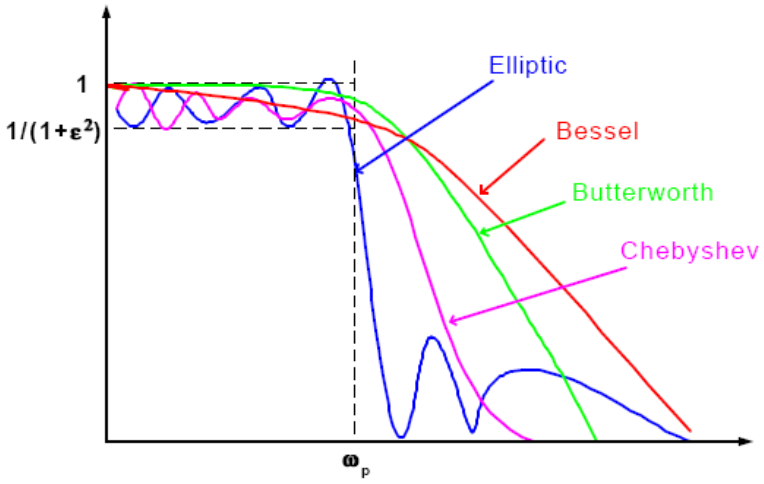

Figure 2.7: Magnitude response of various approximated filter [Soorapanth T. 2002]

2.4 CMOS analog filter

Although increasingly many filtering application are handling by digital signal processing (DSP) and digital filters, but analog continuous-time filter is still a favorable solution. First is due to bandlimiting of the real-world analog signal interface circuit before any sampling operation can be taken by DSP. Secondly, filtering at high frequency especially in front end receiver, require ultrafast sampling and digital circuit which may not be realistic as shown in Fig. 2.8 [Schaumann R. 2001]. As a result, monolithically integrated analog active filters is preferable in implementing IF filter. CMOS technology is chosen due to higher circuit density, low cost and maturity.

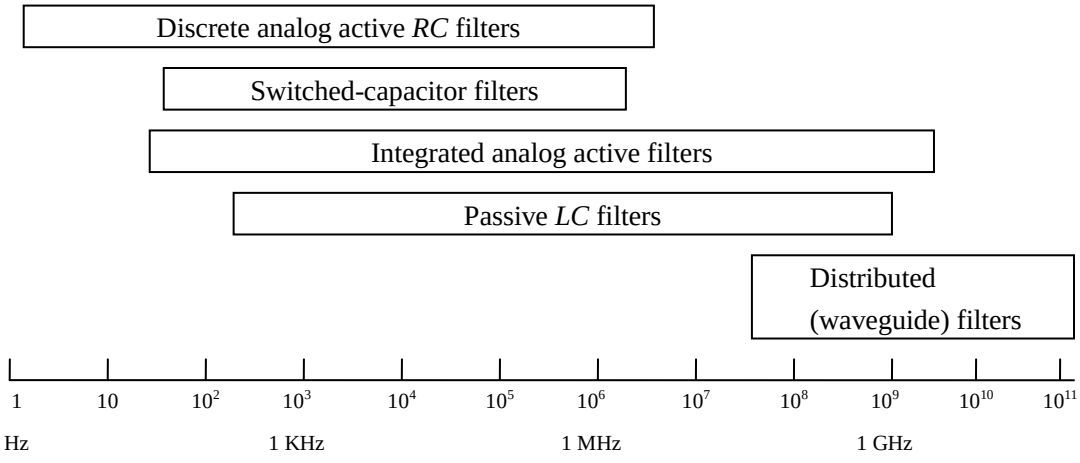

Figure 2.8: Choice of filter type as a function of operating frequency range

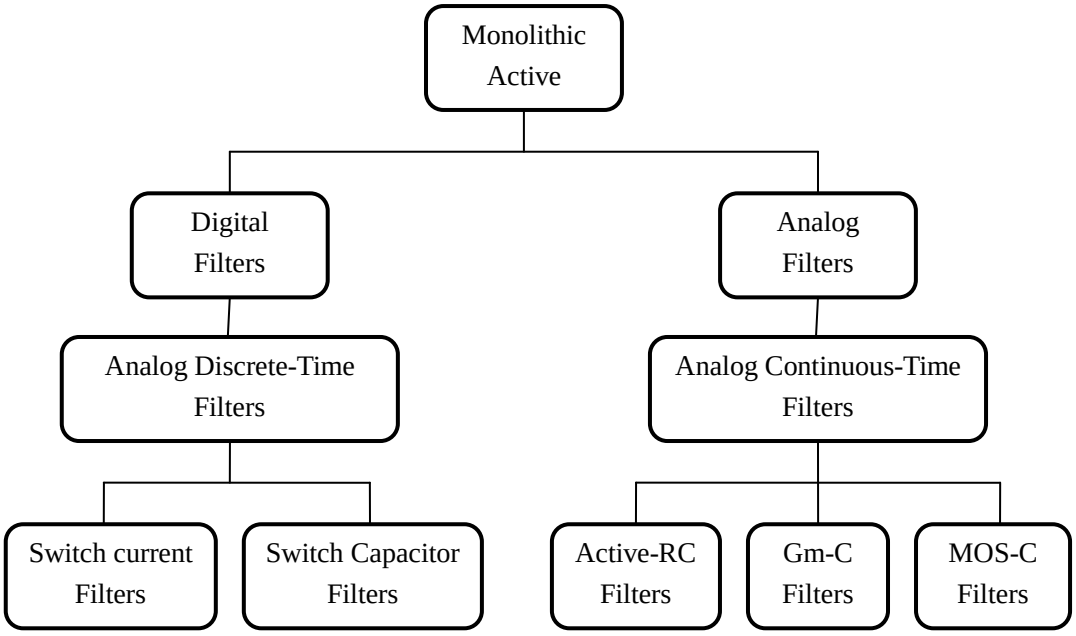

Figure 2.9: Classification of active filter

Different types of monolithic active filters can be distinguished as shown in Fig. 2.9. For the design of high performance active filter, there are 3 main types of analog continuous-time filters, their performances are compared in Table 2.2. Active-RC and Gm-C will be discussed due the discussion of the integrator in the following section.

2.5 Integrators

Any filter, no matter active or passive, consists of integrators. This dissertation is dealing only with voltage integrator. For a passive filter, the capacitors provide the integration functions because the voltage across a capacitor is the integral of current flowing through the capacitor as dictated by Eq.(2.1) and Eq.(2.2) for time domain and s domain respectively.

$$v(t) = \frac{1}{C}\int_0^t i\,dt \tag{2.1}$$

$$V(s) = \frac{1}{sC} I(s) \tag{2.2}$$

2.5.1 Active-RC filters

For active-RC filter, inverting integrator is formed with Miller integrator configuration as shown in Fig. 2.10(a). It consists of op-amp, resistor and capacitor as basic elements which perform good linearity with large power consumption. The transfer function is shown in Eq.(2.3) and Eq.(2.4). The use of op-amp generally limits the frequency range due to the gain bandwidth product (GBW). However, predictable design can be accomplished if the GBW of op-amp is 10% higher than the cutoff frequency of filter [Schaumann R. 2001], i.e. 220×10^6 dBHz. Due to the use of high performance Silterra SMCMOS process, it is possible to achieve this requirement.

$$\frac{V_{in}(s)}{R} = \frac{-V_{out}(s)}{1/sC} \tag{2.3}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sCR} \tag{2.4}$$

2.5.2 Gm-C filters

The basic building block of Gm-C filters is a voltage-to-current transconductance (Gm) loaded with a capacitor (C) as shown Fig. 2.10(b). An ideal transconductance amplifier is an infinite bandwidth voltage-controlled current source, with an infinite input and output impedance [Nauta B. 1993]. The relationship is shown in Eq.(2.5) to Eq.(2.7) where the unity gain frequency is Eq.(2.8). Since Gm-C filters use integrator built from an open-loop transconductance amplifier driving a capacitive load, it avoids the problem of excess phase from high frequency nondominant poles. Gm-C filters have lower power consumption and higher frequency capability from the others. The only trade-off is the linearity due to the open loop nature and noise performance.

$$I_{out}(s) = G_m \times V_{in}(s) \tag{2.5}$$

$$V_{out}(s) = \frac{1}{sC} I_{out}(s) \tag{2.6}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{G_m}{sC} \tag{2.7}$$

$$\omega_{ta} = \frac{G_m}{C} \tag{2.8}$$

2.5.3 MOS-C filters

MOS-C filter is having the same configuration as active-RC except that the bulky resistor at input is replaced by an equivalent CMOS tunable transistor biased in the triode region and reduces area, as shown in Fig. 2.10(c). Due to the use of transistors as simulated resistors, small output impedance op-amp should be employed, which means multistage op-amp is needed. As a result, the limited frequency response of op-amp with two or more stages limits their use to low-frequency applications. Thus, this type of filter is not covered in this dissertation.

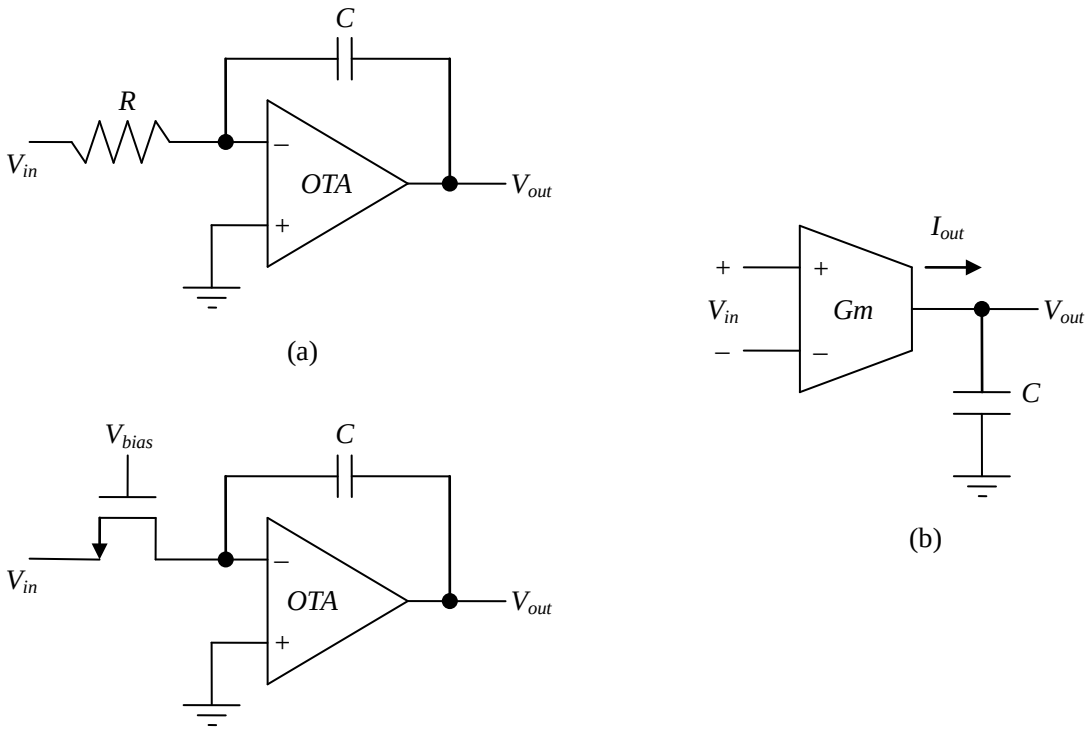

Figure 2.10: Basic building block of integrator (a) Active-RC (b) Gm-C (c) MOS-C

Table 2.2: Performance Comparison

	Active-RC	**Gm-C**	**MOS-C**
Power	high	low	very high
Linearity	good	poor	good
Area	medium	medium	medium

2.6 Distortion

For a nonlinear system, a single frequency input signal will yield multiple output signals at multiples of the input signal frequency. This undesired signal is called harmonic distortion (*HD*). Total harmonic distortion (*THD*) is defined to be the ratio of the total root mean square (*rms*) value of the second and higher harmonic components to the rms value of fundamental as indicated in Eq.(2.9). If two signals with different frequencies are applied at the input, sum and difference of frequencies signal are generated at the output. Such distortion is called intermodulation distortion (*ID*).

$$THD = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \ldots}}{V_f} \times 100 \tag{2.9}$$

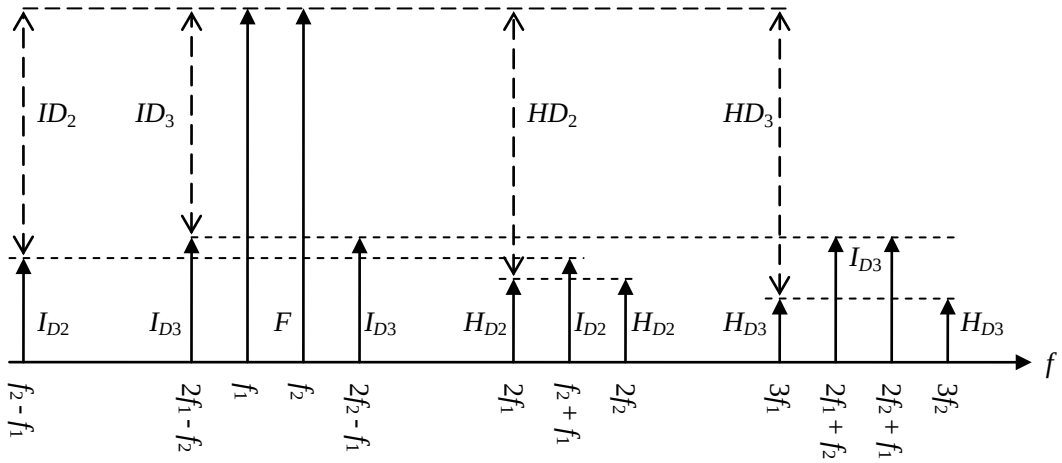

Figure 2.11: Spectrum of nonlinear distortion [Johan J. 2002]

$$HD_2 = \frac{H_{D2}}{F} \quad \text{and} \quad HD_3 = \frac{H_{D3}}{F} \tag{2.10}$$

$$ID_2 = \frac{I_{D2}}{F} \quad \text{and} \quad ID_3 = \frac{I_{D3}}{F} \tag{2.11}$$

where F is the amplitude of the fundamental output tone with frequency of f_1 and f_2, IMP_i and H_{Di} represent the amplitudes of the i-th order intermodulation product and harmonic respectively. ID_i and HD_i stand for the i-th order intermodulation ratio and harmonic distortion ratio respectively.

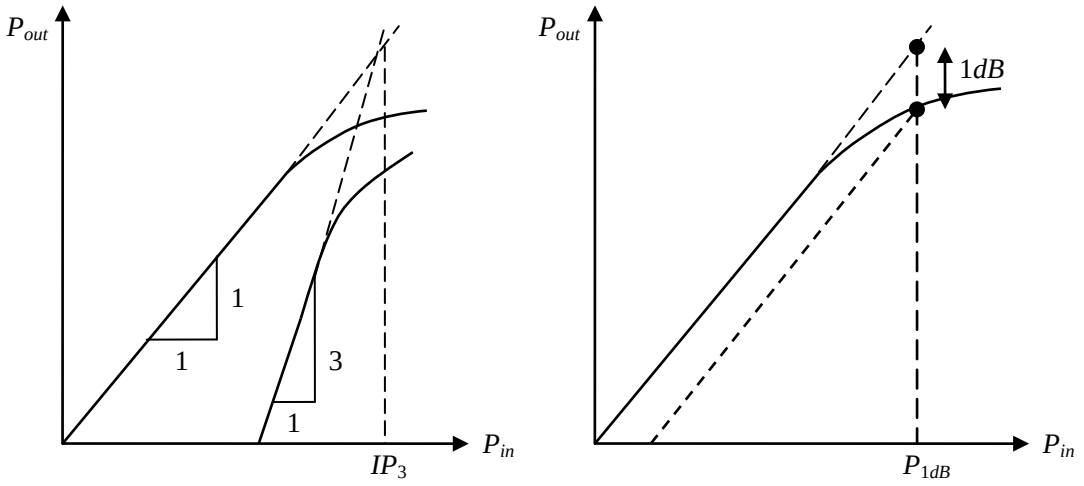

Figure 2.12: (a) *IP*3 (b) 1*dB* compression

The third intercept point IP3 is the intercept point of the fundamental component with the third order intermodulation component while 1dB compression point is defined as the point where the fundamental gain deviates from the ideal small signal gain by 1dB as shown in Fig. 2.12. *dBm* is the usual unit for measurement which is equal to

$$dBm = dB + 10 \tag{2.12}$$

2.7 Noise

The performance of a filter is limited by noise which is generated by the circuit itself such as thermal noise and flicker noise and interference from surrounding such as coupling of power supply and coupling capacitor. Noise can be measured in rms value for time domain or spectral density for frequency domain. From Wiener-Khinchin theorem, spectral density function is the Fourier transform of the autocorrelation function of the time domain signal as shown in Eq.(2.13).

$$V_{n(rms)}^2 = \int_0^\infty V_n^2(f)\,df \tag{2.13}$$

The signal to noise ratio of a signal node in a system is the ratio of signal power to the noise power measured in dB. If the random signal $V_{n(\mathrm{rms})}$ is applied to a 1Ω resistor, the average power dissipated is equal to the noise power. Thus, the SNR is given as

$$SNR = 20\log\left(V_{x(rms)} / V_{n(rms)}\right) \tag{2.14}$$

CHAPTER 3

DESIGN OF OP-AMP AND GM CELL

3.1 OP-AMP

The CMOS op-amp is consists of two gain stages and a unity gain output stage as shown in Fig. 3.1. The first stage is a differential input single ended output stage which used p-type of transistor as the differential input pair while n-type is used as the current mirror active load because p-type input differential pair stage maximizes the slew rate and also reduce 1/f noise [Johns D. & Martin K. 1997]. Such configuration maximizes the transconductance of the second stage [Palmisano et al. 2001]. The second gain stage is n-type common source gain stage that has an active load that have less voltage drop. The third stage is a common drain buffer stage which is also known as source follower. The op-amp circuit is biased by a bias circuitry that stabilizes the transistors' transconductances, where the values are determined by a single resistor and the device dimensions, and thus independent of power supply voltage as well as process and temperature variations.

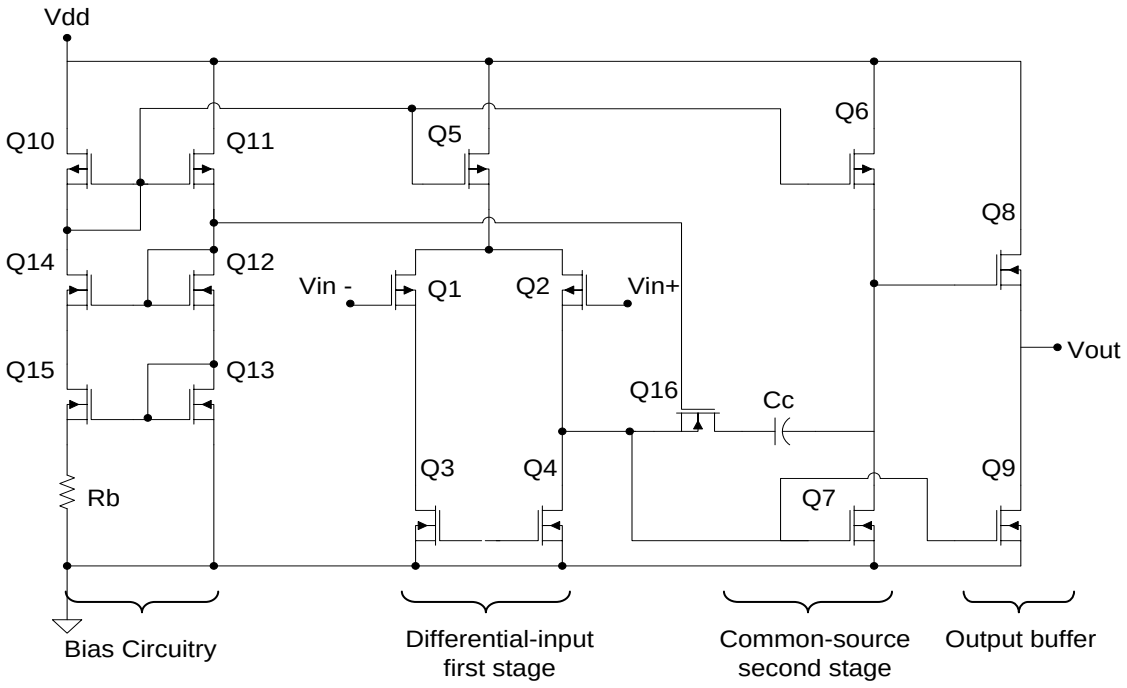

Figure 3.1: Schematic of the two-stage op-amp

3.1.1 Design Approach

A. Systematic Offset Voltage

As far as transistors Q3 and Q4 are concerned, when input voltage is zero, they contribute to the systematic offset voltage and CMRR, besides affecting noise performance according. In order to improve both offset and CMRR, accurate matching must be guaranteed by both a proper layout design and symmetrical bias conditions. This means the same drain-source voltages as

$$V_{GS3} = V_{DS4} = V_{GS7} \tag{3.1}$$

This gives

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_{D3,4}}{I_{D7}}\left(\frac{W}{L}\right)_7 \tag{3.2}$$

The width of transistors Q3 and Q4 following different requirements. Setting minimal length to minimize silicon area or setting high channel length to minimize flicker noise. From Fig. 3.1, assume that the transistor Q16 is “on” and the compensation capacitor has been shunted, Since the $I_{D6} = I_{D7}$, in order to maintain the same current I_{D5} must have

$$\frac{I_{D6}}{I_{D5}/2} = \frac{(W/L)_7}{(W/L)_{3,4}} \tag{3.3}$$

This is the necessary condition to ensure no input-offset voltage is present

$$\frac{2(W/L)_6}{(W/L)_5} = \frac{(W/L)_7}{(W/L)_{3,4}} \tag{3.4}$$

B. Stable Transconductances Biasing

Transconductances must be stabilized in which transistor transconductances are matched to the conductance of a resistor. As a result, the transconductances are independent of power supply voltage as well as process and temperature variations. First, assumed $(W/L)_{10} = (W/L)_{11}$ so that both sides of the biasing circuit having the same current due to the current mirror Q10, Q11. Hence,

$$I_{D15} = I_{D13} \tag{3.5}$$

$$V_{GS13} = V_{GS15} + I_{D15}R_b \tag{3.6}$$

$$V_{eff13} = V_{eff15} + I_{D15}R_b \tag{3.7}$$

$$g_{m13} = \frac{2\left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right]}{R_b} \tag{3.8}$$

Thus, transconductance of Q13 is totally independent of power supply voltages, process parameters, and other parameters variations. Such ratio is chosen

$$(W/L)_{15} = 4 \times (W/L)_{13} \tag{3.9}$$

in order for

$$g_{m13} = \frac{1}{R_b} \tag{3.10}$$

R_b is arbitrary set to 2KΩ, g_{m13} is 500μA/V. $(W/L)_{15}$ is adjusted to 24.48μm and follow Eq.(3.9) to provide an arbitrary 150μA of current in biasing circuitry. Then, use the above equations and materials in [Johns D. & Martin K. 1997] to tune the W/L of each transistor as shown in Table 3.1.

Table 3.1: Finely tuned component values for the two stage op-amp

Parameters	**W**
Q1, Q2	44.10 μm
Q3, Q4	15.66 μm
Q5	31.32 μm
Q6, Q7	55.08 μm
Q8, Q9	66.06 μm
Q10, Q11, Q12, Q13, Q14	6.12 μm
Q15	24.48 μm
Q16	20.88 μm
C_C	280 fF
Rb	2 KΩ

3.1.2 Simulation and analysis

a) AC analysis:

At room temperature, Fig. 3.2 shows that open loop dc gain is 56.8dB and the stopband attenuation is flatly at -60dB. The dominant pole is located at 575.4 KHz. As the temperature increase, gain and phase will have slightly increased due to the increase of transconductance because of the dependency of current on temperature.

Fig. 3.3 shows that Common Mode Rejection Ratio of the op-amp. CMMR is maintained at 60.75dB. As temperature increase, CMRR will be slightly reduced due to the reduction of differential gain which is also dependence on transconductance. Fig. 3.4 shows the Stability Response by referring to the Loop Gain and Loop Gain Phase which indicate that the gain margin is -20dB and phase margin is 54^{o} .

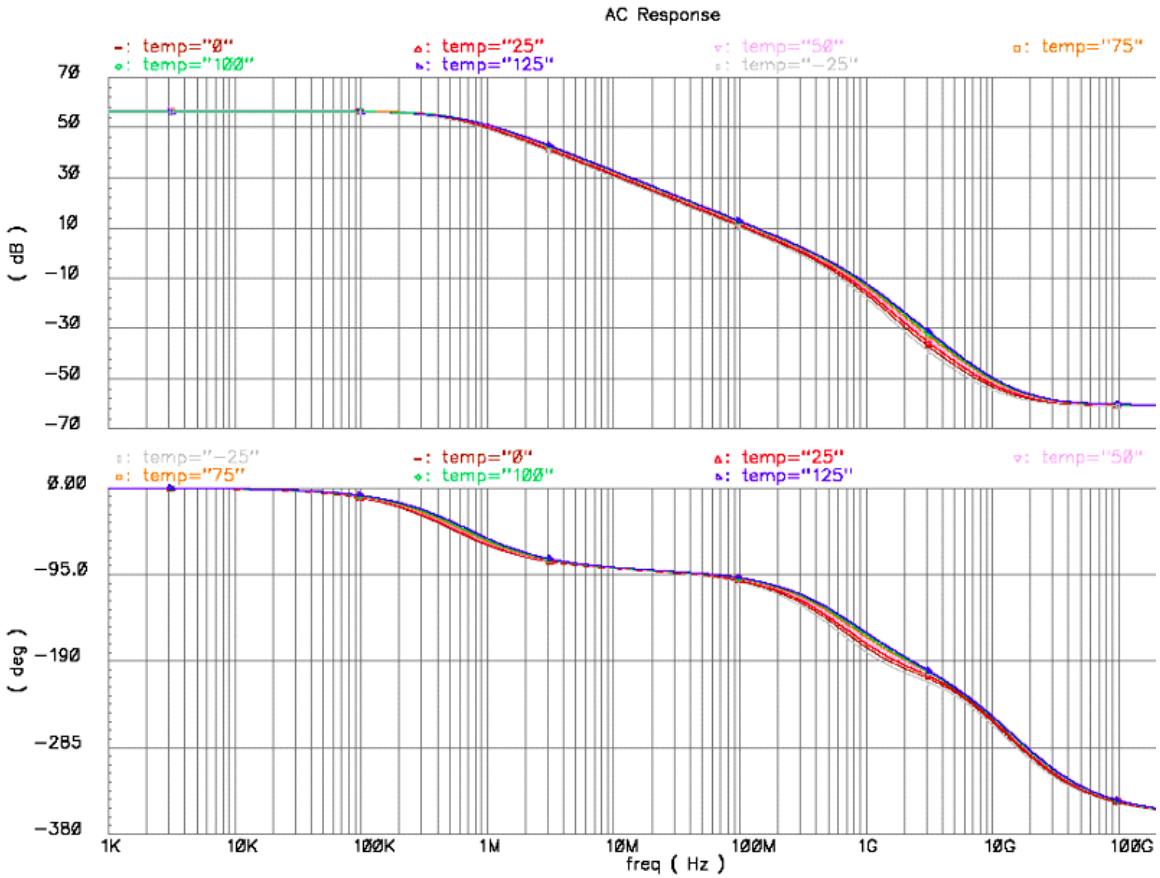

Figure 3.2: Op-amp's open loop gain and phase frequency response

As temperature increased, loop gain will be slightly reduced, while loop gain phase will be increased. This is due to the thermal voltage V_T is related to the built in potential Φ_o which is inverse proportional to junction capacitance C_j which will finally affect the system pole.

Fig. 3.5 shows that loading capacitance, C_{load} is importantly affecting the system's stability. As this capacitance increased, phase margin and gain margin will be reduced due to the pole have been shifted nearer to the oscillation axis. This phenomenon is also applied to the internal compensation capacitor, Cc.

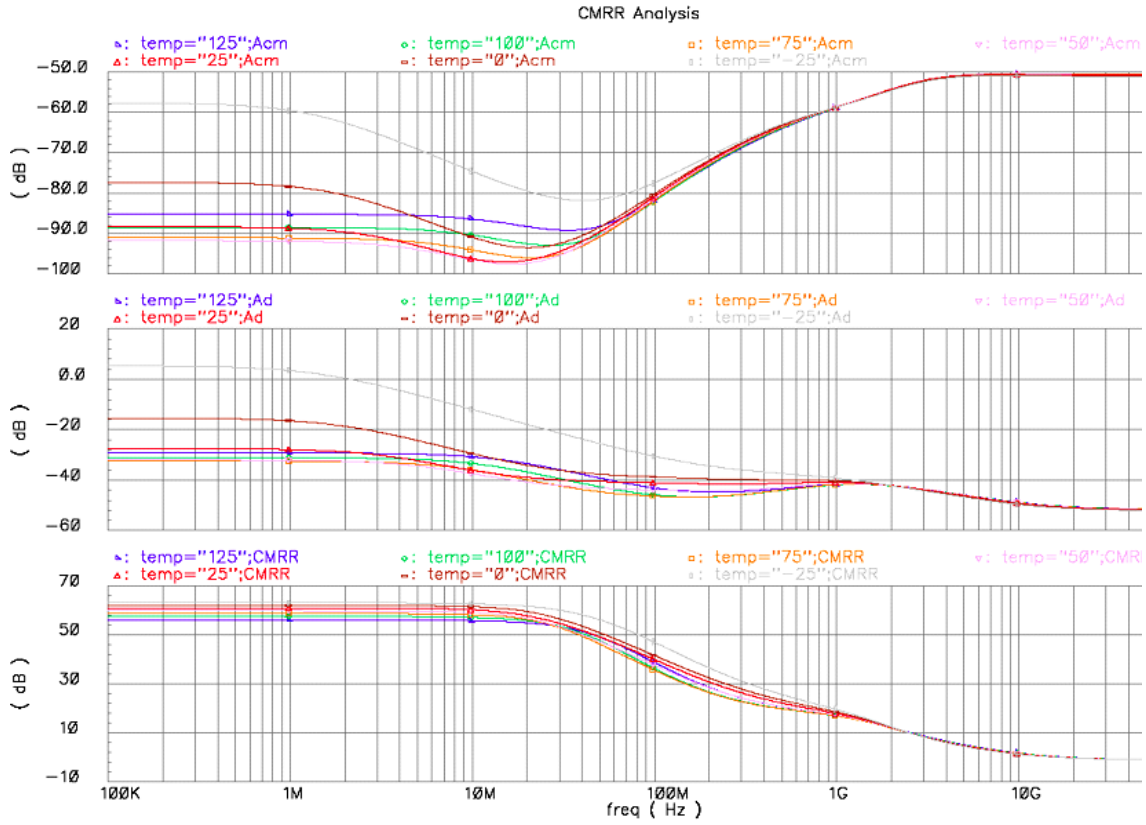

Figure 3.3: Op-amp's open loop Common Mode Rejection Ratio (CMRR)

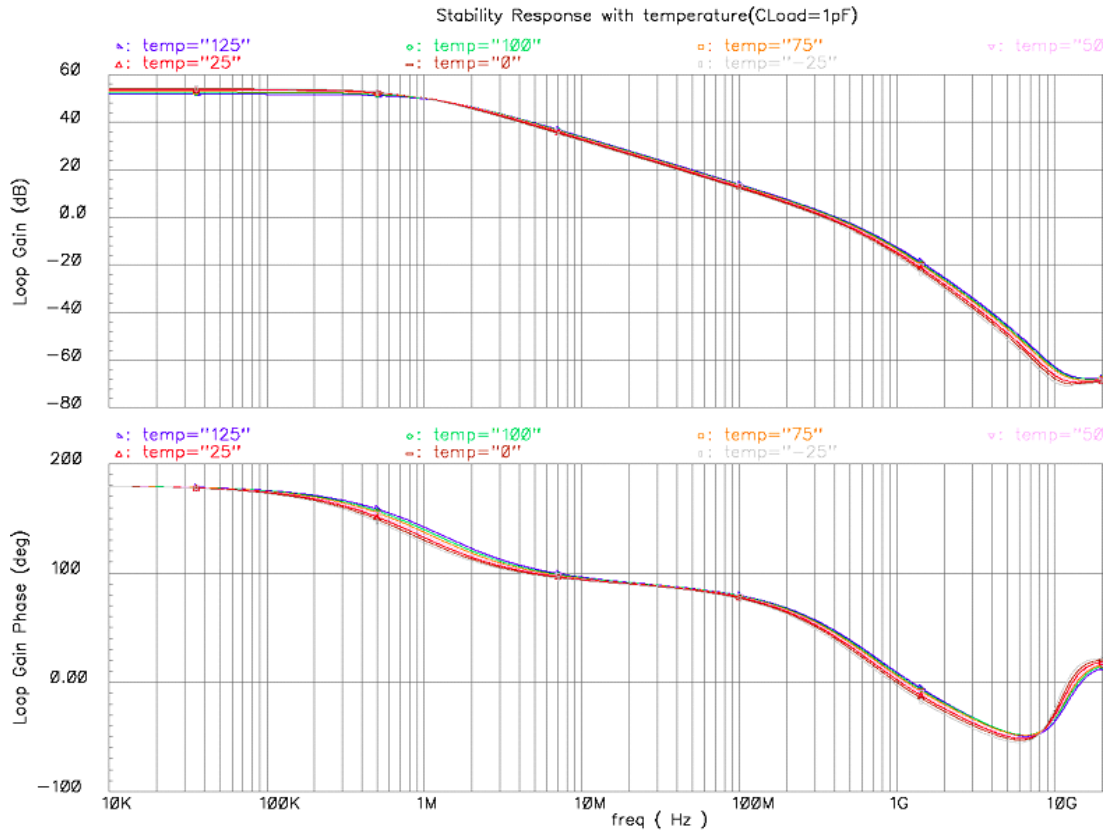

Figure 3.4: Op-amp's Loop Gain Phase Stability Response

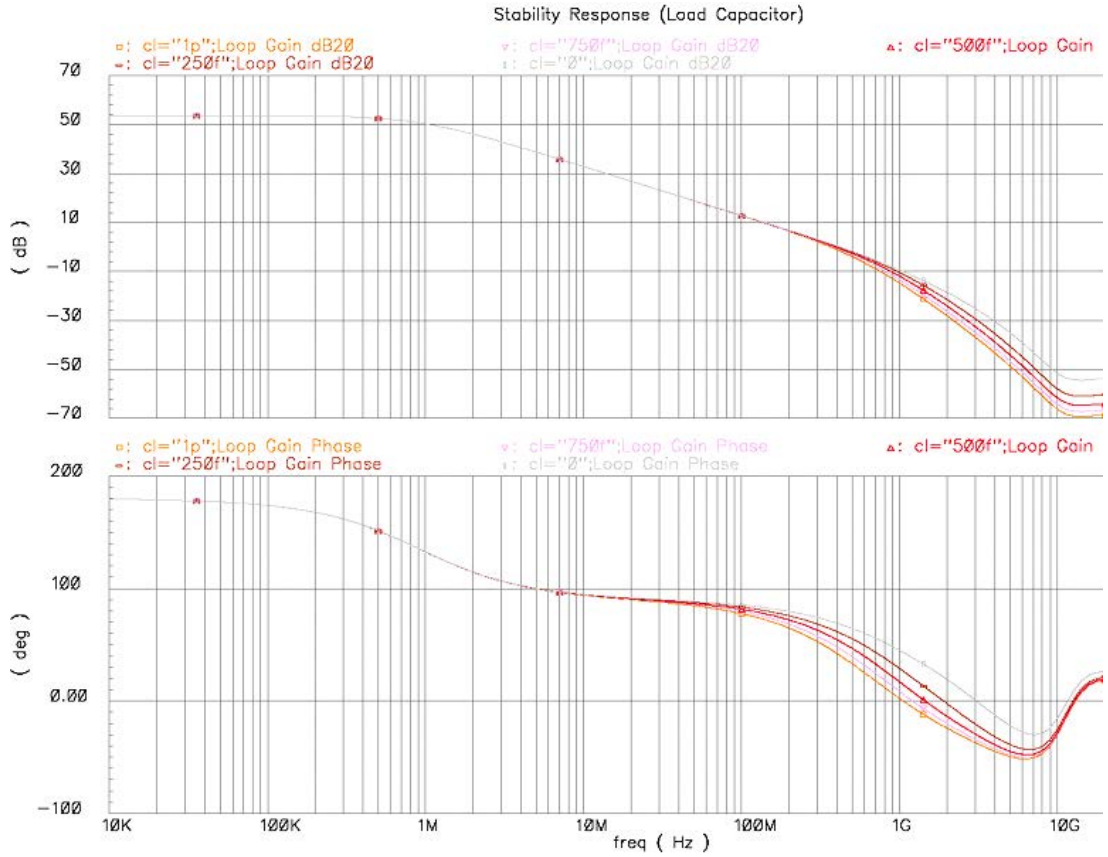

Figure 3.5: Op-amp's stability response with various loading capacitance

b) DC analysis

As shown in Fig. 3.6, minimum common mode input is 0V and the maximum common mode input is 1.43V which is also the ICMR. This is not a surprise because the input stage is using PMOS [Gregorian R. 1999].This op-amp is having high linearity about 1.007 along the ICMR. It confirms the discussion in section 2.4 that active-RC filter have high linearity.

The common mode input voltage is not exactly located at half of the power supply which is 0.9 V. However it only deviates about 1.3mV due to some mismatch at the input stage. The offset voltage can be further reduced by employing fully differential output op-amp.

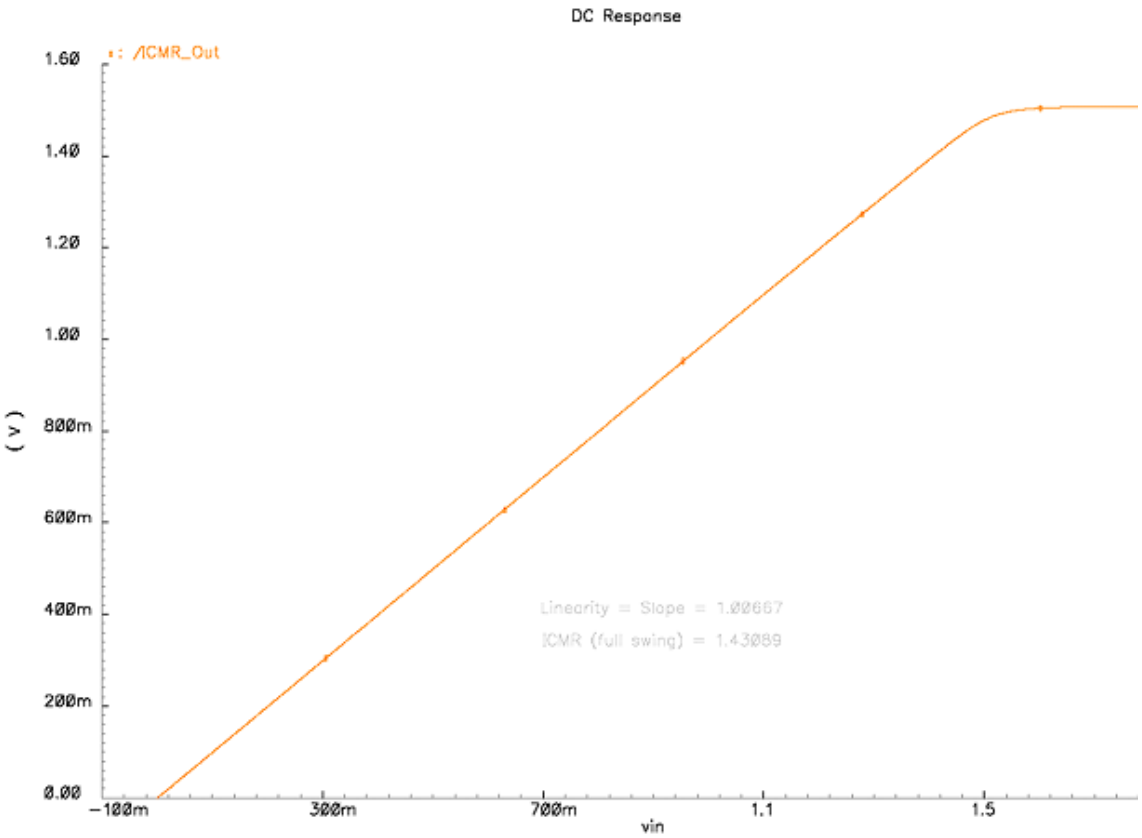

Figure 3.6: Op-amp's Input Common Mode Range (ICMR)

c) Transient analysis

Fig. 3.7 shows the transient response for the step input. It is noticeable that rise time is longer than fall time which is 4.221ns and 1.171ns respectively. Positive slew rate exhibits much slower than negative slew rate which is 189.2V/µs and 682.9V/µs respectively. It means that current flow to charge a capacitor is much slower than sinking the charge through transistor to ground. This is true because of 1pF loading capacitor is connected at the output. The op-amp exhibits 2.7% of overshoot which is tolerable and settling time of 6.125ns. Temperature affects much on positive slew rate, rise time and settling time.

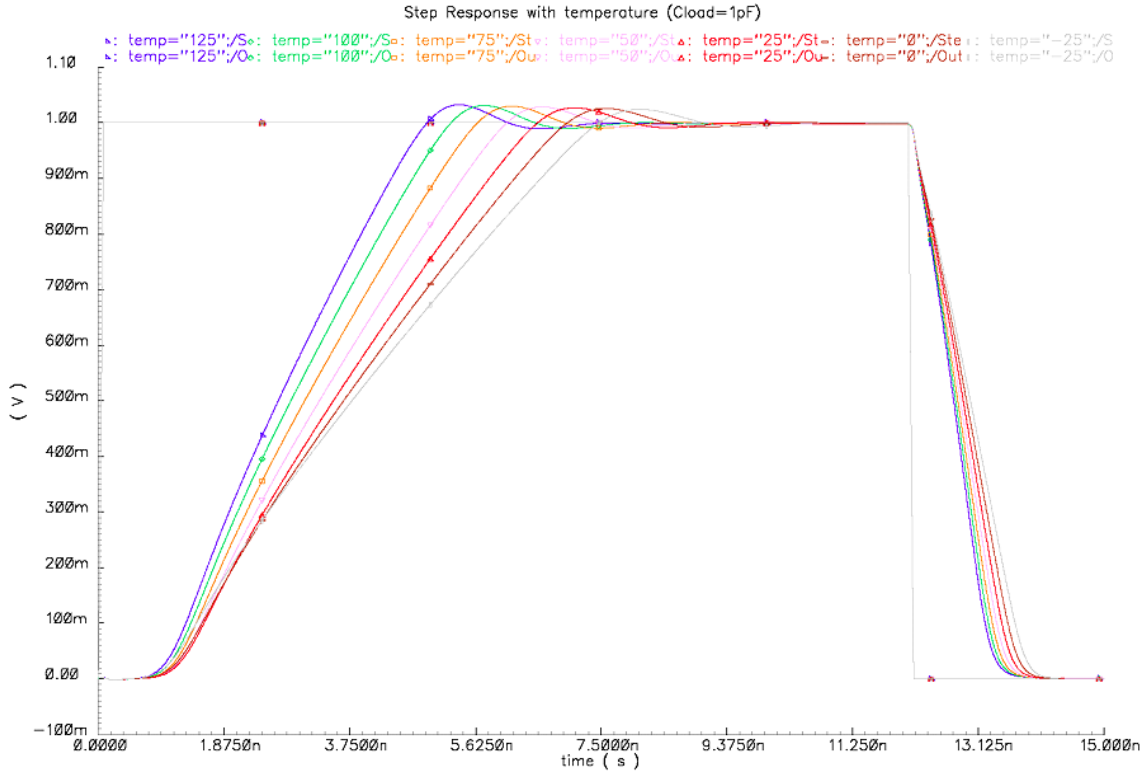

Figure 3.7: Op-amp's step response with temperature variation

Fig. 3.8 shows that internal compensation capacitance have slew rate limiting as a trade off to maintain close loop stability. Nominally, compensating capacitor C_C is set to 0.22 times the loading capacitor C_{load} [Gregorian R. 1999]. For this case, C_C is fine tuned to 280fF as the load is 1pF.

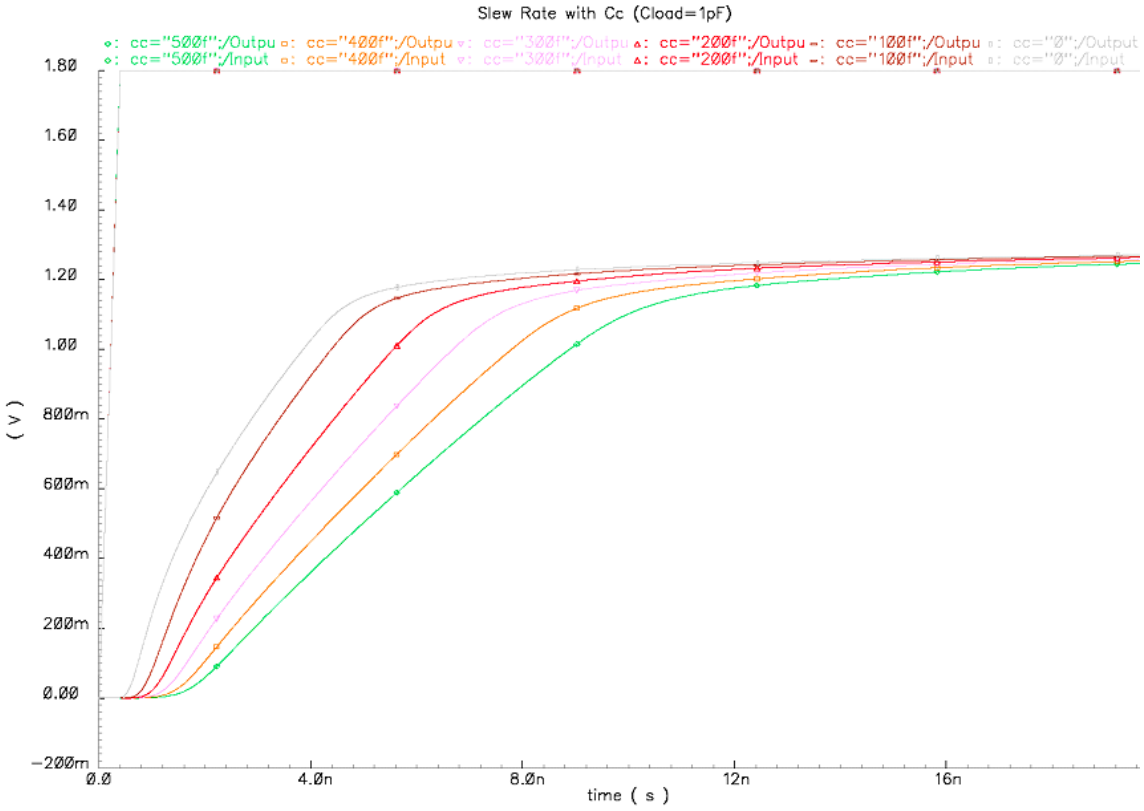

Figure 3.8: Slew rate with compensation capacitance C_C variation

3.2 Gm Cell

There are several architectures described in [Sanchez S.E.2000], [Johns Martin1997] with comparison. To allow filter operation at frequencies into the hundreds of MHz, cascode of multiple stages must be avoided. Thus, no interstage node means no parasitic pole. However, without cascoding, low-frequency transconductor gain is limited to that of a single gain stage. But, it can be improved by using negative resistance in parallel with single stage output resistance. This dissertation will discuss on cascode-free transconductor using positive feedback [Toumazou C. et al.2002] which is also identical in [Nauta B. 1993] as shown in Fig. 3.9. A single Gm cell consists of 6 standard CMOS logic inverters while each individual transconductors are identical to an inverter as shown in Fig. 3.10. This design is using fully differential structure, which implies that only the difference in voltage between inverter 1 and inverter 2 will be processed. Therefore, any noise which is common to both inverters will not affect the differential signal. Moreover, the differential signal will have only odd-order distortion.