DESIGN AND ANALYSIS OF CMOS BASED RFIC VOLTAGE CONTROLLED OSCILLAOTR (VCO) FOR 1.9GHZ RANGE CDMA APPLICATIONS

Oleh

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ABSTRACT

The objective of this paper is to present the Design and Analysis of CMOS Based RFIC Voltage Controlled Oscillator (VCO) for 1.9GHz Range for CDMA Application. The topology used to realize the oscillator is the Cross coupled differential LC tank negative trans-conductance voltage controlled oscillator. The design process begins from the choice of topology. After a topology is chosen, then the targeted specification is set. The circuit is simulated and optimized to meet the specifications. This is done in the schematic and simulation entry. After the simulation results are satisfied, and then the layout of the circuit is drawn. In the layout stage, design rules check (DRC) should always performed to make sure the layout follow the design rules. After DRC checking, the layout versus schematic (LVS) is performed to compare between schematic net list file and layout net list file. The final stage will be the additional of the bond pad into the layout. In chapter 1 of this paper, an introduction to transceiver architecture and Voltage controlled oscillator is given. The various topology described in the previous published paper to implement a Voltage Controlled Oscillator is compared between each other in Chapter 2. In chapter 3, the analysis of the Cross coupled differential LC tank negative trans-conductance topology used in the design of this paper is described. Chapter 4 discusses about the Phase Noise of the oscillator. The designed circuit is simulated using Cadence CAD tools and the design kit is supplied by Silterra Malaysia Sdn. Bhd (Silterra RF design kit, version 180804). The simulation results analysis are shown in chapter 5. The layout process is described in chapter 6 and finally chapter 7 gives the conclusion of the project.

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CHAPTER 1 – INTRODUCTION

1.1 Introduction to CDMA

1.11 What is CDMA?

Code Division Multiple Access, a cellular technology originally known as IS-95, competes with GSM technology for dominance in the cellular world [*Leon Perlman, Cellular Online*]. There are now different variations, but the original CDMA is now known as cdmaOne. Now we have cdma2000 and its variants like 1X EV, 1XEV-DO, and MC 3X. They refer to variants of usage of a 1.25MHz bandwidth channel, 3X uses a 5MHz bandwidth per channel.

Wideband CDMA (WCDMA) that forms the basis of UMTS 3G networks, developed originally by Qualcomm, CDMA is characterized by high capacity and small cell radius, employing spread-spectrum technology and a special coding scheme.

Developed originally by Qualcomm and enhanced by Ericsson, CDMA is characterized by high capacity and small cell radius, employing spread-spectrum technology and a special coding scheme.

CDMA was adopted by the Telecommunications Industry Association (TIA) in 1993. In September 1009, only three years after the first commercial deployment, there were 16 million subscribers on cdmaOne systems worldwide. By May 2001 there were 35 million subscribers on cdmaOne systems worldwide and there are now 60 million. Over 35 countries have either commercial or trial activity ongoing. There are already 43 Wireless Local Loop (WLL) systems in 22 countries using cdmaOne technology.

Enhancing today's data capabilities is the 1XRTT CDMA standard – this next evolutionary step for cdmaOne operators will provide data rates up to 300kbps, significant capacity increases as well as extended battery life for handsets.

Worldwide resources are being devoted to roll out third-generation CDMA technology, including Multi- Carrier (cdma2000 1xMC and HDR in 1.25MHz bandwidth, and 3xMC in 5MHz bandwidth), and Direct Spread (WCDMA in 5MHz bandwidth).

Qualcomm owns a substantial portfolio of CDMA patents, including many “essential” patents that are necessary for the deployment of any proposed 3G CDMA system, such as Multi-Carrier, Direct Spread, and another system referred to as TD-SCDMA.

Qualcomm has now granted royalty bearing licenses to more than 75 manufacturers for CDMA and, as part of these licenses, has transferred technology and know-how in assisting these companies to develop and deploy CDMA products.

1.12 CDMA Technology – Spread Spectrum

CDMA is a "spread spectrum" technology, which means that it spreads the information contained in a particular signal of interest over a much greater bandwidth than the original signal [*Mobile Communication*].

A CDMA call starts with a standard rate of 9600 bits per second (9.6 kilobits per second). This is then spread to a transmitted rate of about 1.23 Megabits per second. Spreading means that digital codes are applied to the data bits associated with users in a cell. These data bits are transmitted along with the signals of all the other users in that cell. When the signal is received, the codes are removed from the desired signal, separating the users and returning the call to a rate of 9600 bps.

Traditional uses of spread spectrum are in military operations. Because of the wide bandwidth of a spread spectrum signal, it is very difficult to jam, difficult to interfere with, and difficult to identify. This is in contrast to technologies using a narrower bandwidth of frequencies. Since a wide and spread spectrum signal is very hard to detect, it appears as nothing more than a slight rise in the "noise floor" or interference

level. With other technologies, the power of the signal is concentrated in a narrower band, which makes it easier to detect. Increased privacy is inherent in CDMA technology. CDMA phone calls will be secure from the casual eavesdropper since, unlike an analog conversation, a simple radio receiver will not be able to pick individual digital conversations out of the overall RF radiation in a frequency band.

1.13 Benefits from CDMA

When implemented in a cellular telephone system, CDMA technology offers numerous benefits to the cellular operators and their subscribers. The following is an overview of the benefits of CDMA [*Mobile Communication*].

1. Capacity increases of 8 to 10 times that of an AMPS analog system and 4 to 5 times that of a GSM system
2. Improved call quality, with better and more consistent sound as compared to AMPS systems
3. The use of same frequency in every sector of every cell simplified system planning
4. Enhanced privacy
5. Improved coverage characteristics, allowing for the possibility of fewer cell sites
6. Increased talk time for portables
7. Bandwidth on demand

1.2 Introduction to Receiver

1.21 Receiver Architecture

In the design of architecture of the front-end receiver, there exist two broad categories of receivers, which are, IF and zero IF. In common terms, these are known as heterodyne and homodyne receivers, respectively. As the radio front-ends continue to evolve toward more on-chip integration, IF frequency continues to decrease, giving rise to different architecture: High IF, very low IF and zero IF. These are broadly categorized under heterodyne and homodyne architecture depending on the frequency planning.

The heterodyne receiver topologies are well known and widely utilized for current wireless applications. In such topologies, the input RF signal is down-converted to an intermediate frequency (IF) where it is amplified and filtered before the final demodulation by a low-frequency demodulator.

The designed of VCO is based on the super-heterodyne architecture of receiver.

1.22 Super-Heterodyne Receiver

In telecommunication, to heterodyne is to generate new frequencies by mixing two or more signals in a nonlinear device such as a vacuum tube, transistor, or diode mixer. The mixing of each two frequencies results in the creation of two new frequencies, one at the sum of the two frequencies mixed, and the other at their difference. A low frequency produced in this manner is sometimes referred to as a beat frequency. A beat frequency or “beating” can be heard for example when multiple engines of an aircraft are running at close but not identical speeds.

Heterodyne is the name of the tones or new frequencies that come from mixing two signals, and super comes from the fact that these frequencies are above the audible spectrum. Normally the heterodyne architecture will generates either the frequency above the carrier frequency of below the carrier frequency, in super-heterodyne architecture, the generated intermediate frequency is below the carrier frequency.

The super-heterodyne receiver was invented by Edwin Armstrong in 1918. This architecture’s principle as used in radio receivers allows certain obstacles to high performance radio design to be overcome. The conventional receiver which was **Tuned Radio Frequency (TRF)** receivers suffered from poor frequency stability, and poor selectivity, as even filters with a high Q factor have a wide bandwidth at radio frequencies.

In radio using the Super-heterodyne principle, all signal frequencies are converted typically to a constant lower frequency before detection. This constant frequency is called the **Intermediate Frequency (IF)**.

Super receivers "beat" or **heterodyne** a frequency from a local oscillator with the incoming signal. The user tunes the radio by adjusting the set's oscillator frequency and/or the tuning of the incoming signals. This heterodyning results in a higher and a lower frequency than that of the incoming frequency. Either the higher or the lower is chosen as the IF, which is amplified and then demodulated (reduced to just audio frequencies through a speaker).

Almost all receivers in use today utilize this method. The diagram below shows the basic elements of a single conversion super-heterodyne receiver. In practice not every design will have all these elements, but the essential elements of a local oscillator and a mixer followed by a filter and IF amplifier are common to all super-heterodyne circuits.

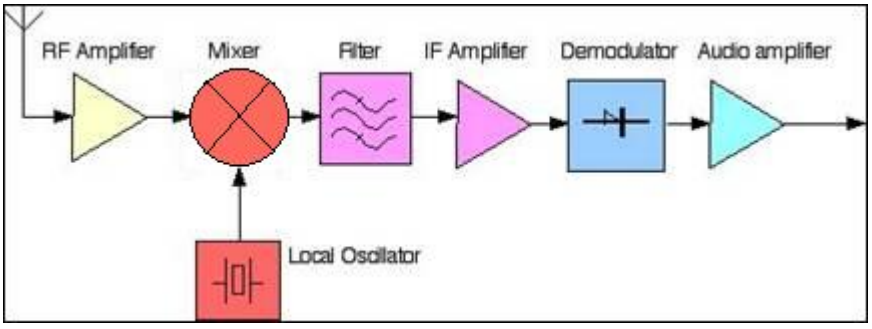

Fig 1.1 Super-heterodyne Architecture of Receiver

The advantage to this method is that most of the radio's signal path has to be sensitive to only a narrow range of frequencies. Only the front end (the part before the frequency converter stage) needs to be sensitive to a wide frequency range. For example, the front end might need to be sensitive to let's say in our design, 1.9G Hz, while the rest of the radio might need to be sensitive only to 80MHz, the typical IF frequency.

Sometimes, to overcome obstacles such as image response, more than one IF is used. In such a case, two frequency converters would be used, and the radio would be a "**Double Conversion Super-heterodyne**".

Super-heterodyne receivers have superior characteristics in both frequency stability and selectivity. It is much easier to stabilize an oscillator than a filter, especially with modem frequency synthesizer technology, and IF filters can give much narrower pass bands at the same Q factor than an equivalent RF filter. A fixed IF also allows the use of a crystal filter in very critical designs such as radiotelephone receivers which have exceptionally high selectivity.

1.3 Introduction to Oscillator

1.31 Definition of Oscillator

In simple terms, an oscillator is an amplifier where sufficient energy is coupled back from the output to the input to become unstable and start oscillating. The output port then provides the wanted output power into the load and the overall circuit configuration determines the frequency stability and sensitivity to load changes.

1.32 Oscillator Classification

Oscillators come in a variety of different types, but perhaps the two major classifications are those that directly sinusoidal outputs as opposed to those with square (or triangular) wave outputs [*David John, 1997*]. Sinusoidal outputs oscillator are usually realized using some kind of frequency-selective or tuned circuit in a feedback configuration, whereas square-wave-output oscillator are usually realized using a nonlinear feedback circuit such as a relaxation oscillator or a ring oscillator. Sinusoidal oscillators realized using tuned circuits can be further classified into RC circuits, switched-capacitor circuits, LC circuits and crystal oscillator. *Fig 1.2* shows the classification of oscillators.

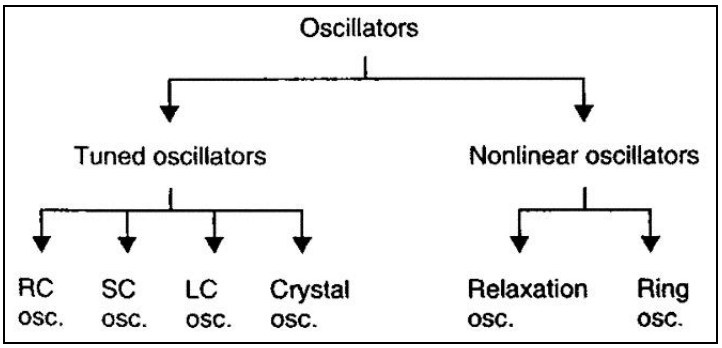

Fig 1.2 Classification of Oscillators [David John, 1997]

1.33 Voltage Controlled Oscillator

In telecommunication, VCO is a principal part of the Phase Locked Loop, PLL. It determines the overall performance of PLL system, such as the operating frequency range, FM distortion, center frequency drift and center frequency.

The first step in building a Voltage Controlled Oscillator (VCO) is to realize an oscillator and then add a means whereby its frequency of oscillation can be controlled by an input voltage.

1.34 Oscillation Principle

An oscillator generates a periodic output. As such, the circuit must entail a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. Most RF oscillator can be viewed as feedback circuit. Consider the simple linear feedback system depicted in *Fig 1.3*, with the overall transfer function

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1-H(s)} \quad \text{..... (1.1)}$$

A self-sustaining mechanism arises at the frequency s0 if $H(s_0) = +1$, and the oscillation amplitude remains constant if s_0 is purely imaginary, i.e., $H(s_0=jw_0) = +1$. Thus, for steady oscillation, two conditions must be simultaneously met at w_0, called Barkhausen's criteria [*Behzad Razavi, 1998*]:

1. The loop gain, $|H(jw_0)|$ = unity

2. the total phase shift around the loop, $L\ H(jw_0)$ = zero (or 180°if the dc feedback is negative)

The above conditions imply that any feedback system can oscillate if its loop gain and phase shift are chosen properly. In most RF oscillators, a frequency-selective network, also called a resonator (e.g. an LC tank) is included in the loop so as to stabilize the frequency. This is illustrated conceptually in *Fig 1 .3*.

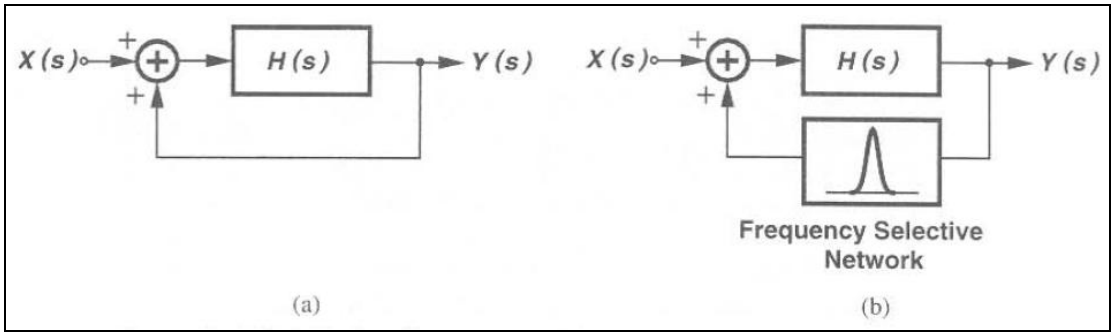

Fig 1.3 (a) Feedback oscillation system, (b) addition of frequency-selective network to (a)

[Behzad Razavi, 1998]

The nominal frequency of oscillation is usually determined by the properties of the circuits, e.g. the resonance frequency of the LC tank in *Fig 1.4(c)*. The self-sustaining effect allows the circuit's noise to grow initially, but another mechanism is necessary to limit the growth at some point. From other point of view, to ensure oscillation start-up, the small signal loop gain must be somewhat greater than one, but to achieve stable amplitude, the "average" loop gain must return to unity.

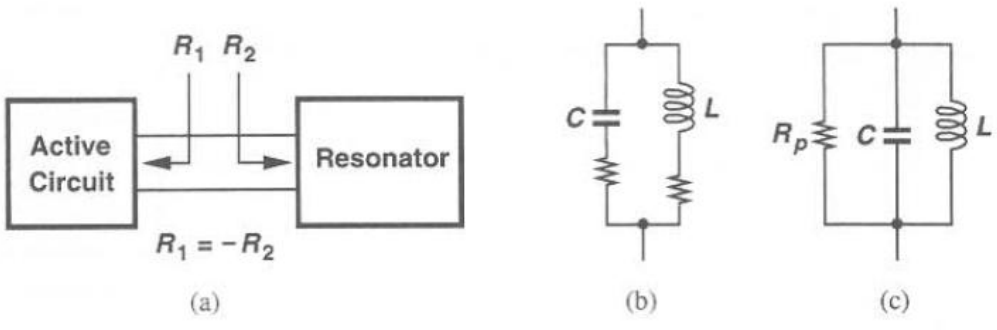

Fig 1.4 (a) One port view of oscillator, (b) LC resonator, (c), equivalent circuit of (b)

[Behzad Razavi, 1998]

CHAPTER 2 – VOLTAGE CONTROLLED OSCILLATOR TOPOLOGY

2.1 LC Oscillator

Negative conductance voltage controlled oscillators are by far the most widely used VCO structures in GHz range designs. The simplicity of the structure that allows the generation of a differential negative conductance with only two transistors in the signal path makes the circuit very attractive for applications where low noise with low power consumption at GHz range are key performance metrics. [*Filkret Dulger, 2001*]

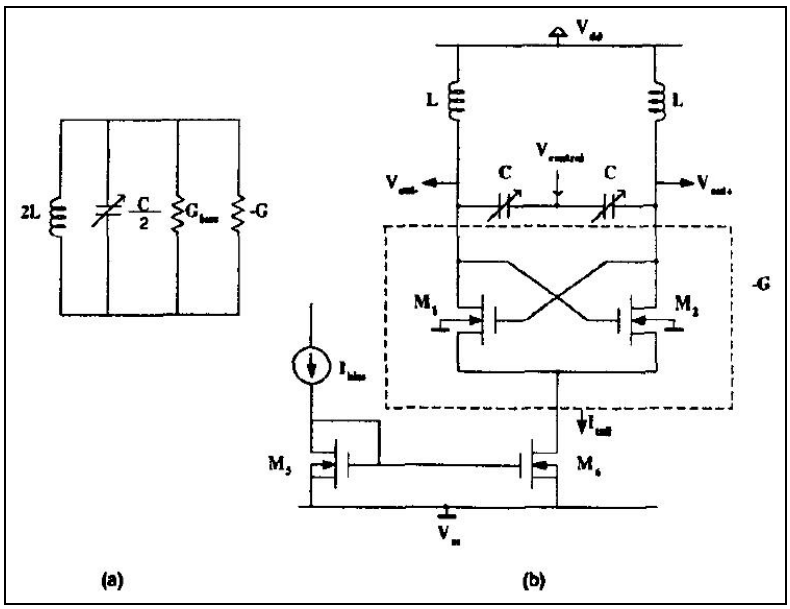

Fig 2.1 Negative conductance Voltage Controlled Oscillator (a) concept, (b) circuit implementation

[*Filkret Dulger, 2001*]

The basic negative conductance VCO is depicted conceptually in *Fig 2.1(a).* The inductor and the variable capacitor form the resonator tank, and the conductance Gloss represents the loss due to the finite quality factor of the resonator. The negative conductance is denoted as *–G* in the illustration. A sample circuit implementation in CMOS is shown in *Fig 2.1(b)* where the differential oscillator is built with symmetry around the resonator tank. The negative conductance *–G* generated by the cross coupled

NMOS transistors M_1 and M_2 is designed to compensate for the loss associated with the LC tank. It can be shown that the negative-conductance seen differentially at the drain of the NMOS transistors is $-G = I\, g_m/2$, where gm denotes the trans-conductance of each transistor. In order for the oscillations to be sustained in the circuit, the tail current of the cross coupled transistor pair should be increased to a level high enough for the negative conductance to be larger in absolute value than the equivalent loss of the tank.

2.2 Relaxation Oscillator

Relaxation oscillator is one of the solutions for generating square-wave outputs. A relaxation oscillator circuit is a repeating circuit which achieves its repetitive behavior from charging and discharging a capacitor. Its repetition time is depends on the recharge time. In this case, the oscillation frequency will be depending on the time constant of the capacitor. Example of relaxation oscillator is op-amp relaxation oscillator, unijunction transistor relaxation oscillator, capacitance multiplier, etc.

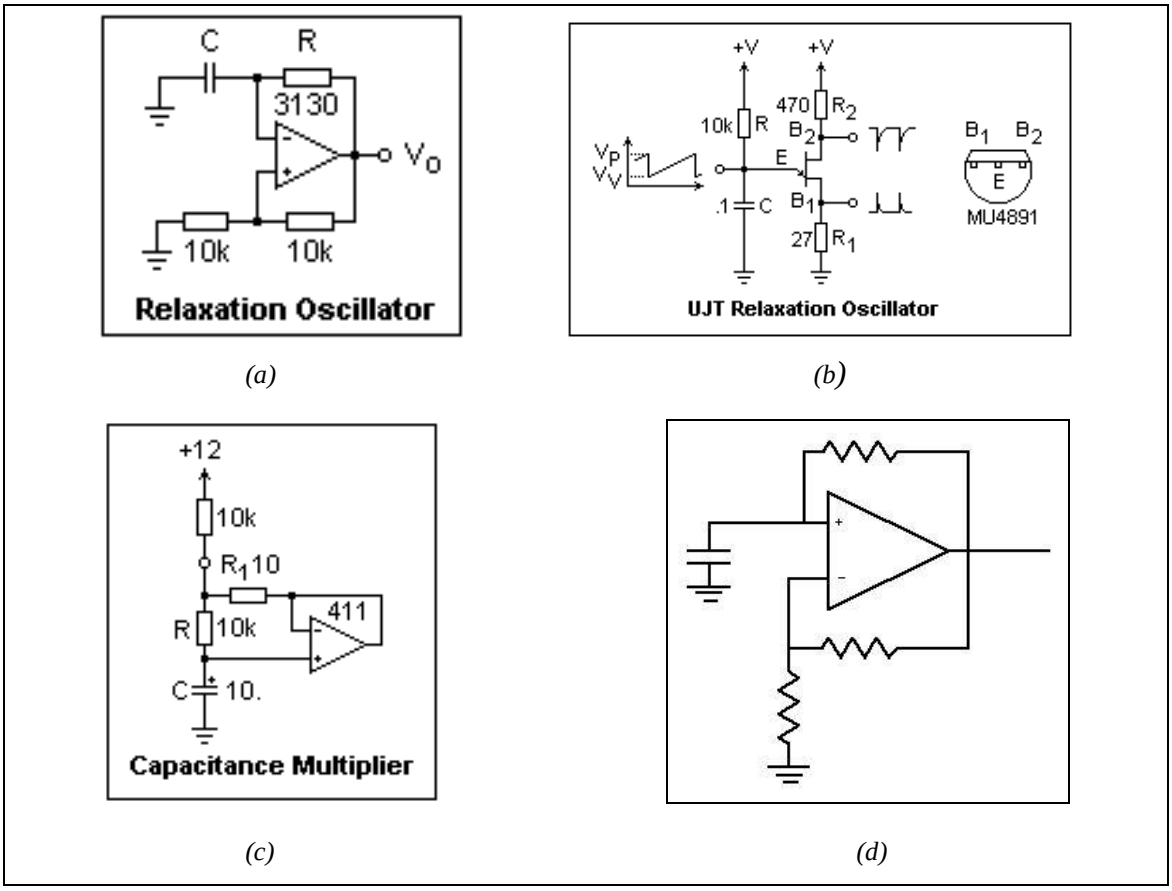

Fig 2.2 Relaxation Oscillator

In basic relaxation oscillator using op-amp, the principle is the uses of positive feedback to drive the op amp to its rails. *Fig 2.2 (d)* shows the basic relaxation oscillator realized using op-amp. The capacitor's charging moves the non-inverting voltage past the threshold value and thus causes the device to switch states, mean causing the oscillation to occur.

To make the switching voltage is half of the rail, the value of R is set to equal to R_g. The oscillation frequency is depends on the time constant for charging the capacitor.

The major draw back of the op-amp relaxation oscillator is the low operation frequency. When operating in high frequency (in the GHz range), the op-amp become unstable. Besides, the low *Q* and low immunity to noise characteristics causes the relaxation oscillator is not popular in RFIC. Thus, in this design of the VCO, the relaxation oscillator using op-amp is not suitable to be chosen.

2.3 Ring Oscillator

Another non-linear oscillator, the ring oscillator is realized by placing an odd number of open-loop inverting amplifiers in a feedback loop [*David Johns*]. The simplest type of amplifier that can be used is a simple digital inverter, as shown in *Fig 2.3*.

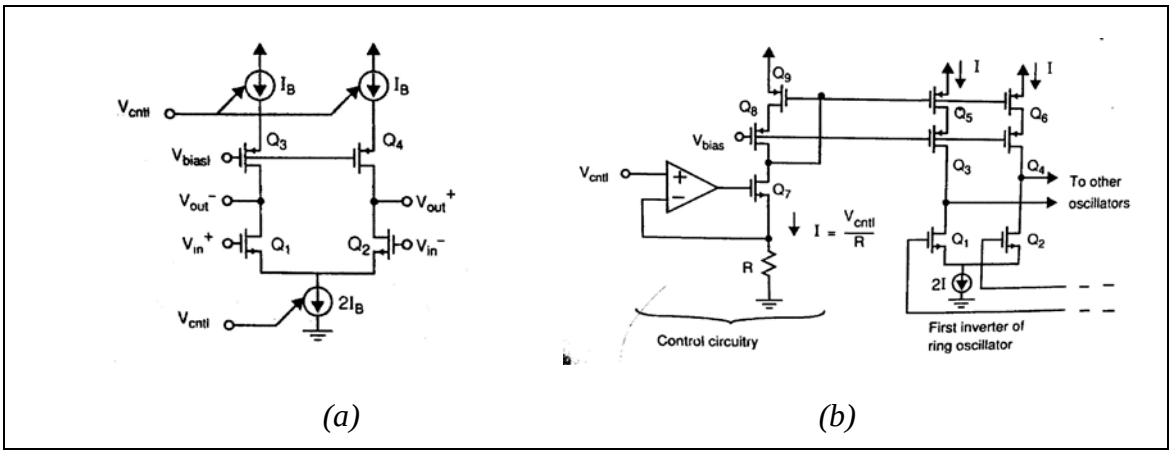

Fig 2.3 (a) Fully integrated inverter with a programmable delay (b) circuit that can be used to realize the voltage-controlled current sources [*David Johns*]

This circuit is a form of negative feedback, but since each inverter has approximately 90°phase shift at its unity-gain frequency, it is guaranteed that the loop gain will still be greater than unity when the phase shift around the loop becomes greater than 180°. As a result, the circuit is unstable and oscillations occur. The oscillation frequency is given by

$$f_{osc} = \frac{1}{T} \quad \text{where} \quad \frac{T}{2} = n\tau_{inv} \quad \ldots\ldots\ldots (2.1)$$

In CMOS technology, the ordinary CMOS inverters which using a NMOS and PMOS can not be used. This avoidance is because ordinary CMOS inverters have a gate-threshold voltage proportional to the power supply voltage. Thus, when the power supply increases in voltage, the voltage excursions increase in voltage proportionally, the currents of the inverters increase in proportion to the square of the power-supply voltages. *Fig 2.3* shows the circuit of the VCO utilizing ring oscillator method.

2.4 Spiral Type Inductor

A calculation approach to estimate the inductance for planar spiral inductor has been introduced [Sunderarajan S. Mohan, 1999]. Three simple, approximate expressions for spiral inductors of square, hexagonal, octagonal and circular geometries have been presented. The first expression, called the modified Wheeler obtained by modifying an expression that Wheeler obtained for discrete inductors. This expression is simple and gives very good accuracy. The second expression is derived from electromagnetic principles by approximating the slides of the spiral by current sheets with uniform current distribution. This expression is intuitive and similar in form to inductance expressions for more conventional elements such as coaxial transmission lines and parallel wire transmission lines. The third expression is obtained by data-fitting techniques. Although it lacks the physically intuitive derivation of the other two approximations, it is very well suited for optimization of circuits using geometric programming.

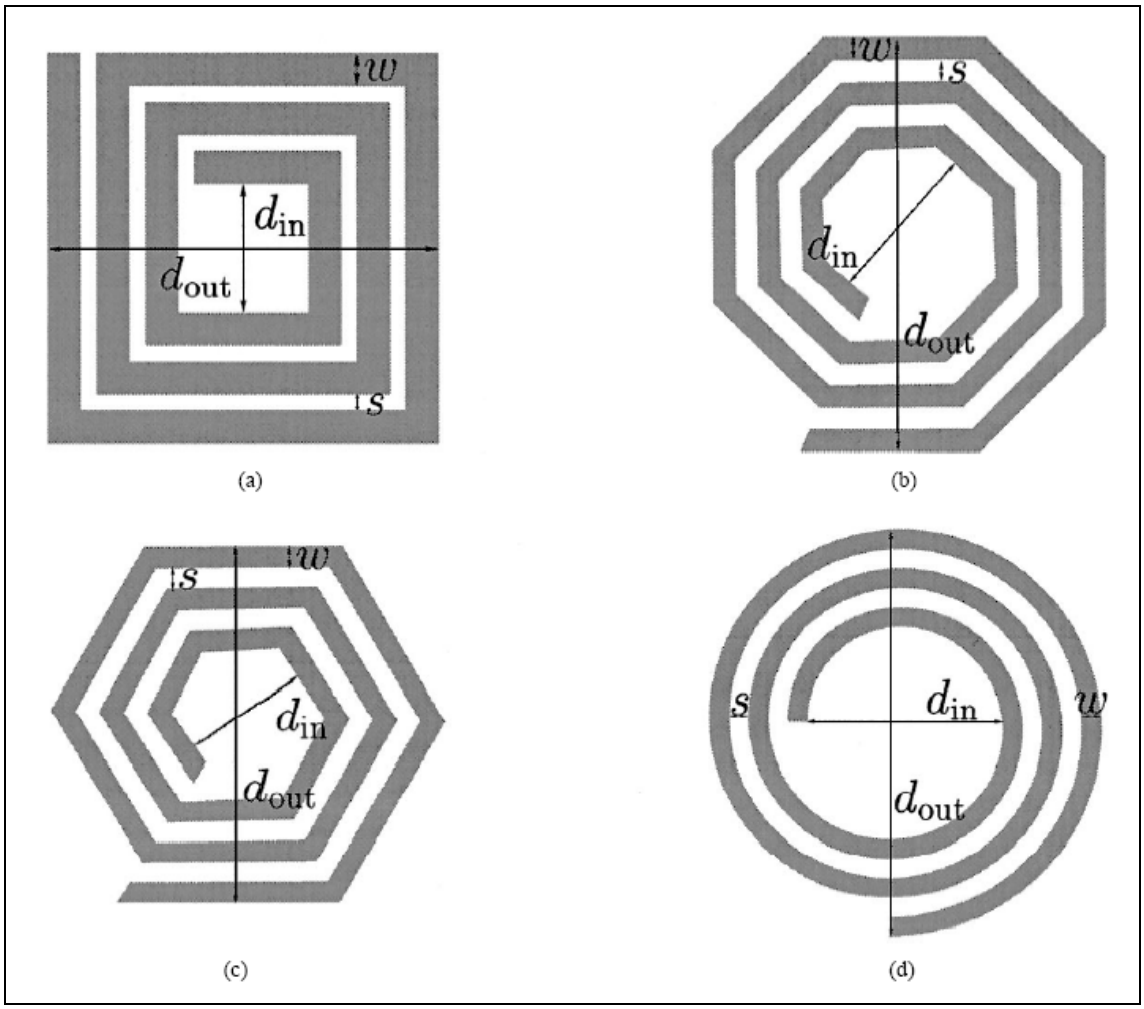

Fig 2.4 On chip inductor realizations: (a) square, (b) hexagonal, (c) octagonal, and (d) circular [Sunderarajan S. Mohan,1999]

2.4.1 Modified Wheeler Formula

Wheeler presented several formulas for planar spiral inductors, which were intended for discrete inductors. Sunderajan S. Mohan has found that a simple modification of the original Wheeler formula allows us to obtain an expression that is valid for planar spiral integrated inductors.

$$L_{mw} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \qquad \text{.... (2.2)}$$

where ρ is the fill ratio defined previously. The coefficients K_1 and K_2 are layout dependent and are shown in Table 2.1. The ratio ρ represents how hollow the inductor

is: for small ρ we have a hollow inductor ($d_{out} \approx d_{in}$) and for a large ρ we havea full inductor ($d_{out} >> d_{in}$). Two inductors with the same average diameter but different fill ratios will, of course, have different inductance values. The full one has a smaller inductance because its inner turns are closer to the center of the spiral and so contribute less positive mutual inductance and more negative mutual inductance.

Table 2.1 Coefficients for Modified Wheeler Expression

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

2.4.2 Expression Based on Current Sheet Approximation

Another simple and accurate expression for the inductance of a planar spiral can be obtained by approximating the sides of the spirals by symmetrical current sheets of equivalent current densities. For example, in the case of the square, we obtain four identical current sheets. The current sheets on opposite sides are parallel to one another, whereas the adjacent ones are orthogonal. Using symmetry and the fact that sheets with orthogonal current sheets have zero mutual inductance, the computation of the inductance is now reduced to evaluating the self-inductance of one sheet and the mutual inductance between opposite current sheets. These self and mutual inductances are evaluated using the concepts of geometric mean distance (GMD), arithmetic mean distance (AMD), and arithmetic mean square distance (AMSD). The resulting expression is

$$L_{gmd} = \frac{\mu n^2 d_{avg} c_1}{2}\left(\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right) \quad \text{..... (2.3)}$$

Where the coefficients, C_i are layout dependent and are shown in Table 2.2. Although the accuracy of this expression worsens as the ratio s/w becomes large, it exhibits a maximum error of 8% for $s \le 3w$. Note that typical practical integrated spiral inductors are built with $s \le w$. The reason is that a smaller spacing improves the interwinding

magnetic coupling and reduces the area consumed by the spiral. A large spacing is only desired to reduce the interwinding capacitance. In practice, this is not a concern as this capacitance is dwarfed by the underpass capacitance.

Table 2.2 Coefficients for Current Sheet Expression

Layout	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

2.4.3 Data Fitted Monomial Expression

The final expression is based on a data fitting technique, which yielded the expression

$$L_{mon} = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \quad \ldots. (2.4)$$

Where the coefficients β and α_i are layout dependent and given in Table 2.3. The expression in (2.4) is called a monomial in the variables d_{out}, w, d_{avg}, n and s. The coefficients were obtained as follows. First change variables to use the logarithms of the variables: $x_1 = \log d_{out}$, $x_2 = \log w$, $x_3 = \log d_{avg}$, $x_4 = \log n$, $x_5 = \log n$. Taking the logarithm of the inductance as well we can express the monomial relation (2.4) as

$$y = \log L = \alpha_0 + \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4 + \alpha_5 x_5 \quad \ldots. (2.5)$$

Where $\alpha_0 = \log \beta$. This is linear-plus-constant model of y as a function of x, and is easily fit by carious regression or data-fitting techniques. To develop our models we used a simple least-squares fit: we chose α_i to minimize

$$\sum_{k=1}^{N} \left(y^{(k)} - \alpha_0 - \alpha_1 x_1^{(k)} - \alpha_2 x_2^{(k)} - \alpha_3 x_3^{(k)} - \alpha_4 x_4^{(k)} - \alpha_5 x_5^{(k)} \right)^2 \quad \ldots.(2.6)$$

Where the sum is over our family of inductors (so $N \approx 19000$). It is also possible to use more sophisticated date-fitting techniques, e.g. one which minimizes the maximum error of the fit, or one in which the coefficients must satisfy given inequalities or bounds.

Since the monomial expression L_{mon} is developed from our library of inductors, it is important to check that it has predictive ability as well, by checking its error on inductors not in the library. Such tests reveal that the fit for such inductors is as good as the fit for the ones in the family from which the model was developed. This is hardly surprising since the fitting method compresses 19 000 numbers (i.e., the inductances) to six (i.e., the monomial coefficients), and so is not prone to “over-fitting.”

The monomial expression is useful since, like the other expressions, it is very accurate and very simple. Its real use, however, is that it can be used for optimal design of inductors and circuits containing inductors, using geometric programming, which is a type of optimization problem that uses monomial models.

CHAPTER 3 – ANALYSIS OF CROSS COUPLED DIFFERENTIAL LC TANK VOLTAGE CONTROLLED OSCILLATOR

3.1 Period Calculation method of LC tank

The conventional technique of the effective capacitance calculation is quite complex and inaccurate through the Fourier series of the varactors and oscillating voltage. In this section, a newer technique, Period calculation method is introduced [*ZhangWen Tang, 2004*]. This technique derives the period of oscillating waveform directly and then predicts the oscillator tuning curve in time domain.

The varactors used in the designed LC tank VCO is Accumulation MOS varactor (AMOS), which are step-like capacitors and have large nonlinearity. *Fig 3.1* shows the serial LC tank representing the varator and the step-like capacitor characteristic of AMOS varators.

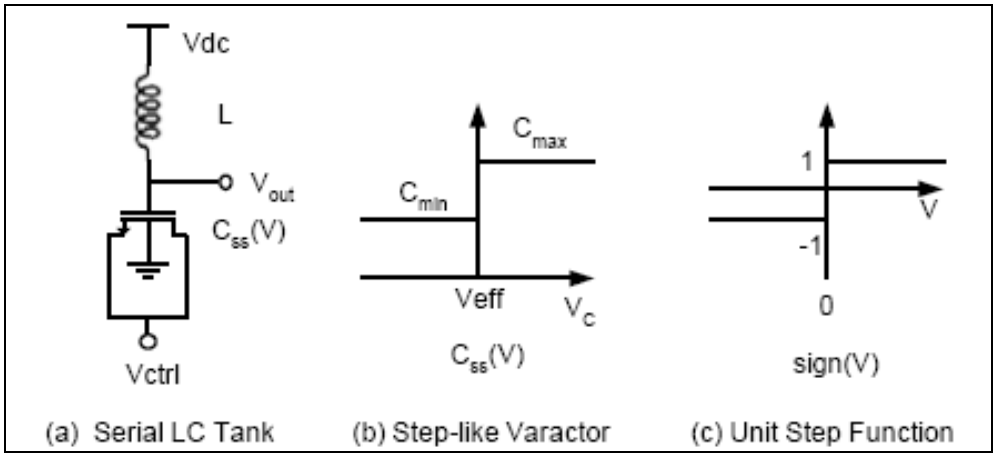

Fig 3.1 (a) Serial LC Tank, (b) Step-like varactor, (c) Unit step function

The small-signal capacitance is given by

$$C_{ss}(V) = \begin{cases} C_{max} & V > V_{eff} \\ C_{min} & V < V_{eff} \end{cases} \quad \ldots\ldots\ldots\ldots(3.1)$$

where $V_{eff} = V_G - V_{ctrl} - V_{TH}$ is the effective control voltage (ECV).

The half circuit of LC tank VCO is a serial LC tank shown in *Fig 3.1(a)*. The step like varactor can also be mathematically represented as below,

$$C_{ss}(V) = \frac{1}{2}(C_{\max} + C_{\min}) - \frac{1}{2}(C_{\max} - C_{\min}) \pm (V - V_{eff}) \qquad \ldots\ldots\ldots\ldots(3.2)$$

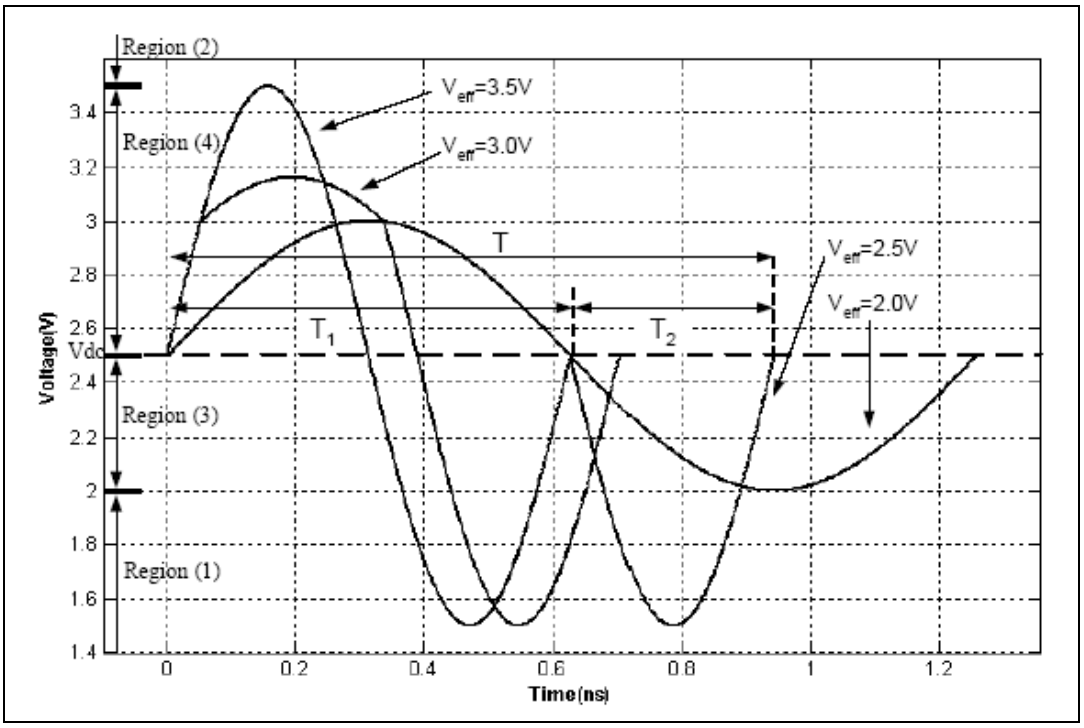

Fig 3.2 Voltage waveform of a varator at different ECV

Fig 3.2 shows the oscillating voltage waveforms of the serial LC tank. Each waveform consists of two segmental sinusoids with different size, which join at the ECV. With the ECV from low to high, there exists 4 regions as below :

1). When $V_{eff} \leq V_{dc} - A_{min}$, the oscillating waveform is a sinusoid with the minimum amplitude A_{min} and minimum frequency ω_{min};

2). When $V_{eff} \geq V_{dc} + A_{max}$, the oscillating waveform is a sinusoid with a maximum amplitude A_{max} and maximum frequency ω_{max};

3). When , $V_{dc} - A_{min} \leq V_{eff} \leq V_{dc}$ 2 partial sinusoids join at ECV. One is over V_{eff} with the amplitude A_{min} and frequency ω_{min}; the other is below with the amplitude $\theta_1 A_{max}$ (θ_1 is an ellipse similar factor, ESF) and frequency ω_{max}.

4). When , $V_{dc} \le V_{eff} \le V_{dc} + A_{max}$ two partial sinusoids join at ECV. One is over V_{eff} with the amplitude A_{min} and frequency ω_{min}; the other is below with the amplitude $\theta_2 A_{max}$ (θ_2 is another ESF) and frequency ω_{max}.

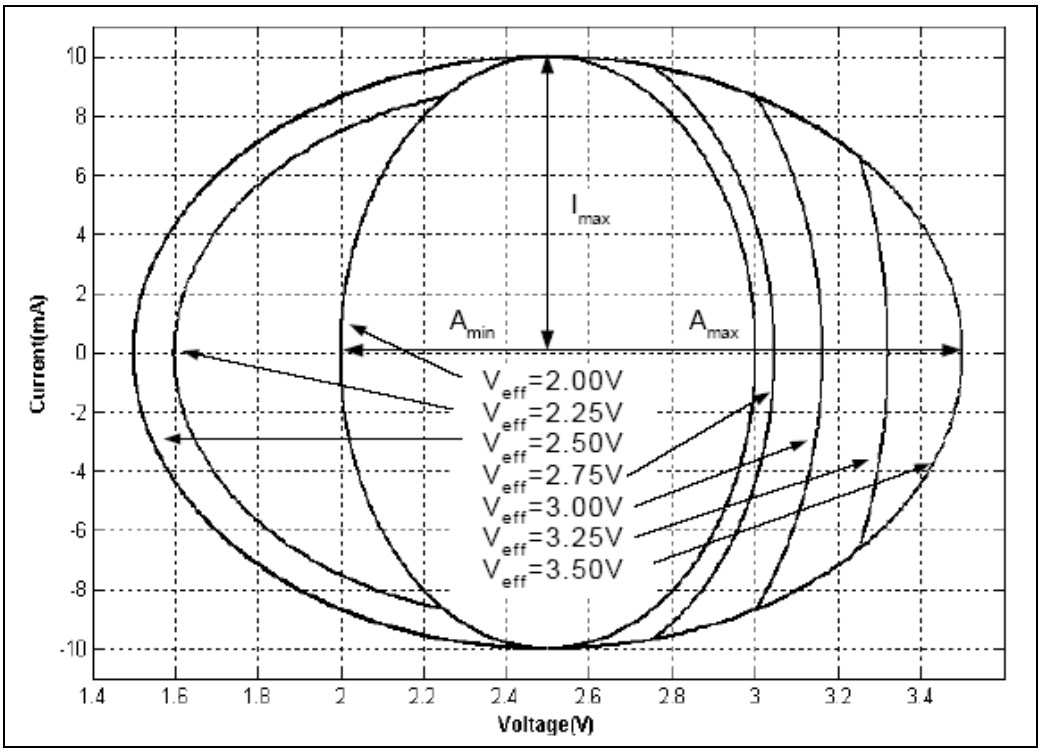

Fig 3.3 I-V locus of a varactor

The I-V locus of a step-like varactor in the serial LC tank is shown in *Fig 3.3*. It consists of two ellipses with different size joined at the ECV. The above 4 regions satisfy the following ellipses' equations:

1). When $V_{eff} \le V_{dc} - A_{min}$, the I-V locus holds

$$\left(\frac{V - V_{dc}}{A_{\min}}\right)^2 + \left(\frac{I}{\omega_{\min} C_{\max} A_{\min}}\right)^2 = 1 \qquad \text{……..(3.3)}$$

2). When $V_{eff} \ge V_{dc} + A_{max}$, the I-V locus holds

$$\left(\frac{V - V_{dc}}{A_{\max}}\right)^2 + \left(\frac{I}{\omega_{\max} C_{\min} A_{\max}}\right)^2 = 1 \qquad \text{……..(3.4)}$$

3). When $V_{dc} - A_{min} \le V_{eff} \le V_{dc}$, two segmental sinusoids respectively hold

$$\left(\frac{V - V_{dc}}{A_{\min}}\right)^2 + \left(\frac{I}{\omega_{\min} C_{\max} A_{\min}}\right)^2 = 1, \qquad \text{for V} \ge V_{eff}$$

$$\left(\frac{V - V_{dc}}{A_{\max}}\right)^2 + \left(\frac{I}{\omega_{\max} C_{\min} A_{\max}}\right)^2 = \theta_1^{\,2}, \qquad \text{for V} \le V_{eff}; \quad \text{.....(3.5)}$$

where the ESF θ_1 satisfies $\frac{A_{\min}}{A_{\max}} \le \theta_1 \le 1$.

Especially when $V_{eff} = V_{dc}$ and $\theta_1 = 1$, it satisfies

$$I_{\max} = \omega_{\min} C_{\max} A_{\min} = \omega_{\max} C_{\min} A_{\max} \qquad \text{.....(3.6)}$$

where I_{max} is the maximum current in the inductor or varactor.

4). When $V_{dc} \le V_{eff} \le V_{dc} + A_{max}$, two segmental sinusoids hold respectively

$$\left(\frac{V - V_{dc}}{A_{\min}}\right)^2 + \left(\frac{I}{\omega_{\min} C_{\max} A_{\min}}\right)^2 = \theta_2^{\,2}, \quad \text{for V} \ge V_{eff}$$

$$\left(\frac{V - V_{dc}}{A_{\max}}\right)^2 + \left(\frac{I}{\omega_{\max} C_{\min} A_{\max}}\right)^2 = 1, \quad \text{for V} \le V_{eff}; \quad \text{.....(3.7)}$$

where the ESF θ_2 satisfies $1 \le \theta_2 \le \frac{A_{\max}}{A_{\min}}$.

Then, the oscillating periods in the above 4 regions can be calculated mathematically.

1). When $V_{eff} \le V_{dc} - A_{min}$, the oscillating period is

$$T = T_{\max} = 2\pi\sqrt{LC_{\max}} \qquad \text{.....(3.8)}$$

2). When $V_{eff} \ge V_{dc} + A_{max}$, the oscillating period is

$$T = T_{\min} = 2\pi\sqrt{LC_{\min}} \qquad \text{.....(3.9)}$$

3). When V_{dc} - A_{min} ≤ V_{eff} ≤ V_{dc}, the oscillating period is a sum of two intervals $T = T_1 + T_2$,shown in *Fig 3.2*. T_1 is the time on the first ellipse; T_2 is the time on the second ellipse. At the ECV, the voltage and current of the varactor are V_{eff} and I_{eff}. From (3.6),(3.8) and (3.9), we obtain the amplitude ratio

$$\frac{A_{\max}}{A_{\min}} = \sqrt{\frac{C_{\max}}{C_{\min}}} \qquad \text{……..…..(3.10)}$$

Substituting (3.10) in (3.5) leads to the ESF θ_1

$$\theta_1 = \sqrt{1 - \left(\frac{V_{eff} - V_{dc}}{A_{\min}}\right)^2 + \left(\frac{V_{eff} - V_{dc}}{A_{\max}}\right)^2} \qquad \text{……..…..(3.11)}$$

Thus, the oscillating period is

$$T = T_1 + T_2 = \frac{\frac{\pi}{2} + a\sin\left(\frac{\left|V_{eff} - V_{dc}\right|}{A_{\min}}\right)}{\pi} T_{\max} + \frac{\frac{\pi}{2} - a\sin\left(\frac{\left|V_{eff} - V_{dc}\right|}{\theta_1 A_{\max}}\right)}{\pi} T_{\min}$$

$$T = \frac{1}{2}\left(T_{\max} + T_{\min}\right) + \frac{1}{\pi}\left[a\sin\left(\frac{\left|V_{eff} - V_{dc}\right|}{A_{\min}}\right)T_{\max} - a\sin\left(\frac{\left|V_{eff} - V_{dc}\right|}{\theta_1 A_{\max}}\right)T_{\min}\right] \text{….(3.12)}$$

4). When V_{dc} ≤ V_{eff} ≤ V_{dc} + A_{max}, the same as case 3. Solving (3.7), we can obtain the ESF and oscillating period

$$\theta_2 = \sqrt{1 - \left(\frac{V_{eff} - V_{dc}}{A_{\max}}\right)^2 + \left(\frac{V_{eff} - V_{dc}}{A_{\min}}\right)^2} \qquad \text{……..…..(3.13)}$$

$$T = \frac{1}{2}\left(T_{\max} + T_{\min}\right) + \frac{1}{\pi}\left[-a\sin\left(\frac{\left|V_{eff} - V_{dc}\right|}{\theta_2 A_{\min}}\right)T_{\max} + a\sin\left(\frac{\left|V_{eff} - V_{dc}\right|}{A_{\max}}\right)T_{\min}\right] \text{…(3.14)}$$

To validate the above method of oscillating period calculation, a serial LC tank circuit in *Fig 3.1(a)* is simulated in HSPICE by [*ZhanWen Tang, 2004*]. Its parameters are L=10nH, C_{max} = 4pF, C_{min} = 1pF, and A_{min} = 0.5V. In *Fig 3.4*, the cross line is the simulation result and the solid line is the calculation result from (3.12) and (3.14).

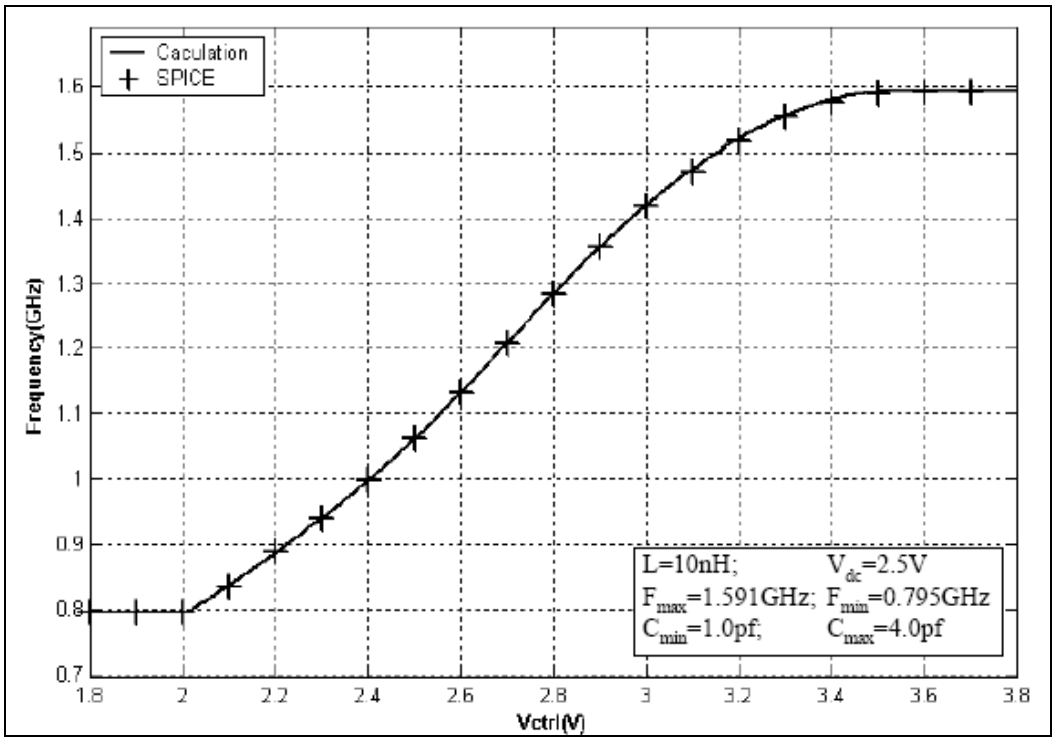

Fig 3.4 Simulation result of [*ZhangWen Tang,2004*].

As the oscillator has a large signal swing (nearly full power supply), the oscillating period is interpolated between T_{max} and T_{min}. The resulting frequency-voltage (F-V) tuning curve, which is shown in *Fig 3.4*, varies linearly with ECV in a range defined by the oscillation amplitude. Although the capacitance-voltage (C-V) characteristic of MOS varactors is step-like, the F-V tuning curve is well linear.

The parameters necessary for the period calculation technique is the maximum and minimum capacitance (C_{max} and C_{min}), inductance L, minimum amplitude A_{min} which is equal to $(4/\pi)I_{bias}R_{eq}$, where R_{eq} is the equivalent parallel resistance of the LC tank. The maximum amplitude A_{max} can be calculated by (10). At different bias current, the tuning curve can be predicted immediately.

CHAPTER 4 – PHASE NOISE

4.1 Introduction to Phase Noise

The major noise of an oscillator is phase noise. Noise injected into an oscillator by its constituent devices or by external means may influence both the frequency and the amplitude of the output signal. In most cases, the disturbance in the amplitude is negligible or unimportant, and only the random deviation of the frequency is considered. The latter can also be viewed as random variation in the period or deviation of the zero crossing points from their ideal position along the time axis.

The equation for a nominally periodic sinusoidal signal is given by,

$$x(t) = A\cos\left[\omega_c t + \phi_n(t)\right] \quad \text{……. (4.1)}$$

where $\phi_n(t)$ is a small random excess phase representing variations in the period. The function $\phi_n(t)$ is called "Phase Noise".

For $|\phi_n(t)| << 1$ rad,

$$x(t) \approx A\cos\omega_c t - A\phi_n(t)\sin\omega_c t \quad \text{……. (4.2)}$$

this mean that the spectrum of $\phi_n(t)$ is translated to $\pm\omega_c$.

In RF applications, phase noise is usually characterized in the frequency domain. For an ideal sinusoidal oscillator operating at ω_c, the spectrum assumes the shape of an impulse, whereas for an actual oscillator, the spectrum exhibits "skirts" around the carrier frequency, this is shown in *Fig 4.1* [*Behzad Razavi, 1998*].

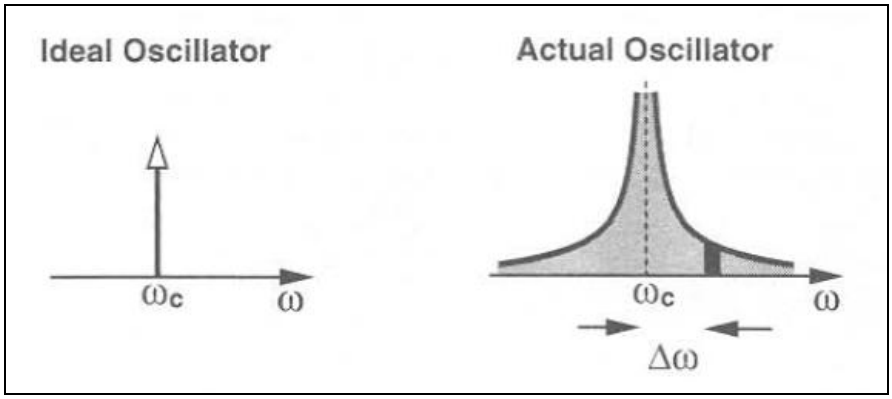

Fig 4.1 Output spectrum of ideal and actual oscillators [*Behzad Razavi, 1998*]

To quantify phase noise, a unit bandwidth at an offset $\Delta\omega$ with respect to ω_c is considered, then, the noise power in this bandwidth is calculated, and the result is divided by the carrier (average) power.

4.2 Effect of Phase Noise In RF Communications

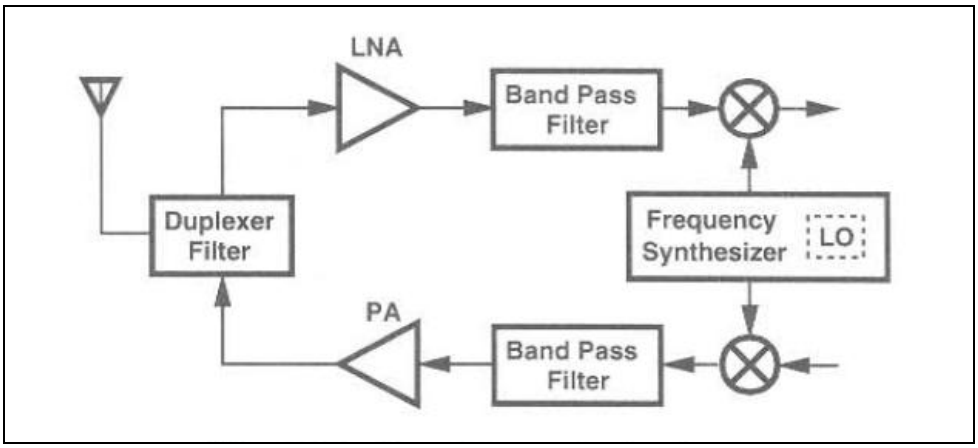

Fig 4.2 Generic transceiver front end [*Behzad Razavi, 1998*]

To understand the effect of phase noise in RF communication systems, consider a generic transceiver given in *Fig 4.2* [*Behzad Razavi, 1998*] where a local oscillator provides the carrier signal for both the transmit path and receive path. If the LO output contains phase noise, both downconverted and upconverted signals are corrupted. This is shown in *Fig 4.3*.