INVESTIGATION OF PHOSPHORUS SPIN ON DOPANT ON SOI WAFER

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INVESTIGATION OF PHOSPHORUS SPIN ON DOPANT ON SOI WAFER

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DECLARATION

I hereby declare that I have conducted, completed the research work and written the dissertation entitled ‘Investigation of Phosphorus Spin on Dopant on SOI Wafer’. I also declare that it has not been previously submitted for the award of any degree and diploma or other similar title of this for any other examining body or University.

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
BOE	Buffer Oxide Etchant
CMOS	Complementary Metal-Oxide Semiconductor
CVD	Chemical Vapour Deposition
EHP	Electron-Hole-Pairs
erfc	Complementary Error Function
HMS	Hall Effect/electronic transport Measurement System
IC	Integrated Circuit
MEMS	Micro-Electromechanical Systems
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
RCA	Radio Corporation of America
RMS	Root Mean Square
SC-1	Standard Clean 1
SC-2	Standard Clean 2
SCE	Short-Channel Effects
SEM	Scanning Electron Microscopy
SOD	Spin on Dopant
SOI	Silicon on Insulator
XRD	X-ray Diffraction

LIST OF SYMBOLS

%	Percentage
ΔV	Voltage drop
°	Degree
°C	Degree celsius
µm	Micrometer
B	Magnetic field
c(x, t)	Concentration at depth x and time t
cm	Centimeter
D	Diffusion coefficient
D_0	Pre-exponent factor
E_a	Diffusion activation energy
I	Current
J	Steady-state flow of impurity atoms
K	Kelvin
mm	Millimeter
MΩ·cm	Mega ohm centimeter
N_0	Impurity concentration at the wafer surface
nm	Nanometer
ppm	Parts per million
Q	Dose
rpm	Revolutions per minute
Rs	Sheet resistance
SLM	Standard litres per minute
t_f	Thickness of the film

V_H	Hall voltage
ρ	Resistivity

LIST OF CHEMICAL FORMULA

Al	Aluminium
Cr	Chromium
Cu	Copper
Fe	Ferum
N_2	Nitrogen
Ni	Nickel
O_2	Oxygen
Si	Silicon
SiO_2	Silicon dioxide

PENYELIDIKAN TENTANG PUTARAN FOSFORUS ATAS DOPAN PADA WAFER SOI

ABSTRAK

Wafer silikon di atas penebat telah memungkinkan untuk sektor litar bersepadu mengembangkan prestasi peranti semikonduktor dan teknik pendopan sangat penting dalam membentuk persimpangan PN untuk peranti semikonduktor. Terdapat dua teknik pendopan yang paling biasa iaitu pemendapan wap kimia dan implantasi ion. Dalam kajian ini kaedah pendopan baru iaitu penyebaran haba menggunakan dopan atas putaran digunakan. Teknik dopan atas putaran adalah teknik alternatif yang merangkumi pemendapan larutan yang mengandungi dopan ke atas wafer silikon di atas penebat. Tujuan penyelidikan ini adalah untuk mengkaji kesan suhu pre-pemendapan dan masa rendaman terhadap turun naik rintangan kepingan. Selain itu, keseragaman pendopan juga dikaji dengan menggunakan teknik pemetaan. Wafer SOI doped boron besar dipotong dan dibersihkan menggunakan kaedah standard Radio Corporation of America. Filmtronics SOD P509 berfungsi sebagai dopan jenis-N menggunakan wafer silikon di atas penebat selama 40 saat pada 4000 rpm dengan menggunakan penyalut putaran. Suhu pre-pemendapan dan masa pemendapan ditetapkan dari 700°C hingga 1000°C dan 30 hingga 120 minit untuk menentukan pengaktifan dopan. Selepas pre-pemendapan, sampel diproses dengan asid hidrofluorik cair. Semua sampel dicirikan oleh penduga empat titik, kesan Hall dan mikroskop kuasa atom. Peningkatan masa rendaman pre-pemendapan mengurangkan rintangan lembaran tetapi tidak terus berkurang apabila dopan diaktifkan tepu. Apabila rintangan lembaran menurun, kepekatan dopan meningkat. Suhu dan masa rendaman meningkatkan kepadatan pembawa dan kekasaran permukaan tetapi mengurangkan Hall mobiliti.

INVESTIGATION OF PHOSPHORUS SPIN ON DOPANT ON SOI WAFER

ABSTRACT

Silicon on insulator (SOI) wafer has made it possible for the integrated circuit sector to develop superior, high-performance of semiconductor device and doping techniques are essential in forming the PN junction for semiconductor device. There are two most common doping techniques which is chemical vapour deposition and ion implantation. In this research study new doping method which is thermal diffusion using spin on dopant is introduced. The spin on dopant technique is an alternative technique that involves spinning a dopant-containing solution onto silicon on insulator wafers. The aim of this research work is to investigate the effect of thermal diffusion temperature and soaking time on its sheet resistance. In addition, doping uniformity also been investigated by using mapping techniques. Three inches boron-doped silicon on insulator wafer were cut and undergo Radio Corporation of America (RCA) standard cleaning. Filmtronics spin on dopant (SOD) P509 served as N-type dopants placed on silicon on insulator wafer for 40 seconds at 4,000 rpm using a spin coater. Thermal diffusion temperature and soaking time were set from 700°C to 1000°C and 30 to 120 minutes, respectively. After thermal diffusion, samples were etched with hydrofluoric acid (HF). All samples were characterized by four point probe, Hall Effect and Atomic Force Microscopy (AFM). The increase of thermal diffusion soaking time reduces sheet resistance until activated dopants are saturated at 900°C. When sheet resistance decreased, the concentration of dopants increased. Temperature and soaking time enhanced the carrier density and surface roughness but reduced Hall mobility. Mapping techniques showed that low non-uniformity value which was less than 10% suggested good thermal diffusion control.

CHAPTER 1

INTRODUCTION

In this research, silicon on insulator (SOI) wafer is investigated to determine the effect of thermal diffusion temperature and soaking time on its sheet resistance. The structure that is known as SOI is a type of semiconductor that is made of a layer of monocrystalline silicon that is kept off from the bulk substrate by a thin layer of insulator. Several temperatures and soaking times were applied to determine the optimal thermal diffusion temperature and soaking time for providing the required sheet resistance of the SOI wafer. This chapter describes the research background, problem statement, research objectives and thesis outline.

1.1 Research Background

Silicon is an integral component of numerous technological products. However, as technology advancing, the demand for smaller, more efficient gadgets has increased. The industry has been able to overcome a number of the limitations of traditional scaling due to the improvement of substrate engineering. As a consequence to this, device architecture and tailored substrates are now tightly connected, a relationship that will only become stronger as the integrated circuit industry continues its march toward 32 nm and beyond. Conventional bulk silicon devices are susceptible to electrical challenges such as junction area, leakage current, isolation, and parasitic capacitance. SOI structures have garnered a lot of attention because they offer solutions to these problems. SOI has enabled the IC industry to produce superior high-performance logic solutions (Nguyen, Celler & Mazuré, 2009).

SOI wafers are multilayer semiconductor and dielectric frameworks that are finely constructed. They provide advanced Si devices with capabilities that have never

been seen before. Using SOI wafers in the fabrication process enables the production of monolithic semiconductor circuits. These circuits have dielectric isolation in place of junctions. SOI structures are made of a layer of single-crystalline silicon that is separated from the bulk substrate by a layer of silicon dioxide (SiO_2). An essential element of SOI systems is the SiO_2 layer, which is also frequently referred to as the buried oxide (BOX) layer.

SOI wafers have several advantages over traditional bulk silicon wafers, including dielectric isolation, short-channel effects, vertical junctions, flexibility in circuit design and processing, low voltage operation, and dependability. Vertical isolation shields the thin active silicon layer from the majority of the parasitic effects that are caused by the extremely "bulky" substrate. Leakage currents, radiation-driven photocurrents, latch-up effects, and other similar phenomena are examples of these effects. Inter-device separation in SOI, on the other hand, is significantly easier to achieve due to lateral isolation. The capacitance, leakage current, and junction surface are all reduced when a buried oxide layer is present at the junction. As a result of these characteristics, there is a reduction in the amount of power consumed, an increase in velocity, and a wider temperature range. Furthermore, the narrow junction area limits the extent of the drain and source regions, and the dual-gate control of the body potential makes SOI devices less vulnerable to short-channel effects (SCE). These effects are the result of "charge sharing" between the gate and junctions, and they are caused when the drain and source regions of the device are not allowed to extend as far as they normally would (Cristoloveanu, 2014).

Scalability is one of the most crucial characteristics that SOI wafers should possess. The film thickness of the SOI wafer can be adjusted, in contrast to the bulk Si. A wide range of silicon or other semiconductor film thicknesses, buried oxide

thicknesses, or other insulator thicknesses can be achieved using the Smart Cut^{TM} process by fine-tuning implant energy and oxidation or deposition time. This allows the Smart Cut^{TM} technique to be used to cut through a wide variety of materials. The thickness of the silicon film that is often required for modern applications might range anywhere from 5 nm to 1.5 µm. In most cases, the thickness of silicon dioxide ranges from 10 nm to 5 µm. As a result, SOI wafers are compatible with the vast majority of device topologies, including thick-film power transistors, ultrathin CMOS, and sensors (Nguyen, Celler & Mazuré, 2009). However, the practical usage of SOI wafers still faces significant obstacles. The key concerns are wafer efficiency in terms of cost, uniformity, and availability, unique transistor effects such as floating body, self-heating, dynamic transients, and interface coupling, as well as technological modification and integrated circuit architecture for SOI applications, are the primary issues (Moriceau, Fournel & Rieutord, 2014).

Doping techniques are required in the silicon sector because the electrical properties of the material need to be precisely managed. Doping can be accomplished by several process. One such approach is known as chemical vapour deposition (CVD), which makes use of a furnace twice (once for thermal diffusion and once for drive-in) and can be expensive due to the explosive nature of the source gas. The other extensively used process is ion implantation, which involves blasting Si with high-energy dopant ions to substitute Si atoms in the lattice. This is done to increase the device performance. This method ensures a high degree of doping homogeneity; nevertheless, the point defects and vacancies in the lattice that are produced as a result of the bombardment operation would lower the quality of the materials and, as a result, the functionality of the device degrades.

The spin on dopant (SOD) method is an alternative method that involves spinning a dopant-containing solution onto SOI wafers, which is then followed by thermal diffusion procedures. SOD can evenly distribute liquid dopants on a silicon substrate. In the manufacturing of microelectronic devices, dopants are employed to generate ultra-shallow connections with a single thermal treatment. This strategy presents numerous benefits over the previous typical methods: The SOD sources are not only inexpensive but also risk-free; hence, the process of screening for the presence of dangerous gases can be skipped. Furthermore, the elimination of high-energy dopant ions renders the SOD method nondestructive. In addition to this, the SOD method is simplified and accelerated due to the room-temperature spinning process and the one-time utilization of the furnace. (Patel *et al.*, 2019).

1.2 Problem Statement

The characteristics of semiconductors are determined by the impurities that are added to the fundamental materials. These impurities can change the electrical, physical, and optical properties of semiconductors. In conventional approaches to the manufacturing of semiconductor devices, doping can be accomplished using any one of the following three processes: ion implantation, in situ co-deposition, or thermal diffusion. Ion implantation is a remarkable procedure that enables a high degree of control to be applied over the number of impurity atoms that are implanted as well as the depth to which they are inserted. However, the usual method of ion implantation, which involves blasting semiconductors with energetic ions, produces substantial crystal damage. Because of this, an annealing phase is required to repair the crystal and activate the implanted impurities. As a result of the normally necessary extremely high temperatures, its potential application is limited to platforms that are capable of

sustaining high thermal budget procedures. Ion implantation is a method that is both difficult and expensive due to the variables mentioned above. (Barri *et al.*, 2021).

In co-deposition processes, such as chemical vapour deposition (CVD), use a carrier gas to inject the dopant directly into the growth chamber. This process offers a high level of control over the dopant concentration as well as the solubility of the dopant, both of which may be modified by adjusting the vapour pressure of the dopant gas source and the temperature of the substrate while the thin film is being deposited. However, because the CVD approach involves the use of hazardous and explosive gases, several safety precautions need to be taken during the process. As a result, this method is both expensive and unsafe. In addition to this, because it makes homogeneous contact with the surface of the wafer, this approach lacks spatial control. (Martin, 2010).

In conventional furnaces, doping is achieved by exposing the wafers to a flux of dopant atoms obtained from the sublimation or evaporation of a solid, liquid, or gas source. A greater amount of dopant will diffuse into the substrate if the wafers are heated for the amount of time necessary to achieve the desired doping profile. In most cases, doping furnaces can only be placed within huge facilities that can handle a significant number of substrates. On the other hand, due to the potentially hazardous nature of the dopant sources, this stage of the process often requires a significant amount of time spent in a laboratory setting (Barri *et al.*, 2021).

In recent years, enormous research efforts have been made to establish new strategies for implementing dopants into semiconductor materials. One of these new strategies is called spin on dopant and it offers several advantages over conventional methods. This is done to overcome the difficulties and costs that are associated with

traditional technologies. (Patel *et al.*, 2019). Hence, P509 SOD was used as a dopant on SOI wafer.

The knowledge gap from previous research is that the doping methods used were expensive and involved explosive sources of gas, such as the CVD and ion implantation method. Hence, the novelty in this research work is using thermal diffusion process with the SOD method, which can overcome all the problems faced in CVD and ion implantation. Besides that, SOI wafer was used compared to silicon wafer that was used by previous researchers due to the advantage of quality is easy to control.

1.3 Research Objectives

There are three main objectives in this research shown as follows:

1. To investigate electrical properties of SOI wafer after thermal diffusion process at various temperature and soaking time.
2. To determine the doping uniformity of the SOI wafer after the doping process by using a mapping technique.
3. To determine the surface roughness of the SOI wafer after thermal diffusion process at various temperature and soaking time.

1.4 Thesis Outline

This dissertation consists of five chapters, which start from Chapter 1: Introduction. In Chapter 1, the introduction, research background, problem statements and scopes of research are discussed. Next, Chapter 2 is the literature review done for the research project. The main focus of Chapter 2 is diffusion mechanisms and diffusion concentration gradients in various conditions, followed by an introduction to SOI wafer structures and applications, as well as its advantages over a silicon wafer.

In addition, Chapter 2 discusses the spin-on-dopant method, sheet resistance, four-point probe measurement, and Hall Effect measurement. Chapter 3 explains the raw materials, experimental procedures and characterization techniques used throughout the research project to investigate the effect of temperature and time taken for thermal diffusion towards sheet resistance of the SOI wafer. Furthermore, Chapter 4 consists of the experimental result obtained through experimental work and the analysis and discussion done on this research project. Finally, Chapter 5 containing conclusion made after completing the experimental work, analysis, and discussion of the entire research project. Various recommendations are also being suggested for future related work in this final chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Doping Process

Doping refers to the process of intentionally introducing impurity into semiconductor materials to control its electrical properties. Doping is used in the semiconductor device fabrication to change the electrical characteristics of semiconductors material, which is the primary use of the technique to create the p-n junction in transistor. Movements of free electrons and holes, generally known as charge carriers, are responsible for current conduction in semiconductors. Doping is the process of adding impurity atoms to a semiconducting material to enhance the number of charge carriers within it. When a doped semiconductor includes predominantly free holes, it is refer as p-type semiconductor, and when it contains predominantly free electrons, it is refer as n-type semiconductor (Rahman, 2014). Impurity doping can be accomplished through two primary processes: diffusion and ion implantation.

2.1.1 Diffusion

The production of impurity doped regions in semiconductor wafers is commonly accomplished by the process of diffusion. As can be seen in Figure 2.1, the primary method of impurity doping utilized up until the early 1970s was diffusion, which took place at higher temperature. The traditional method involves placing a batch of wafers in a diffusion furnace and exposing them to a gaseous form of the impurity species. This results in the impurity species being deposited on or near the surface of the wafers. After that, the wafer goes through a process called drive-in diffusion, which often takes place in another diffusion furnace. The furnace is filled with an inert gas that is heated to between 900°C and 1050°C and flows through it.

This allows the impurity atoms to diffuse into certain portions of the wafer that are not covered by oxide layers. The impurity concentration, temperature, and length of time spent in the furnace all influence the extent of the diffusion process. The time required for diffusion is normally somewhere within the range of 30 minutes for the temperature range between 900°C and 1050°C. Poor impurity homogeneity over the surface of the wafer and poor control of impurity dosage have been long-standing issues with diffusion furnaces. Due to these issues, the diffusion furnace is becoming less useful as integrated circuit components continue to get smaller and more densely packed (Sze & Lee, 2012)(Russo, 2014).

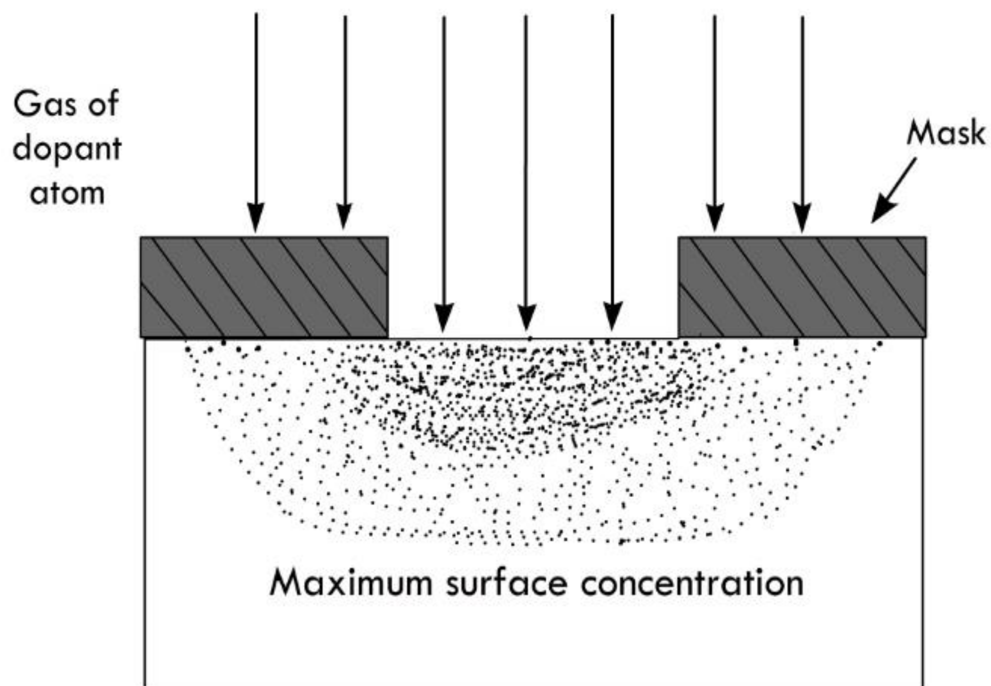


Figure 2.1: Thermal diffusion (Zant, 2004)

2.1.2 Ion Implantation

Ion implantation into semiconductor wafers is a doping technique that improves poor impurity uniformity over the surface of the wafer and poor control of impurity dosage in diffusion. Both the consistency of the doping and the dosage can be precisely measured and regulated. Ion implantation has been used in a huge

percentage of doping operations ever since the early 1970s, as can be seen in Figure 2.2. Ion beams are used in this method to irradiate the semiconductor with dopant ions, which are then implanted into the semiconductor. The doping concentration has a peak distribution inside the semiconductor, and the profile of the dopant distribution is mostly controlled by the ion mass and the implanted-ion energy. However, the depth to which impurity dopants can be deposited via ion implantation is restricted due to the fact that energy concerns must be taken into account (Russo, 2014).

Due to both diffusion and ion implantation techniques often complement one another, they are both used in the manufacturing of integrated circuits and discrete devices. For instance, a deep junction (such as a twin well in CMOS) can be formed by the process of diffusion, whereas a shallow junction (such as a source/drain junction in a MOSFET) can be formed through the process of ion implantation (Sze & Lee, 2012).

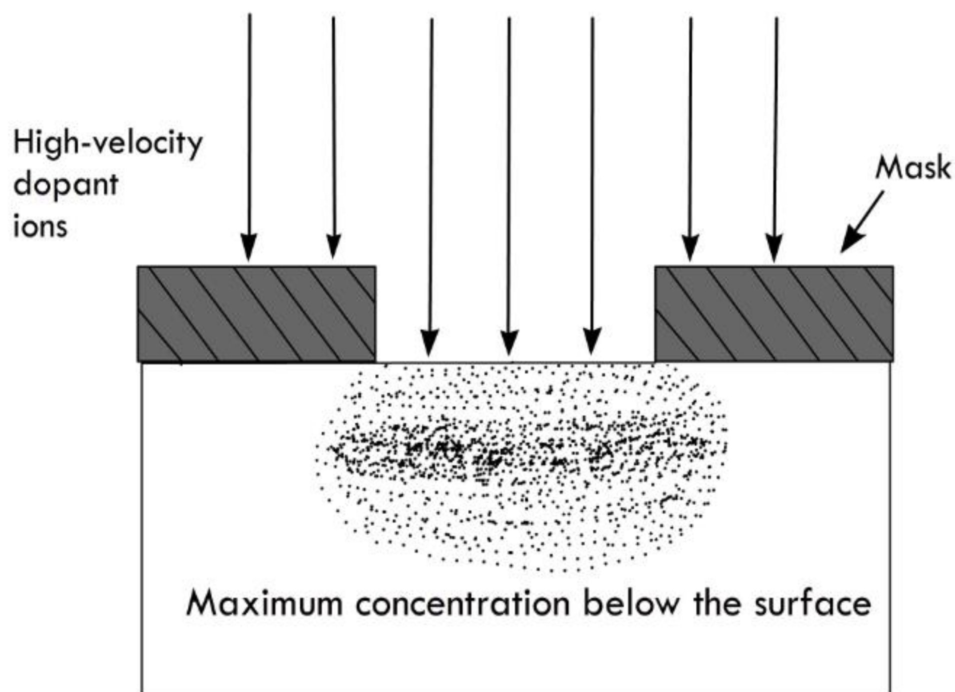


Figure 2.2: Ion implantation (Zant, 2004)

2.2 Diffusion Mechanism

The diffusion process begins with the deposition of a thin high-concentration layer of the targeted contaminant on the silicon surface via windows etched in the protective barrier layer. Impurity atoms penetrate from the top into the silicon crystal through interstitial or substitutional diffusion processes at high temperatures (900°C to 1200°C) demonstrated in Figure 2.3 and Figure 2.4 (Parasuraman, 2014).

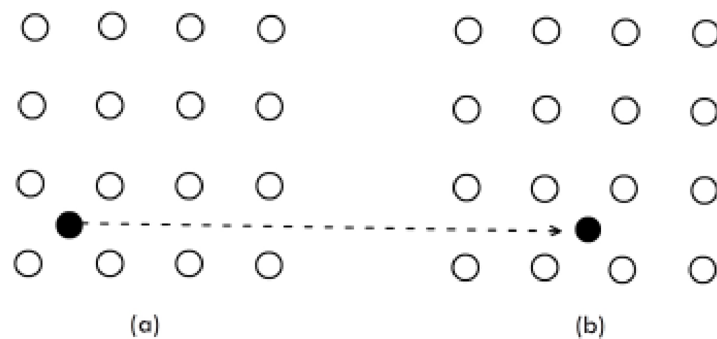


Figure 2.3: Interstitial diffusion mechanism (Ghandhi, 1995)

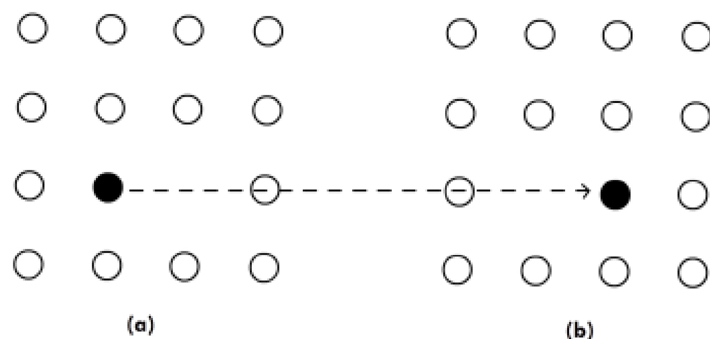


Figure 2.4: Substitutional diffusion mechanism (Ghandhi, 1995)

The impurity atom jumps from one crystal lattice position to another in the situation of substitutional diffusion. As a result, the impurity atom "substitutes" for a silicon atom in the lattice. For the substitutional process to take place, holes in the silicon lattice have to be present. Theoretically, a particular amount of vacancies will always exist in the lattice. Holes might potentially be generated at high temperatures

by shifting silicon atoms from their regular lattice locations into the unoccupied interstitial region among crystal lattices. Interstitial diffusion refers to the substitutional diffusion process in which silicon atoms are shifted into interstitial areas. (Ghandhi, 1995).

Referring to Jaeger (2002), significant space develops among atoms in the silicon lattice and some impurity atoms permeate through the crystal by leaping from one interstitial site to another. Interstitial diffusion moves faster than substitutional diffusion because it does not need the presence of holes. Due to the obvious high rate of diffusion, interstitial diffusion is challenging to regulate. Impurity atoms require to fill substitutional positions in the lattice to supply electrons or holes for conduction. Due to the source of vacancies being restricted, substitutional diffusion happens at a fairly low pace. However, this slow diffusion rate is a benefit since it enables good management of the diffusion process.

2.2.1 Diffusion System

The open furnace tube method uses solid, liquid, or gaseous inputs. Diffusion may be performed using three-zone horizontal furnaces. Wafers are placed in a quartz boat and placed inside the furnace's middle region, which has the maximum temperature. Impurities diffuse within the wafer after being delivered to the silicon surface.

Liquid spin on sources may be used to apply the most common silicon dopants. These spin on dopants are adaptable, secure, and simple for using, although their homogeneity is often lower than that of other impurity sources. Most manufacturing systems employ other solid, liquid, or gaseous contaminant sources to ensure effective quality control (Jaeger, 2002).

A concentration of the dopant vapour at the surface should be formed for liquid and gaseous sources. When using a liquid input, the carrier gas is typically utilized to travel the vapours towards the diffusion furnace. The carrier gas in liquid-source systems passes via a bubbler, which releases the liquid source's vapour. The gas takes the vapour into the furnace tube, where it interacts with the surface of the silicon wafer. Figure 2.5 depicts the setup for thermal diffusion with a liquid dopant source. A carrier gas, such as nitrogen, is flowed through the dopant liquid, transporting the vapour into the furnace. When an oxide layer must be generated in combination with doping, oxygen is also utilized (May & Spanos, 2006).

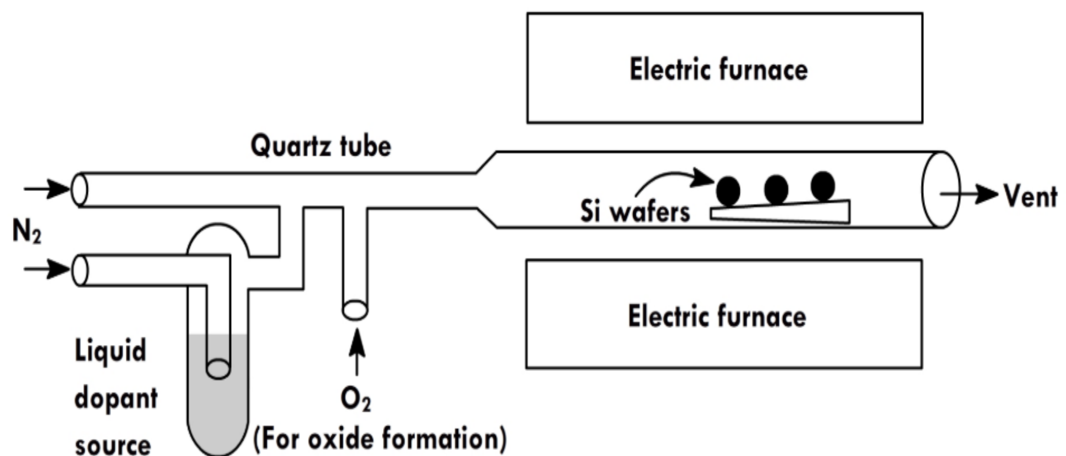


Figure 2.5: Setup for thermal diffusion with a liquid dopant source (May & Spanos, 2006)

An identical configuration is utilized for gaseous sources. The carrier gas is utilized in this situation to dilute the dopant gas to the desired concentration. Gas-source methods provide the gaseous condition dopant material straightforwardly towards the furnace tube. The usual gas sources are exceedingly hazardous, and extra input purging and trapping devices are necessary to guarantee that input gas is eliminated from the system prior to wafer entrance. Furthermore, many diffusion

procedures do not even employ each of the supply gas or create unwanted reaction by-products. Hence, the product of diffusion systems should be treated by firing or by chemicals or water washing prior to getting expelled into the environment. Figure 2.6 depicts a gas manifold system for a thermal diffusion system. The dopant gas and inert gas are combined to achieve the desired concentration of dopant. If an oxide layer is also required, a reaction gas, such as oxygen, is utilized (Zant, 2004).

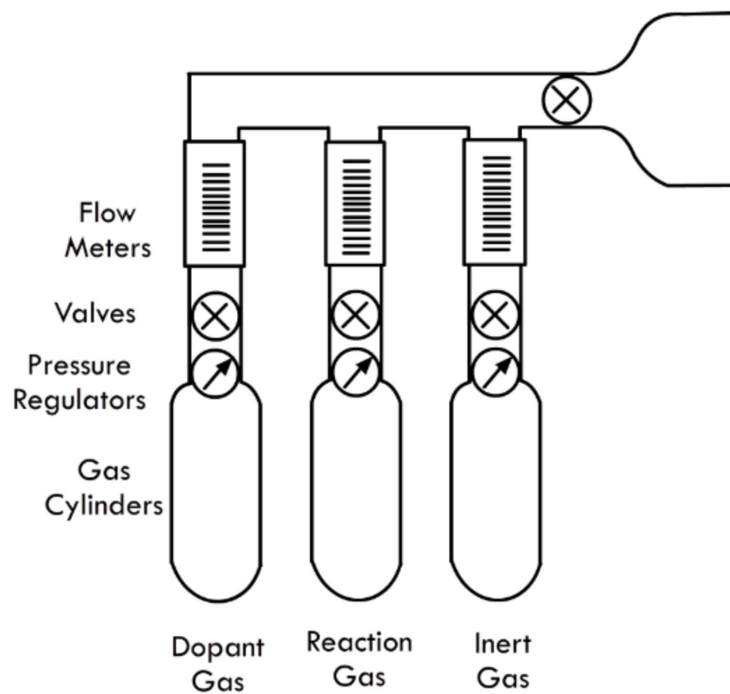


Figure 2.6: Gas manifold system for a thermal diffusion system (Zant, 2004)

Solid sources are made by loading wafer-sized "slugs" into the furnace alongside the output wafers; this is termed as a solid neighbour source. Another alternative is to rotate the oxide source on the wafer surface using an appropriate solvent, which is usually utilized for oxide sources. It is also probable to evaporate the solid source in a nearby furnace and utilize a carrier gas to carry the vapours to the wafer. Carrier gases typically nitrogen (N_2) or oxygen (O_2) flow at a regulated pace over a source boat positioned in the furnace tube in one form of solid-source system. The carrier gas absorbs the vapour from the source and delivers the dopant species to

the wafer, where they are deposited on the wafer's surface. The temperature of the source is regulated to keep the proper vapour pressure. The source might be located in a low-temperature part of the furnace or it might be located outside of the furnace. Solid boron and phosphorus impurity sources in wafer form were accessible and inserted in the boat among neighbouring pairs of silicon wafers. Figure 2.7 depicts the application of solid sources in thermal diffusion. Solid sources for thermal diffusion might be either faraway or neighbour sources. The solid is evaporated at a remote source, and then the vapours are transferred into the furnace. The solid is placed in the furnace alongside the wafers in neighbouring sources. All of these sources provide unique wafer concentration patterns (Parasuraman, 2014).

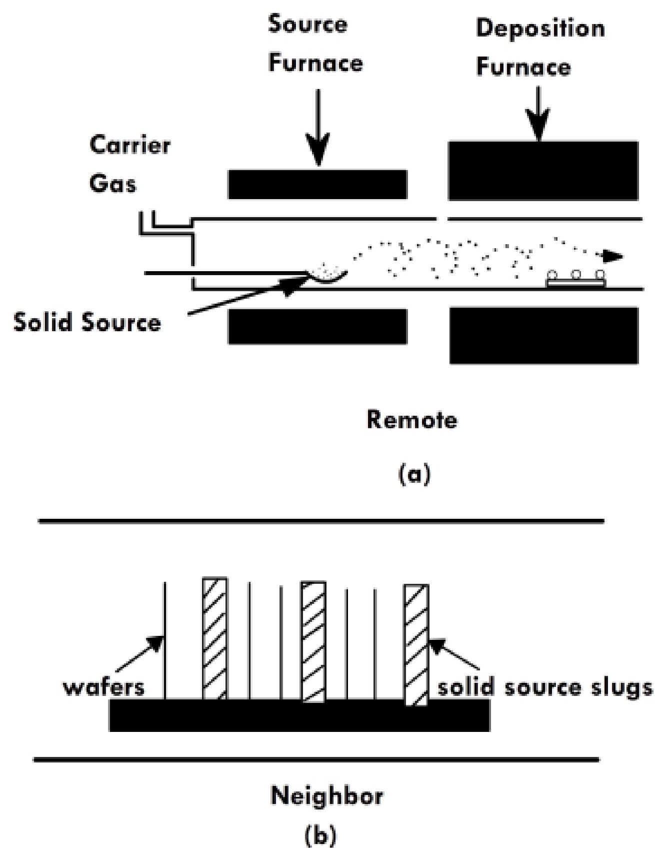


Figure 2.7: Application of solid sources in thermal diffusion (Zant, 2004)

Jaeger (2002) states that boron is the only regularly utilized p-type dopant. Since the diffusion coefficients of aluminium and gallium in silicon dioxide are relatively high, these elements cannot be effectively covered by SiO_2. Indium is not utilized since it is a low-level acceptor. In contrast, antimony, phosphorus, and arsenic can all be covered by silicon dioxide and are mostly utilized as n-type dopants in silicon manufacturing.

2.2.2 Phosphorus Diffusion

The dopant atoms come from a variety of sources. These sources can be solid, liquid, or gaseous. In our study, we focus on n-type phosphorus dopant. Hence, these are some examples of phosphorus Si dopant materials are as Table 2.1:

Table 2.1: Types of dopant sources

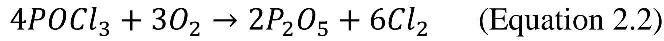
Compound	Formula	State
Phosphorus Oxychloride	$POCl_3$	Liquid
Phosphorus Pentoxide	P_2O_5	Solid
Phosphine	PH_3	Gas

Phosphorus is more soluble in silicon than boron, and surface concentrations as low as $10^{21}/cm^3$ have been produced during high-temperature diffusion. The reaction of phosphorus pentoxide at the wafer surface incorporates phosphorus into silicon shown as Equation 2.1:

$$2P_2O_5 + 2Si \rightleftharpoons 4P + SiO_2 \qquad \text{(Equation 2.1)}$$

Solid P_2O_5 wafers, as well as ammonium monophosphate ($NH_4H_2PO_4$) and ammonium diphosphate ($(NH_4)2H_2PO_4$) wafers, may be utilized as solid phosphorus sources. However, most diffusion systems use either liquid or gaseous sources. At

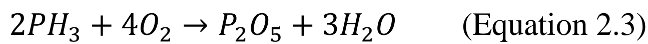
room temperature, phosphorus oxychloride ($POCl_3$) is a liquid. A bubbler pushes a carrier gas into the diffusion furnace, which transports the vapour. The gas stream also contains oxygen, and P_2O_5 is deposited on the wafers' surfaces shown as Equation 2.2:



$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2$ (Equation 2.2)

Cl_2 and $POCl_3$ must be removed from the exhaust stream, and liberated chlorine gas acts as a gettering agent.

Phosphine, PH_3, is an extremely poisonous, flammable gas utilized as the gaseous source for phosphorus. It is also available in a diluted version with 99.9% argon or nitrogen. In the furnace, phosphorus is oxidized with oxygen which the reaction is shown as Equation 2.3:



$2PH_3 + 4O_2 \rightarrow P_2O_5 + 3H_2O$ (Equation 2.3)

The residual phosphine in the exhaust gases must be removed, and the gas supply system must be equipped to expel phosphine from the feed to the tube. (Parasuraman, 2014).

2.2.3 Diffusion Concentration Gradients

The solubility of Si in solids determines the number of impurities that may be incorporated into it. Figure 2.8 shows how this varies depending on the impurity atom and temperature. The concentrations of impurities as a function of depth from the wafer surface may be determined using Fick's laws of diffusion. Fick's first law is written as Equation 2.4:

$J = -D\frac{\partial c(x,t)}{\partial x}$ (Equation 2.4)

where J denotes the steady-state flow of impurity atoms, c(x, t) denotes the concentration at depth x and time t, and D is the diffusion coefficient. D is a temperature-dependent variable that is given by Equation 2.5:

$$D = D_0 \, exp \, (-\frac{E_a}{k_B T}) \qquad \text{(Equation 2.5)}$$

where D_0 denotes the pre-exponent factor, while E_a denotes the diffusion activation energy. (Parasuraman, 2014).

Fick's second law is a more basic equation for non-steady states with flux that fluctuates with time and position.

$$\frac{\partial c(x,t)}{\partial t} = -\frac{\partial J(x,t)}{\partial x} = D\frac{\partial^2 c(x,t)}{\partial x^2} \qquad \text{(Equation 2.6)}$$

The assumption is that D does not vary with concentration. This assumption is invalidated at high impurity concentrations. The concentration gradient under various conditions can be calculated using Equation 2.4 and Equation 2.6.

The maximum quantity of dopants that may be assimilated based on impurity solubility is shown in Figure 2.8. The solid solubility of contaminants in Si varied due to temperature. The solubility of frequently employed p and n dopants is high, reaching that of degenerate semiconductors. Metals and oxygen have solubility values of a few parts per million (ppm). There are two common doping conditions in thermal diffusion. Variable separation or Laplace transform techniques may be used to solve the partial differential equation in Equation 2.6. In modelling impurity diffusion in silicon, two types of boundary conditions are important. The first is constant-source diffusion, in which the surface concentration is kept constant during the diffusion. The second method is termed as limited-source diffusion, and it involves depositing a

predetermined quantity of the impurity species in a thin layer on the surface of the silicon (Jaeger, 2002).

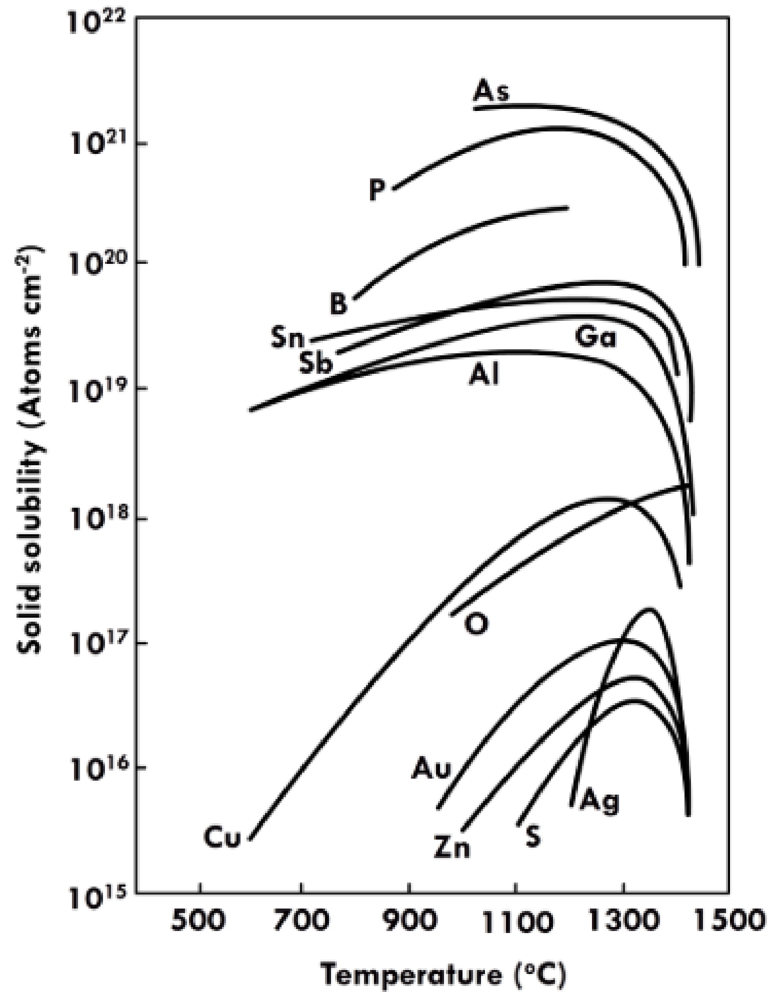


Figure 2.8: Solid solubility of various impurities in Si as a function of temperature (Zant, 2004)

2.2.3(a) Constant-Source Diffusion

There is a stable concentration of contaminants near the surface of gaseous and liquid sources. There is a vapour of impurity atoms that maintains the surface concentration constant. Furthermore, since the penetration depth is substantially less than the wafer depth, the wafer may be represented as a semi-infinite solid. The impurity concentration, N(x, t), is given in this case by

$N(x,t) = N_0\, erfc\,(\frac{x}{2\sqrt{Dt}})$ (Equation 2.7)

where N_0 is the impurity concentration at the wafer surface ($x = 0$) and this kind of diffusion is termed a complementary error function (erfc) diffusion. The diffusion front moves deeper and deeper within the wafer over time, while the surface concentration remains constant. The total amount of impurity atoms per unit area in silicon is termed as the dose, Q, and is measured in atoms/cm^2. Q grows with time, and an external impurity source must give a steady flow of impurity atoms to the wafer's surface. By integrating the diffused impurity concentration across the silicon wafer yields the dose. (Sze & Ng, 2006). The equation is shown as Equation 2.8.

$Q = \int_0^{\infty} N(x,t)dx = 2N_0\sqrt{\frac{Dt}{\pi}}$ (Equation 2.8)

A complementary error function impurity distribution results from constant-source diffusion. Figure 2.9 displays the error function solution for this system, which shows concentration profiles with growing time for a fixed surface concentration. (Parasuraman, 2014). As the Dt product grows, the surface concentration N_0 stays unchanged, and diffusion goes deeper into the silicon wafer. Dt may alter as a consequence of increased diffusion time, the rising temperature of diffusion, or a combination of both. The concentration is highest at the surface.

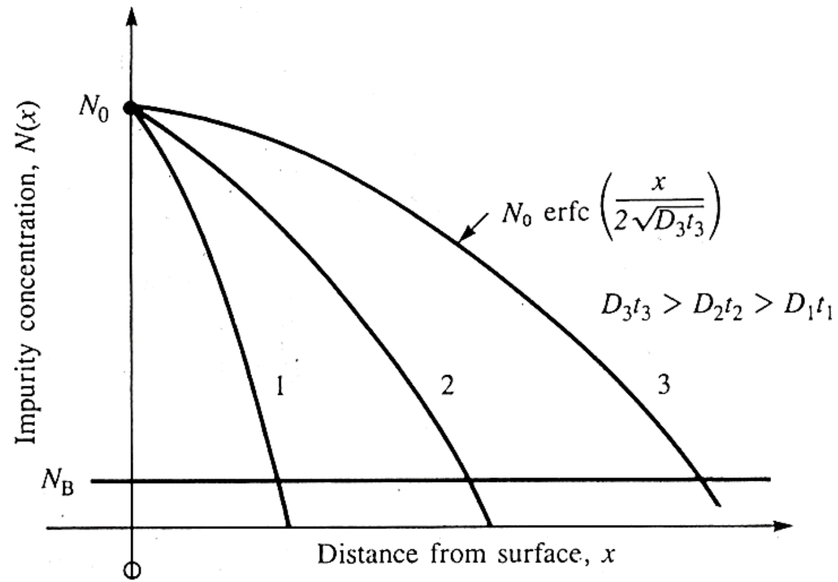


Figure 2.9: Graph of constant-source diffusion (Jaeger, 2002)

2.2.3(b) Limited-Source Diffusion

An impulse function on the silicon surface is used as the initial boundary condition to explain a limited-source diffusion. The amount of the impulse is equivalent to the dose Q. In this situation, the overall number of dopant atoms is constant at the start of the diffusion process, whereas the concentration of atoms at the surface eventually drops over time. This occurs when doping is done from a solid source that is nearer to the wafer (either solid slugs close to the wafer or dopants spun on the wafer surface). Let Q denote the overall number of dopants per unit area on the surface. The concentration, N(x, t), is then calculated as Equation 2.9.

$$N(x,t) = \frac{Q}{\sqrt{\pi D t}} exp\ (-\frac{x^2}{2\sqrt{Dt}})^2 \qquad \text{(Equation 2.9)}$$

This is a Gaussian function, as opposed to the error function solution for a constant surface concentration. Figure 2.10 depicts a limited-source diffusion or constant total dopant diffusion that produces a Gaussian distribution. The diffusion

front goes further into the wafer as the Dt product rises, and the surface concentration decreases. Each of the three curves has the same area under it.

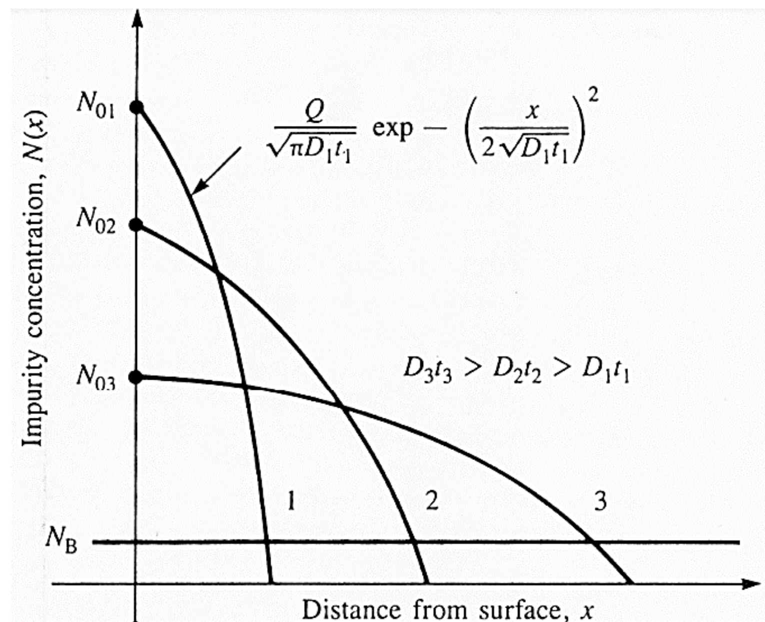


Figure 2.10: Graph of limited-source diffusion

On a normalized logarithmic plot, the forms of the Gaussian and complementary error function curves seem to be identical, as depicted in Figure 2.11. The erfc curve nevertheless goes down faster than the Gaussian curve.

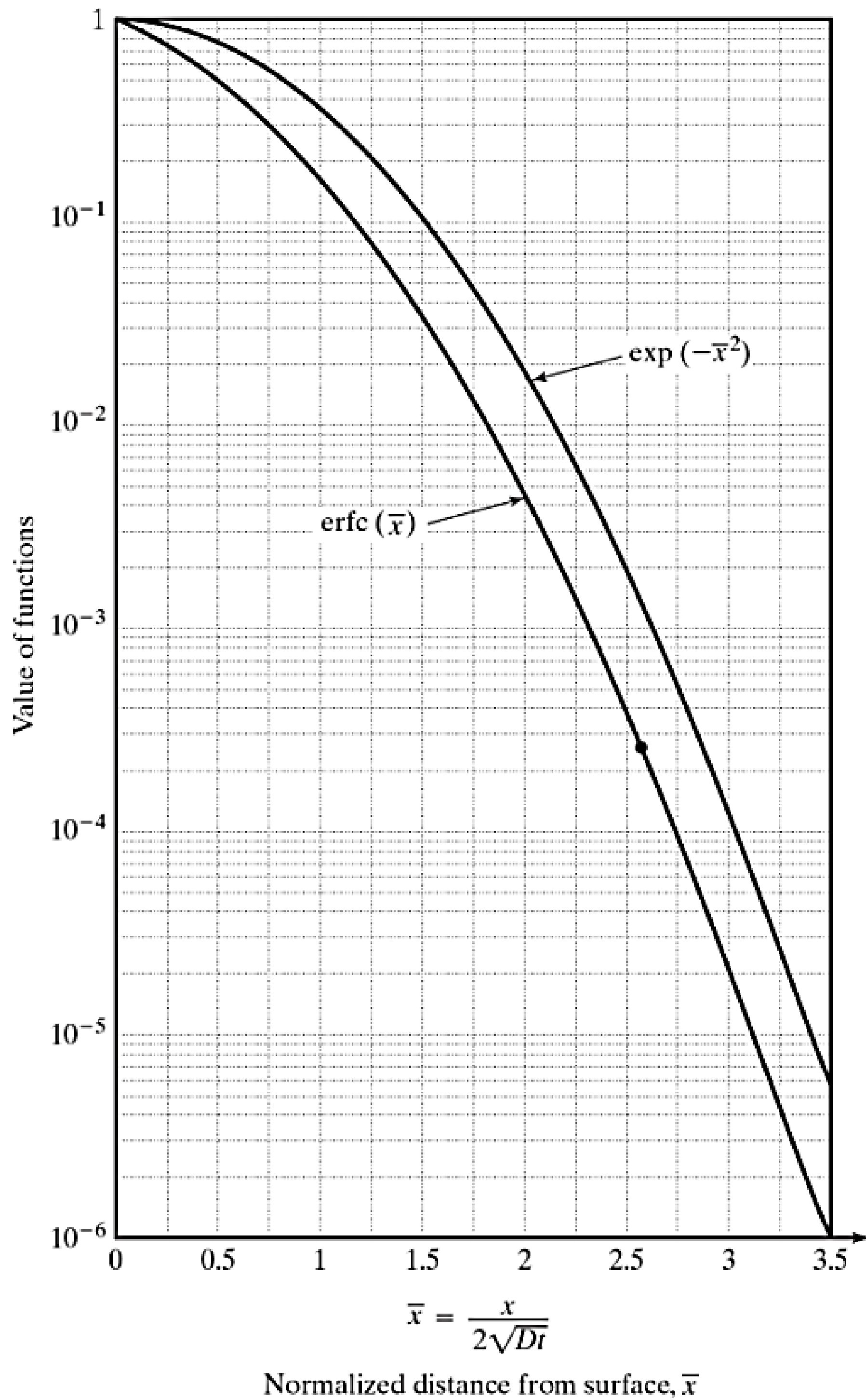


Figure 2.11: Comparison of normalized Gaussian and erfc curves (Jaeger, 2002)

2.2.4 Two-Step Diffusion

Thermal diffusion, like the oxidation process, is a two-step process that consumes the underlying Si. A constant-source diffusion is typically succeeded by a limited-source diffusion, giving a two-step diffusion process. The constant-source

diffusion stage, also termed as the thermal diffusion step, is employed to create a known dose in a thin layer on the surface of the silicon (Ghandhi, 1995). The thermal diffusions step involves implementing dopant atoms onto the wafer surface. During thermal diffusion, the silicon wafer is heated to a specially set and monitored temperature, and an excess of the preferred dopant is kept above the wafer. Dopants diffuse into the crystal until their concentration at the surface equals that of the surrounding ambient above it.

The constant dose resembles an impulse and acts as an impurity source for the second diffusion stage. The drive-in step is used to advance the diffusion process to the required depth during the second diffusion. The stage in which dopant atoms diffuse into the wafer provides the required concentration gradient (Parasuraman, 2014).

Figure 2.12 depicts the stages in thermal diffusion. At (a), dopant atoms are introduced at the surface of the wafer and penetrate into the wafer which known as thermal diffusion stage. At (b), the dopant move deeper into the wafer which known as drive-in stage. While dopant atoms travel vertically within the wafer, they are also distributed laterally. This has significance for the optimum proportions of the doped area. Boron is a common dopant in Si for the p-type and arsenic, antimony, and phosphorus for the n-type (May & Spanos, 2006).