INVESTIGATION OF OXIDATION PROCESS ON SOI WAFER

SHAHARATUL A’INI BINTI SALLEH

UNIVERSITI SAINS MALAYSIA

2022

SCHOOL OF MATERIALS AND MINERAL RESOURCES ENGINEERING

UNIVERSITI SAINS MALAYSIA

INVESTIGATION OF OXIDATION PROCESS ON SOI WAFER

By

SHAHARATUL A'INI BINTI SALLEH

Supervisor:

Assoc. Prof. Dr. Khatijah Aisha Binti Yaacob

Dissertation submitted in partial fulfillment of the requirements for the degree of

Bachelor of Engineering with Honours

(Materials Engineering)

Universiti Sains Malaysia

August 2022

DECLARATION

I hereby declare that I have conducted, completed the research work and written the dissertation entitled ‘Thesis Title’. I also declare that it has not been previously submitted for the award of any degree and diploma or other similar title of this for any other examining body or University.

Name of Student: **Shaharatul A’ini bt Salleh** Signature:
Date: 15 August 2022

Witness by
Supervisor: Assoc. Prof. Dr. Khatijah Aisha Binti Yaacob Signature:
Date: 15 August 2022

ACKNOWLEDGEMENT

Most of all, I would like to send my greatest gratitude to my supervisor, Assoc. Prof. Dr. Khatijah Aisha bt. Yaacob for her continuous support, guidance, and supervision while completing the Final Year Project paper. The advice and continuous support give me a great motivation in completing this project. Without her guidance, this project will not be completed successfully.

Apart from that, I would like to express my gratitude to the administration of School of Materials and Mineral Resources Engineering, Universiti Sains Malaysia for providing all the necessities and equipment in terms of resources, facilities, and materials in making this project a success.

Besides, I would like to extend my thanks to the technical staff of School Materials and Minerals Resources Engineering because without them, this project would not have run smoothly and perfectly. Therefore, many thanks to all technical staff involved in my project directly or indirectly, especially to Mr. Azam who has given a lot of guidance in using the equipment related to this project.

Other than that, I would like to say a million thanks to my parents, family members, classmates, and other colleagues who gave me moral support and advice in completing this project successfully. I truly will not forget all those faces that are always supporting me from behind. Finally, a massive appreciation for myself for not giving up and trying my best throughout completing this project.

TABLE OF CONTENTS

ACKNOWLEDGEMENT ..... **iv**

TABLE OF CONTENTS ..... **v**

LIST OF TABLES ..... **viii**

LIST OF FIGURES ..... **ix**

LIST OF SYMBOLS ..... **xii**

LIST OF ABBREVIATIONS ..... **xiii**

ABSTRAK ..... **xiv**

ABSTRACT ..... **xv**

CHAPTER 1 INTRODUCTION **1**

1.1 Research Background 1

1.2 Problem Statement 3

1.3 Objective 3

1.4 Research Scope 4

1.5 Thesis Outline 4

CHAPTER 2 LITERATURE REVIEW **5**

2.1 Overview 5

2.2 Thermal Oxidation 5

  2.2.1 Mechanism of Thermal Oxidation Process 6

  2.2.2 Growth of Silicon Dioxide 7

  2.2.3 Properties of Silicon Dioxide 9

  2.2.4 SiO_2 Crystal Structure 11

2.3 Other Technique of Silicon Dioxide Deposition 14

  2.3.1 Chemical Vapor Deposition (CVD) 14

  2.3.2 Plasma-Enhanced Chemical Vapor Deposition (PECVD) 17

  2.3.3 Evaporation Deposition 18

2.3.4 Sputtering Deposition 21
2.4 Silicon Dioxide Growth Factor 22
2.4.1 Effect of Oxidation Temperature and Time 22
2.4.2 Effect of Dopant Concentration 23
2.4.3 Effect of Wafer Orientation 24
2.4.4 Effect of Impurities 26
2.4.5 Effect of Dopant Redistribution 28
2.5 SOI Wafer 30
2.5.1 Fabrication of SOI Wafer 32
2.5.2 Advantages of SOI Wafer 35
CHAPTER 3 MATERIALS AND METHODOLOGY 38
3.1 Overview 38
3.2 Chemicals and Materials 39
3.2.1 SOI Wafer 39
3.2.2 Oxygen Gas 39
3.2.3 Ammonium Hydroxide 40
3.2.4 Hydrochloric Acid 40
3.2.5 Hydrogen Peroxide 40
3.2.6 Deionized Water 40
3.3 Experimental Procedure 41
3.3.1 Sample Preparation 41
3.3.2 RCA Cleaning of SOI Wafer 42
3.3.3 Thermal Oxidation Process of SOI Wafer 44
3.3.4 Characterization of SOI Wafer 45
3.4 Characterization Technique 45
3.4.1 X-Ray Diffraction (XRD) on Raw SOI Wafer 45
3.4.2 Four-point Probe 47

3.4.3 Scanning Electron Microscope (SEM) 48

3.4.4 Atomic Force Microscopy (AFM) 48

3.4.5 Thickness Measurement 49

CHAPTER 4 RESULTS AND DISCUSSIONS 51

4.1 Overview 51

4.2 Raw Material Characterizations 51

4.2.1 X-Ray Diffraction Analysis of SOI Wafer 51

4.2.2 Resistivity 52

4.2.3 Scanning Electron Microscope (SEM) 53

4.3 Characterization on Thermally Grown Silicon Dioxide on SOI Wafer 54

4.3.1 Effect of Oxidation Temperature and Time Towards SiO_2 Thickness on SOI Wafer 54

4.3.2 Effect of Resistivity After Thermal Oxidation 62

4.3.3 Effect of Oxidation Temperature Toward ρ 63

4.3.4 Effect of Oxidation Time Towards ρ 65

4.3.5 Comparison of Resistivity on Raw Wafer and Oxide Grown Wafer 65

4.3.6 Atomic Force Microscopy (AFM) analysis on oxide grown samples. 66

CHAPTER 5 CONCLUSION AND FUTURE RECOMMENDATIONS 69

5.1 Conclusion 69

5.2 Recommendations for Future Research 70

REFERENCES 71

LIST OF TABLES

Page

Table 1: Properties of SiO_2 growth by using various source of oxygen *(Sze and Lee, 2012)*...10

Table 2: Segregation coefficient of impurities. m = equilibrium concentration of impurity in the silicon/equilibrium concentration of impurity in the oxide *(Grove et. al., 1964)*. 28

Table 3: Chemicals used and their details. 39

Table 4: Oxidation process parameters on SOI wafer. 42

Table 5: Model specification for F20 Series Thin Film Analyzer. 50

Table 6: Colour chart thermally grown SiO_2 films observed perpendicularly under daylight fluorescent lighting *(Pliskin and Conrad, 1964)*. 56

Table 7: SiO_2 thickness growth at 1000 ℃. 57

Table 8: SiO_2 thickness growth at 950 ℃. 59

Table 9: SiO_2 thickness growth at 900 ℃. 60

Table 10: SiO_2 thickness growth at 850 ℃. 61

Table 11: Data table of resistivity at different temperature and time. 63

Table 12: Surface roughness of wafer sample. 68

LIST OF FIGURES

Page

Figure 1 Basic thermal oxidation apparatus *(Sze and Lee, 2012).* 7

Figure 2: Wet oxidation process on silicon wafer *(Deal and Grove, 1965).* 8

Figure 3: Dry Oxidation Process on Silicon Wafer *(Deal and Grove, 1965).* 8

Figure 4: (a) Structure of thermally grown silicon dioxide. (b) Two-dimensional image of crystalline structure of silicon dioxide. (c) Two-dimensional image of amorphous structure of silicon dioxide *(Sze and Lee, 2012).* 12

Figure 5: Model for oxidant diffusion from the gas phase to silicon surface during thermal oxidation. 13

Figure 6: A typical CVD system with heater elements around the chamber and gas inlet *(Bahreyni, 2008).* 16

Figure 7: Parallel-plate radio frequency (rf) plasma deposition reactor (*Sze and Lee, 2012).* 18

Figure 8: Basic setup of an evaporation system *(Michael and Gary, 1998).* 19

Figure 9: E-beam evaporation technique *(Zhang and Hoshino, 2019).* 20

Figure 10: Resistive evaporation technique *(Zhang and Hoshino, 2019)*................. 20

Figure 11: Illustrates the sputtering system *(Zhang and Hoshino, 2019).* 22

Figure 12: Oxidation of silicon (thickness of oxide grown layer was plotted against temperature and time) (*Lin, 2008).* 23

Figure 13: The effect of O_2 partial pressure on SiO_2 film thickness after thermally oxidizing (100) and (111) oriented substrate for 10 minutes at 850 °C and 1050 °C in O_2/N_2 mixtures *(Raider, 1980).* 26

Figure 14: Oxidation rate of (100) Si at 1150 °C in the presence of HCl and Cl_2 (Kriegler et al., 1972) 27

Figure 15: Illustration of the redistribution process for Case 1 – oxide takes up impurity, m<1 *(Grove et. al., 1964).*....29

Figure 16: Illustration of the redistribution process for Case 2 – oxide rejects impurity, m>1 (Grove et. al., 1964)....30

Figure 17: SOI wafer structure *(Seyit, 2014).*....32

Figure 18: Step used in the BSOI process *(Moriceau, H., 2014).*....34

Figure 19: Schematic representation of CMOS transistors based on silicon-on-insulator (SOI) wafer....36

Figure 20: Summary of thermal oxidation process....41

Figure 21: Wafer slices are kept in a petri dish....42

Figure 22: RCA cleaning process setup....43

Figure 23: Cross section of oxidation furnace *(Reed, 1998).*....45

Figure 24: Schematic diagram for illustrating Bragg's Law. (*Bragg, W.L., 1934)*...46

Figure 25: Jandel Multipurpose Four-Point Probe System....48

Figure 26: Schematic diagram for AFM operating principle. (*Boudaoud et al., 2014)*....49

Figure 27: Thin Film Analyzer with wafer on stage....50

Figure 28: XRD patterns for SOI wafer....52

Figure 29: Details of SOI wafer specification from the manufacturing company.....53

Figure 30: Cross section of SOI wafer by using SEM....54

Figure 31: Physical difference of SOI wafers at different temperatures....55

Figure 32: Linear and parabolic stage for dry oxidation process at 1100 °C *(Lin, 2008).*....57

Figure 33: SiO_2 thickness growth at 1000 °C....58

Figure 34: Thickness of oxide growth at 950 °C....59

Figure 35: Thickness of oxide growth at 900 °C....60

Figure 36: Thickness of oxide growth at 850 °C....61

Figure 37: Oxide thickness versus temperature and time. 62

Figure 38: Resistivity of SOI wafer at various temperatures. 64

Figure 39: Resistivity of SOI wafer at various oxidation temperature and time. 65

Figure 40: Topography of sample wafer by using AFM analysis at (a) 850 °C, (b) 900 °C, (c) 950 °C and (d) 1000 °C for oxidation time......................67

Figure 41: Surface roughness of wafer sample. 68

LIST OF SYMBOLS

a_1, a_2	Impurity's activity coefficient
C_G	Oxidant concentration
C_s	Concentration at surface
C_0, C_i	Concentrations at two interfaces
D	Oxidant diffusivity
d	Interplanar spacing in the crystalline phase
h_G	Mass transfer coefficient
n	Order of diffraction
x_0	Oxide thickness
θ	Angle between diffracted and transmitted beams
λ	Wavelength of the incident X-ray beam

LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopic
CVD	Chemical Vapor Deposition
DC	Direct current
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PVD	Physical vapor deposition
RF	Radio frequency
SC	Standard Cleaning
SEM	Scanning Electron Microscope
SOI	Silicon-on-insulator
USM	Universiti Sains Malaysia
XRD	X-Ray Diffraction

PENYIASATAN PROSES PENGOKSIDAAN DI ATAS WAFER SOI

ABSTRAK

Teknologi wafer SOI digunakan secara meluas dalam peranti mikroelektronik kerana kelebihannya yang telah digunakan untuk meminimumkan atau menghapuskan kebocoran substrat, dan meningkatkan prestasi reka bentuk. Mereka mempunyai kelajuan pantas, pengurangan ralat, penggunaan kuasa yang rendah, penskalaan yang meningkat, dan imuniti selak. Tujuan projek ini adalah untuk menyiasat dan mengkaji tahap ketebalan lapisan oksida yang boleh terbentuk pada wafer SOI setelah melalui proses pengoksidaan dengan pelbagai parameter dan pengaruhnya terhadap sifat elektrik wafer. Pada mulanya, wafer dipotong kepada 1cm x 1cm dan kemudiannya dibersihkan dengan menggunakan RCA Cleaning untuk membuang sisa organic, menghilangkan pencemaran atom logam ionik dan berat. Setelah itu, wafer memulakan proses pengoksidaan. Wafer SOI telah menjalani proses pengoksidaan pada suhu dari 850 °C hingga 1000 °C dan masa rendaman dari 1 jam hingga 7 jam dan aliran gas oksigen ditetapkan kepada 200 cc/min. Selepas proses pengoksidaan dilakukan, pertumbuhan ketebalan oksida pada wafer SOI akan dianalisis dengan menggunakan pengukur FilMetric. Didapati bahawa semakin tinggi suhu dan masa yang digunakan, semakin bertambah ketebalan oksida. Dengan menggunakan probe empat mata, kerintangan wafer SOI diukur dan ia menunjukkan bahawa apabila suhu dan masa pengoksidaan meningkat, kerintangan sampel wafer berkurangan. AFM digunakan untuk menganalisis kesan kekasaran permukaan wafer dan topografi wafer selepas proses pengoksidaan. Daripada keputusan AFM, dapat disimpulkan bahawa apabila suhu dan masa pengoksidaan meningkat, kekasaran permukaan sampel wafer meningkat.

INVESTIGATION OF OXIDATION PROCESS ON SOI WAFER

ABSTRACT

Silicon-on-Insulator, SOI wafer technology is widely used in microelectronic devices due to its advantages that have been used to minimize or eliminate substrate leakage and improve design performance. They have fast speeds, error reduction, low power consumption, increased scaling, and latch-up immunity. The purpose of this project is to investigate and study the degree of thickness of the oxide layer formed on SOI wafers after undergoing an oxidation process at various oxidation temperature and time and its influence on the electrical properties of the wafer. Firstly, wafer was cut by 1cm x 1cm size and cleaned by using RCA Cleaning to remove the organic residues ionic and heavy metal atomic contamination. In this study, SOI wafers undergo oxidation process at temperature from 850 ℃ to 1000 ℃ and soaking time from 1 hour to 7 hours at the oxygen gas flow fixed to 200 cc/min. After the oxidation process, the oxide thickness growth on the SOI wafer were be analyzed by using FilMetric measurement. It was found that oxide thickness increased as the oxidation temperature and time increased. By using four-point probe, the resistivity of the SOI wafer was measure and it shows that as the oxidation temperature and time was increased, the resistivity of the wafer sample is decreased. AFM were used to analyzed the effect of wafer surface roughness and wafer topography after the oxidation process. From the AFM results, it can be concluded that when the oxidation temperature and time were increased, the surface roughness of the wafer sample was increased.

CHAPTER 1

INTRODUCTION

1.1 Research Background

Thermal oxidation is used to develop a silicon dioxide layer on a silicon substrate. This process can be done by the thermal growth methods or other undesired native growth processes. However, there is a lack of research in thermal oxidation of SOI wafers. Thus, in this study, we explore more on the thermal oxidation of SOI wafers. In 1966, the first pattern-independent SOI structures were created using high-dose oxygen implantation *(Watanabi and Tooi, 1966)*. Unfortunately, Watanabe and Tooi's study has not been followed up on by more SOI research. However, in the 1970s Izumi and his colleagues proved that a device-quality SOI structure can be formed. They began experimenting with buried oxide production by ion implantation in 1976, using an Extrion 200-20a ion implanter *(Katsutoshi, 1998)*. Germanium was popular in the early days of semiconductor devices because germanium has a lower melting point. However, silicon has exceeded germanium and Ge easily be replaced due to the existence of a stable oxide for silicon that could be easily grown on the substrate. In 1991, when the silicon is kept in an oxygen rich environment at elevated temperatures, it will be oxidized which results in the formation of silicon dioxide, SiO_2 *(Katsutoshi, 1991)*.

Simply heating silicon in an oxygen-containing environment produces a high dielectric strength, electrically insulating SiO_2 layer at a low cost. Generally, the oxide layer can be formed by an oxidation process in an oxidation furnace at a temperature between 800°C to 1100°C. The oxidation reaction can be expressed as:

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \tag{1.1}$$

This SiO_2 layer is chemically and mechanically stable, efficiently passivates the surface states of the underlying silicon and creates an effective diffusion barrier for frequently used dopant species. It formed a pure glass with a melting point of 1730 ℃ and exhibited excellent dielectric properties *(Lin, 2008)*. The electric resistivity can reach 1×10^{20} Ω.cm and having energy band gap in around 9 eV *(Lin, 2008)*. A well-grown SiO_2 layer can withstand an electric field of up to 10^9 V/m without undergoing breakdown *(Lin, 2008)*. An SiO_2 has a dense structure that usually will fully cover the wafer and prevent the inner silicon from further oxidation *(Lin, 2008)*.

Thermal oxidation can be performed in oxidation furnaces during semiconductor wafer production. This oxidation furnace is an important element in semiconductor wafer manufacture. It is a basic thermal processing equipment that is used to oxidize semiconductor wafers at high temperatures. From past research, it is proven that the development of a high-quality SiO_2 has helped to establish the dominance of Si in the semiconductor industry. Generally, SiO_2 functions as an insulator in several device structures or as a barrier to diffusion or implantation during device fabrication. Depending on whether dry oxygen or water vapour is employed, there are two SiO_2 development methods: dry and wet oxidation. Dry oxidation is usually used to form thin oxide in a device structure because of its good Si-SiO_2 interface characteristics, whereas wet oxidation is used for thicker layers because of its higher growth rate. After the oxidation process, a SiO_2 layer is formed all over the wafer surface *(Gary and Simon, 2004)*.

1.2 Problem Statement

From the first invented of the SOI wafer, the researchers have discovered that SOI wafer had more advantageous when compared to bulk Si wafer. This has garnered the interest of researchers to develop more techniques in order to characterized more of these advantageous SOI wafer.

Past few years, researchers around the world had considered ways to improve the semiconductor devices. While there are many works done by other researcher on the application of the SOI wafer in semiconductor field, it has been realized that they are limited works have been done to investigate the parameters involved to grow SiO_2 on the SOI wafer and its properties by undergoing thermal oxidation process.

Formation of SiO_2 by thermal oxidation process is not new in the industry, however, the formation of the SiO_2 will be difficult if the growth parameters are not properly understood. The growth of SiO_2 depends on the process parameters such as temperature and growth time. This research is about the growth of SiO_2 by using thermal oxidation method. SOI wafer was used and oxygen gas, O_2 as the source of oxygen. Once the SiO_2 were formed, the samples were characterized by X-ray diffraction, SEM, Filmetrics, four-point probe and AFM.

1.3 Objective

The following objectives are expected to achieve in this research: -

i) To measure the oxide layer thickness growth on SOI wafers at various temperature and time.

ii) To investigate the electrical properties and surface roughness after thermal oxidation of SOI wafer.

1.4 Research Scope

The scope of this research is to thermally grow silicon dioxide by undergoing a thermal oxidation process. This process will be done in an oxidation furnace at various temperatures and time. The oxygen gas was used as the oxidation source to form the silicon dioxide on the wafer surface. Observation and analysis on the thickness layer of silicon dioxide form on the wafer surface was carried out. Such study is very crucial in determining the best parameter to grow the silicon dioxide by undergoing a thermal oxidation process.

1.5 Thesis Outline

Five parts were divided in this thesis which contains Chapter 1, Chapter 2, Chapter 3, Chapter 4 and Chapter 5. Chapter 1 discussed the introduction of the dissertation including background research, problem statement, objective of this research and the scope of the project in this research. Chapter 2 discussed on the overview on thermal oxidation on wafers, techniques to grow SiO_2, the factor growth of the oxide layer, and mechanism of the oxidation process in previous works or research that are closely related to this study. Chapter 3 discussed the summary of the thermal oxidation process and the characterization methods used in this project. Chapter 4 presents and discussed the results and findings of the experimental work done in this study. All methods mentioned in Chapter 3 will be used and discussed. Finally, Chapter 5 discussed the conclusion and the recommendation for future study.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

Nowadays, the semiconductor industry has tried its best to find the best materials to improve the performance of semiconductor devices. As the demand for advanced semiconductor devices is increasing, the semiconductor industry is conducting more in-depth research to improve the properties of semiconductor devices.

For over 50 years, many researchers in the world of semiconductor have focused their attention on the study of increasing the properties of semiconductor materials in the wafer industry. A large-scale study has been done on silicon semiconductor materials to improve the silicon wafer industry. Silicon has contributed greatly in the manufacture of semiconductors devices and the production of wafers.

By decades, silicon has become a favoured material in the integrated circuits industry when it shows a large bandgap which gives the ability to operate at high temperature and by having an extraordinary synergy with its oxide which is SiO_2. A high dielectric strength of SiO_2 can be formed by heating the silicon in oxygen. In this project, it shown that the oxide grow was affected by the oxidation temperature and oxidation time. The growth of SiO_2 also can be affected by the dopant concentration, dopant redistribution, wafer orientation and impurities. However, only oxidation temperature and time were studied in this project.

2.2 Thermal Oxidation

Thermal oxidation is a process of growing an oxide layer on the wafer surface. When the wafer is exposed to the oxygen gas, the surface of the silicon wafer will be oxidized and SiO_2 will be formed. Hence, this will produce a high-quality electrical insulator and can be used as barrier material during impurity diffusion. Due to these properties, silicon has become the leading material used for fabrication of semiconductor devices, focused on integrated circuits.

Thermal oxidation of SOI wafer can be achieved by heating the wafer at relatively high temperature in the range between 850 ℃ to 1000 ℃ with the exposure to the atmosphere containing oxygen gas. Upon the exposure to the oxygen, the silicon on the wafer surface will react with the oxygen gas and form silicon dioxide, SiO_2. This thermal oxidation process can be run in two modes which are dry oxidation process which use oxygen gas as the oxygen source or wet oxidation which use water as oxygen source.

Reaction for dry oxidation process:

$$Si + O_2 \rightarrow SiO_2 \tag{2.1}$$

Reaction for wet oxidation process:

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{2.2}$$

2.2.1 Mechanism of Thermal Oxidation Process

Silicon dioxide grows when a silicon atom reacts with oxygen gas. At first, a sample wafer is placed on the crucible. Then, it is placed in a heated chamber or oxidation furnace to undergo a thermal oxidation process. Figure 1 shows a basic thermal oxidation apparatus. The thermal oxidation apparatus consists of a resistance heater, a fused quartz tube which contains a silicon wafer sample, and a source which contains pure oxygen gas or water vapor. The oxidation parameter is then set according to the desired parameter.

The wafer is exposed to oxygen gas. Initially, oxygen and silicon react to generate SiO_2. The surface oxide layer must now be exceeded by other oxygen atoms that must diffuse through the dioxide layer to react with the silicon crystal underneath. As a result, the growth rate is mostly controlled by the reaction time of oxygen and silicon, but the oxidation rate is primarily determined by the velocity of oxygen diffusion through silicon dioxide at a given thickness. The rate of growth slows as the thickness of the silicon dioxide increases.

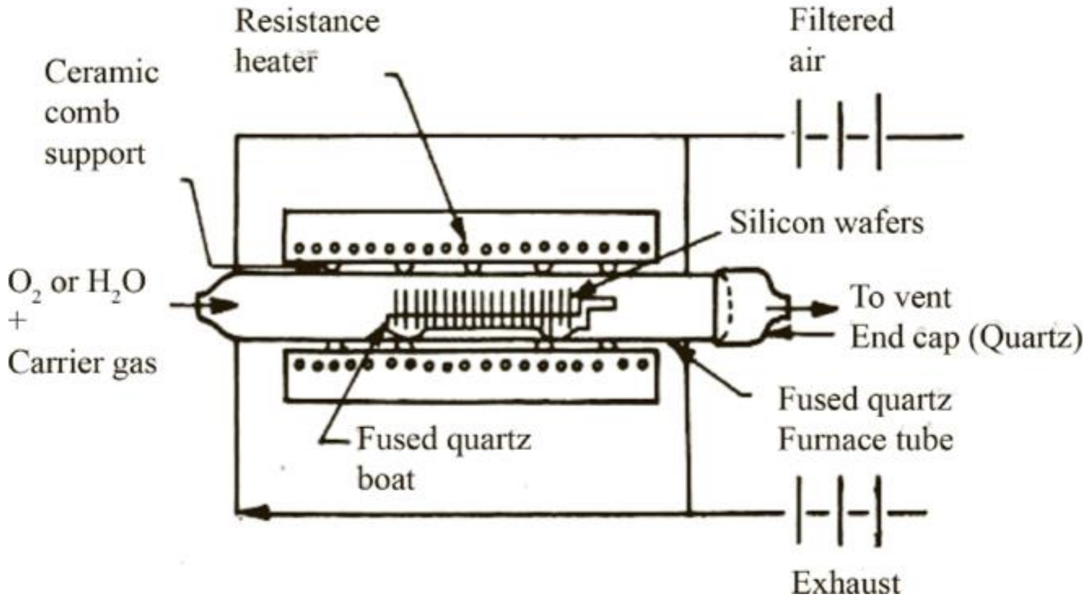
Resistance heater
Filtered air
Ceramic comb support
Silicon wafers
O₂ or H₂O + Carrier gas
To vent
End cap (Quartz)
Fused quartz Furnace tube
Fused quartz boat
Exhaust

Figure 1 Basic thermal oxidation apparatus *(Sze and Lee, 2012)*.

2.2.2 Growth of Silicon Dioxide

The SiO_2 that forms on the wafer surface is called oxide growth. The oxide growth can have various thicknesses which are affected by the various parameters set in this experiment. Different thickness of oxide growth will give a different effect to the properties of the wafer and semiconductor devices.

Figure 2 shows the oxide thickness for wet oxidation process and Figure 3 shows the oxide thickness for dry thermal oxidation reported by Deal and Grove *(Deal and Grove, 1965)*. Referring to Figure 2, wet oxidation has a faster growth rate than dry oxidation. This is due to the wet oxidation process using water vapor instead of oxygen, in which water molecules are smaller than oxygen molecules and diffuse faster through silicon dioxide. However, by undergoing a wet oxidation process, the oxide films tend to be porous. Opposite to the wet oxidation process, the dry oxidation process has a much slower growth rate but has the advantage of being more controllable, giving a denser oxide growth and a much cleaner oxide growth layer.

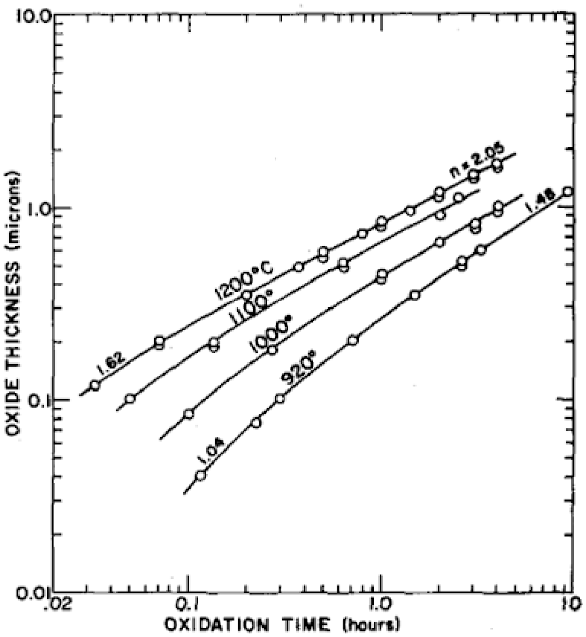

Figure 2: Wet oxidation process on silicon wafer *(Deal and Grove, 1965)*.

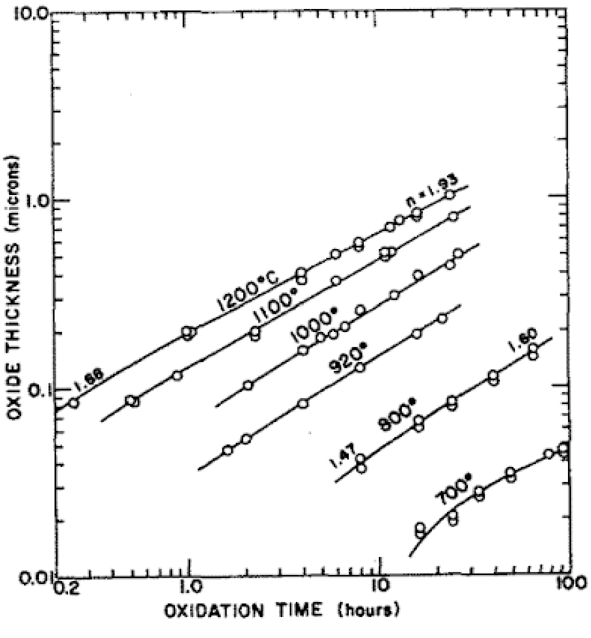

Figure 3: Dry Oxidation Process on Silicon Wafer *(Deal and Grove, 1965)*.

To vary the oxide thickness, various parameters are used which is the oxidation temperature is set. The oxidation temperature is increased linearly from low temperature to the oxidation temperature set so that the wafer will not wrap due to sudden temperature change. Oxygen flow is directed as shown in Figure 1 by the arrow.

During the early stages of oxide growth, the oxide thickness varies linearly with time and temperature. As the oxide becomes thicker, the oxidant must diffuse through the oxide layer to react at the silicon-silicon dioxide interface, and the reaction becomes diffusion limited. The oxide growth then becomes proportional to the square root of oxidizing time, which results in a parabolic growth rate.

It was noted earlier that for dry oxidation, there is apparently rapid oxidation that gives rise to an initial oxide thickness of about 20 nm. In the early stage of growth in dry oxidation, there is a large compressive stress in the oxide layer that reduces the oxygen diffusion coefficient in the oxide. As the oxide becomes thicker, the stress is reduced because of the viscous flow of the silica and the diffusion coefficient will approach its stress-free value.

2.2.3 Properties of Silicon Dioxide

Silicon dioxide, SiO_2 is an amorphous substance that form of pure glass with a melting temperature of 1730 °C which is similar to fused silica *(Lin, 2008),* that used in microsystems as a dielectric in capacitors and transistors as an insulator to separate various electronic devices and as a structural or sacrificial layer in several micromachining techniques. Silicon dioxide can be easily grown or deposited on silicon surface wafers using a variety of techniques. With resistivity values as high as 10^{20} Ωm, and having a energy band gap around 9 eV (*(Lin, 2008),* high-quality oxide coatings provide excellent electrical insulation. A well grown silicon dioxide layer can sustain a high electric field of up to 10^9 V/m without breakdown *(DiMaria et al., 1992)*. It is also a good thermal insulator by having a thermal conductivity of roughly 1.4 W/m-K *(Sze and Lee, 2012).*

When oxide layers are formed or coated on a substrate, the residual stress is always compressive, on the order of 1 GPa. As a result, the design and size of micromechanical structures composed of oxide are regulated to avoid mechanical buckling upon release from the substrate. Table 1 shows the deposition processes and characteristics of silicon dioxide films. In general, deposition temperature and film quality are directly related. At higher temperatures, deposited oxide coatings are structurally comparable to thermally formed silicon dioxide.

Table 1: Properties of SiO_2 growth by using various source of oxygen *(Sze and Lee, 2012).*

Property	Thermally grown at 1000°C	$SiH_4 + O_2$ at 450°C	TEOS at 700°C	$SiCl_2H_2 +$ N_2O at 900°C
Composition	SiO_2	SiO_2(H)	SiO_2	SiO_2(Cl)
Density (g/cm^3)	2.2	2.1	2.2	2.2
Refractive Index	1.46	1.44	1.46	1.46
Dielectric Strength (10^6 V/cm)	>10	8	10	10
Etch rate (A/min) (100:1 H_2O:HF)	30	60	30	30
Etch rate (A/min) (buffered HF)	440	1200	450	450
Step coverage	-	Nonconformal	Conformal	Conformal

Lower densities exist in films formed at temperatures below 500 °C. Densification occurs when deposited silicon dioxide is heated between 600 °C and 1000

°C, causing the oxide thickness to drop while the density increases to 2.2 g/cm^3. At a wavelength of 0.6328 μm, silicon dioxide has a refractive index of 1.46. Lower-index oxides are porous, such as the oxide formed via silane-oxygen deposition, which has a refractive index of 1.44. The porous nature of the oxide also contributes to a lower dielectric strength and, as a result, a larger leakage current in the oxide layer. Oxidation rates in a hydrofluoric acid solution are affected by deposition temperature, annealing history, and dopant content. Higher-quality oxides are often etched at slower speeds *(Sze and Lee, 2012)*.

2.2.4 SiO_2 Crystal Structure

As shown in Figure 4 (a), the basic structural unit of thermally grown silicon dioxide is a silicon atom surrounded tetrahedrally by four oxygen atoms. These tetrahedra are connected at their corners in a variety of ways by oxygen bridges to produce the different phases or structures of silicon dioxide, generally known as silica. Silica contains a variety of crystalline structures, including quartz and amorphous structures. When silicon is thermally oxidized, the structure of silicon dioxide becomes amorphous. The main difference between crystalline and amorphous is that crystalline has periodic structure whereas amorphous does not, as seen in Figure 4 (c).

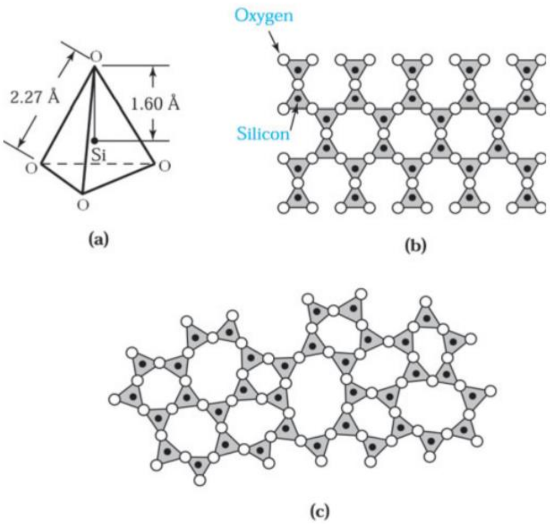

Figure 4: (a) Structure of thermally grown silicon dioxide. (b) Two-dimensional image of crystalline structure of silicon dioxide. (c) Two-dimensional image of amorphous structure of silicon dioxide *(Sze and Lee, 2012)*.

Deal and Grove initially proposed the mechanism for silicon oxide formation in 1965 *(Deal and Grove, 1965)*. To estimate the oxide thickness, a mathematical model is used which is given by the Deal-Grove model *(Deal and Grove, 1965)*:

$$t = \frac{X^2 + AX}{B} \tag{2.1}$$

where, t : Process time
X : Oxide thickness
A and B : Parameters for each oxidation condition (temperature, etc.)

During oxidation, the Deal-Grove model defines two development stages: linear and parabolic. The one-dimensional model for the oxidant flow from the gas phase to the silicon surface during thermal oxidation is shown in Figure 5. Equations 2.2 – 2.4 offer three first-order equations defining the three series components of the sample fluxes, namely F1, F2, and F3, in the one-dimensional model.

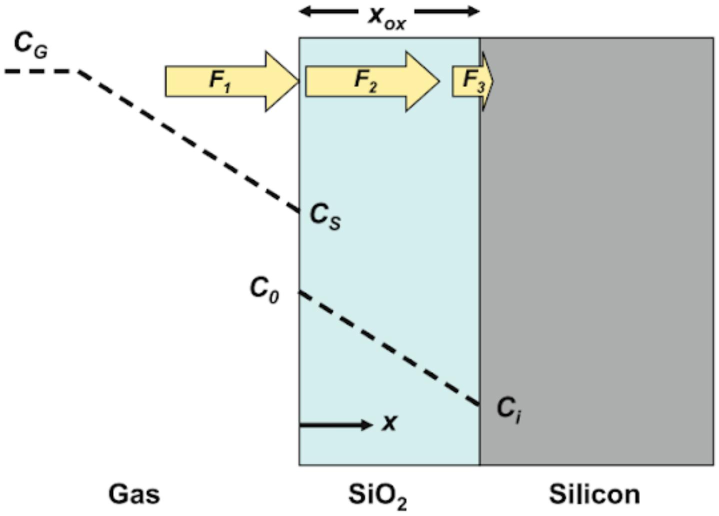

Figure 5: Model for oxidant diffusion from the gas phase to silicon surface during thermal oxidation.

F_1 represents the gas transport flux in molecules per square centimetre per second, F_2 represents the diffusion flux through the oxide layer and may be calculated using Fick's first rule, and F_3 represents the reaction flux at the SiO2/Si interface:

$$F_1 = h_G (C_G - C_S) \tag{2.2}$$

$$F_2 = -D\frac{\partial C}{\partial X} = D\,\frac{(C0 - Ci)}{X0} \tag{2.3}$$

$$F3 = k_sC_i \tag{2.4}$$

where h_G represents the mass transfer coefficient (molecules per cm^2s), C_G the oxidant concentration, Cs the concentration at the surface, D the oxidant diffusivity in the oxide (cm^2/s), C_0 and C_i the concentrations at the two interfaces, x_0 the oxide thickness, and k_s the reaction rate constant (cm/s). Given the assumption of steady-state circumstances, the three fluxes reflecting the various phases of the oxidation process must be equal. The processes run in parallel, and the overall process speed is defined by the pace of the slowest process. Equating all fluxes results in:

$$F\ (F1 = F2 = F3) = \frac{C*}{\frac{1}{ks}+\frac{1}{h}+\frac{X0}{D}} \tag{2.5}$$

The total rate of oxidation is proportional to the flow of oxidant molecules,

$$\frac{dx}{dt} = \frac{F}{N} = = \frac{C*/N}{\frac{1}{ks}+\frac{1}{h}+\frac{X0}{D}} \tag{2.6}$$

where N is the number of oxidant molecules per unit volume of oxide grown. N = 2.2 x 10^{22} cm^{-3} for dry oxidation and is approximately double that value for wet oxidation. Note that M = density / (Avogadro's number × molecular weight of SiO_2). Take the boundary condition of $x_o = x_i$ at t = 0. The oxide growth kinetics can be obtained by integrating equation 2.6 from an initial oxide thickness x_i to a final thickness x_o. The differential equation may be rewritten as:

$$\frac{x_{ox}^2}{B}+\frac{x_{ox}}{B/A} = (t + \tau) \tag{2.7}$$

where,

$$A = 2D\left(\frac{1}{k_s} + \frac{1}{h}\right),\ B = \frac{2DC_A}{N},\ \tau = \frac{x_i^2 + Ax_i}{B}$$

The terms B and B/A can be referred to as parabolic and linear constants for describing the oxide growth kinetics. The oxidant diffusion and interface reaction rates are the physical meanings of the rate constants B and B/A.

2.3 Other Technique of Silicon Dioxide Deposition

Other than thermal oxidation methods, silicon dioxide may be deposited using other alternative processes such as CVD and others. In this section, the alternative processes are discussed. However, this other technique cannot replace the thermally grown oxides due to the best electrical properties obtained with thermally grown films.

2.3.1 Chemical Vapor Deposition (CVD)

Chemical vapor deposition is a technique for depositing a variety of different materials including dielectric, semiconductors, and metals. CVD is most used for polysilicon, insulators such as SiO_2, and certain metals such as tungsten. This process will involve a chemical reaction. The film components are delivered by reactants in the form of gasses in CVD, offering better control over process parameters and reducing contamination. The higher temperature drives the reaction in conventional CVD. The reaction that forms the film should ideally occur exclusively on the wafer surface. If the reaction happens in the gas stream or known as gas-phase nucleation, particles will develop instead of a robust film.

CVD is commonly carried out at low pressures ranging from 0.15 to 2 torr. The apparatus is similar to oxidation furnaces, except the tube is sealed and evacuated. Because many of the gasses employed in CVD are poisonous and pyrophoric, the exhaust stream must be handled with extreme caution. In general, CVD equipment is constructed so that reactant movement limits the rate of deposition. To measure the flow of reactant gasses into the chamber, precise mass flow controls are required. Temperature control is only required to a few degrees, which is far less than what is necessary for a reaction rate limiting process like silicon oxidation. SiO_2 films are created by reacting silane with an oxidant, often oxygen or N_2O. Suitable oxide films can be produced at 450 °C or lower.

A typical CVD system is schematically illustrated in Figure 6. Different gasses are combined under regulated conditions and made to react with each other depending on the desired film. The deposited film is generally a by-product of the interaction between the multiple gas molecules, but it may also be the result of the decomposition of a single gas.

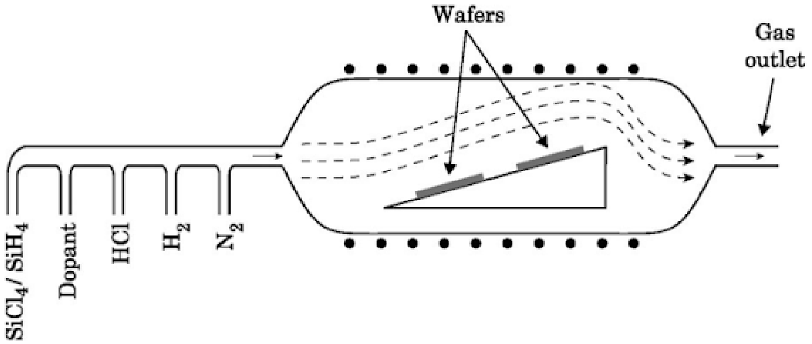

Figure 6: A typical CVD system with heater elements around the chamber and gas inlet *(Bahreyni, 2008)*.

The CVD processes can be categorized based on the pressure inside the chamber during the process. In 1960, the atmospheric pressure CVD or APCVD was performed at an elevated temperature range of 700 °C to 1250 °C. After a decade, the low-pressure CVD or LPCVD systems were introduced and replaced APCVD ones in most applications. When utilizing CVD, the procedure is carried out at atmospheric pressure in the CVD reactor, whereas LPCVD is carried out at lower pressure. The films are generated by reacting silane, dopant, and oxygen at low temperatures ranging from 300 °C to 500 °C. The chemical reactions are:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \tag{2.8}$$

$$4PH_3 + 5O_2 \rightarrow 3P_2O_3 + 6H_2 \tag{2.9}$$

Silicon dioxide may be deposited at intermediate temperatures ranging from 500 °C to 800 °C by decomposing tetraethyl orthosilicate, Si (OC_2H_5), also known as TEOS, in an LPCVD reactor. The liquid source vaporizes the chemical TEOS. The TEOS compound decomposed as follows:

$$Si\,(OC_2H_5) \rightarrow SiO_2 + \text{by products} \tag{2.10}$$

This results in SiO_2 and a combination of organic and organosilicon by-products. A higher temperature is required, which is appropriate for polysilicon gates requiring a homogeneous insulating layer with adequate step coverage. The improved step coverage improves surface mobility at elevated temperatures *(Gary and Simon, 2004).*

Silicon dioxide is generated for high-temperature deposition up to 900 °C by combining dichlorosilane, $SiCl_2H_2$, with nitrous oxide at low pressure as follows.:

$$SiCl_2H_2 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2HCl \qquad (2.11)$$

This deposition method produces high film uniformity and is often used to build insulating layers. The advantages of LPCVD over APCVD film include better uniformity, lower processing temperature, and less dependence on gas dynamics inside the chamber.

2.3.2 Plasma-Enhanced Chemical Vapor Deposition (PECVD)

For some reason, PECVD was developed. PECVD is an energy-enhanced CVD technology that adds plasma energy to a typical CVD system's thermal energy. Figure 7 depicts a parallel-plate, radial-flow PECVD reactor with a cylindrical glass or aluminium chamber sealed with aluminium endplates. There are two parallel metal electrodes within. The top electrode is subjected to a radio frequency voltage, while the bottom electrode is grounded. A plasma discharge occurs between the electrodes as a result of the radio frequency voltage. Wafers are put on the bottom electrode, which is heated by resistance heaters to temperatures ranging from 100 °C to 400 °C. The reaction gasses enter the discharge through inlets placed around the bottom electrode's perimeter. This reactor's key benefit is its low deposition temperature. However, it has a limited capacity, particularly for large-diameter wafers, and the wafers may get contaminated if loosely adhering deposits fall on them.

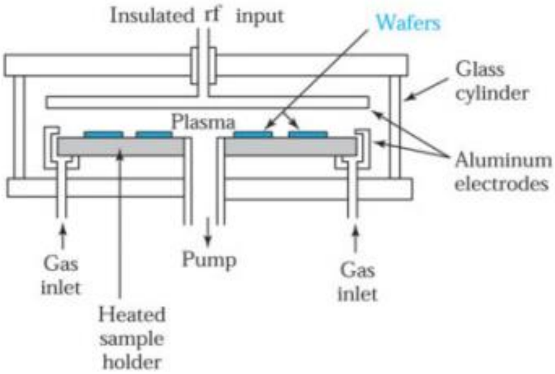

Figure 7: Parallel-plate radio frequency (rf) plasma deposition reactor (*Sze and Lee, 2012).*

PECVD's low temperature, self-cleaning capabilities, and varied film tunability have ensured its prominence in the semiconductor industry. Limiting the plasma area helps to reduce deposits on reactor surfaces. The typical parallel-plate layout is an efficient design for concentrating deposition on the wafer. Simultaneously, the reactor's plasma capacity allows for in-situ plasma cleaning by adding etchant cleaning gasses such as C_2F_6 or NF_3 to remove silicon dioxide and silicon nitride deposits from chamber surfaces.

2.3.3 Evaporation Deposition

Physical evaporation is one of the oldest methods of depositing films. Evaporation is another process but commonly used to deposit thin metal sheets. When a material is heated in a vacuum, it evaporates and emits vapor particles that go directly to the target substrate and condense back into a solid form *(Zhang and Hoshino, 2019)*. To minimize the negative impacts of current pollutants in the environment, the entire process is carried out under vacuum at low pressures (Bahreyni, 2008).

Traveling particles may react with background gas or other unknown particles to generate unwanted films if they collide. A higher vacuum produces higher-quality films. Before heating the source material, a vacuum pressure of about 10^{-4}Pa or less is commonly achieved. Evaporation is a kind of deposition known as physical vapor deposition (PVD) because it does not involve any chemical interactions which in contrast to CVD that relies on chemical reaction *(Michael and Gary, 1998)*.

Figure 8 illustrates the setup of an evaporation system. A big bell jar is evacuated to a low base pressure, often less than 10^{-7} torr. The less contaminants integrated into the expanding film, the lower the base pressure. The substrates are positioned at the top of the vacuum chamber, with the side that will receive the film facing down. The substance to be deposited is transformed into a vapor, which condenses on the substrates. There are two types of evaporation apparatus that are commonly used which are e-beam evaporation and resistive heat evaporation.

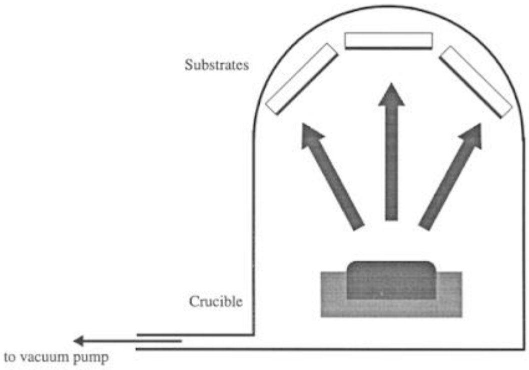

Figure 8: Basic setup of an evaporation system *(Michael and Gary, 1998)*.

E-beam evaporation uses thermal emission of electrons from a filament to heat samples. To eliminate direct contamination from the filament, a magnetic field is utilized to bend the electron beam by 270°. Electron beams can be used to evaporate materials that require high temperatures. They are also suitable for bigger sample volume deposition. Figure 9 shows the thermal evaporation technique for e-beam evaporation.

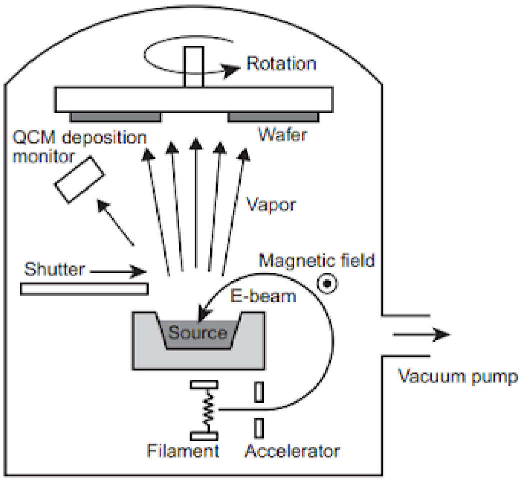
Rotation
QCM deposition monitor
Wafer
Vapor
Shutter
Magnetic field
E-beam
Source
Vacuum pump
Filament
Accelerator

Figure 9: E-beam evaporation technique *(Zhang and Hoshino, 2019)*.

Resistive evaporation technique induced by a current passing through a filament, or a metal plate known as an evaporation boat which holds the materials to be evaporated. This method is usually used for low-cost or small sample volume deposition systems due to its composition of the tool being simple. This deposition suited the organic materials that usually required a mild heat process rather than more intense e-beam heating. Figure 10 shows the resistive evaporation system.

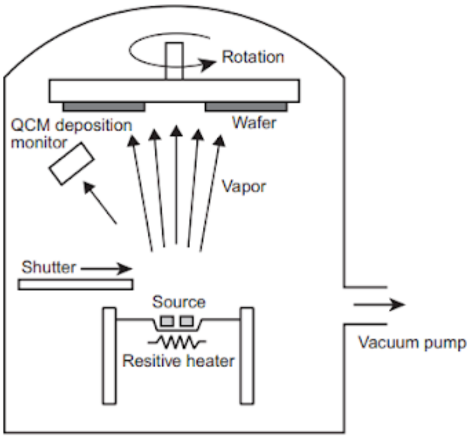
Rotation
QCM deposition monitor
Wafer
Vapor
Shutter
Source
Resitive heater
Vacuum pump

Figure 10: Resistive evaporation technique *(Zhang and Hoshino, 2019)*.

Limitation of Evaporative Deposition

As evaporation deposition is conducted at a high temperature, internal tension is created when the wafer is returned to room temperature due to the difference in thermal expansion coefficients of the wafer and the deposited material. This tension, or mismatch at the interface, may bend the wafer or cause the deposited film to peel off from the substrate on its own. As a result, evaporation is ineffective for creating a very thick layer. Electroplating can be used to deposit metal layers thicker than a few micrometres. Besides, evaporation deposition has a nonuniformity of coverage over wafer or multiple wafers and needs a longer time to pump down the pressure of the chamber due to low vacuum.

2.3.4 Sputtering Deposition

Sputtering is also categorized in physical vapor deposition, PVD. Atoms are expelled from a solid target material as a result of plasma bombardment in this process. Metals, metal alloys, metal oxide, metal nitride, silicon, silicon oxide, and silicon nitride are among the materials deposited by sputtering. Sputtering is another physical approach for coating a substrate with a thin layer of a target substance that does not involve chemical reactions. A flow of relatively heavy ions is used to knock off atoms at the surface of the target material, which then falls on the surface of the substrate and progressively creates a film of the substance.

In a normal procedure, the chamber is first emptied before introducing the sputter gas. To create a plasma, a DC or RF voltage is supplied between the target and the substrate. The sputter gas is typically an inert gas such as argon, although reactive gasses such as oxygen can also be mixed in. If the silicon is sputtered with oxygen, deposition of silicon oxide films may occur. Figure 11 illustrates the sputtering system.

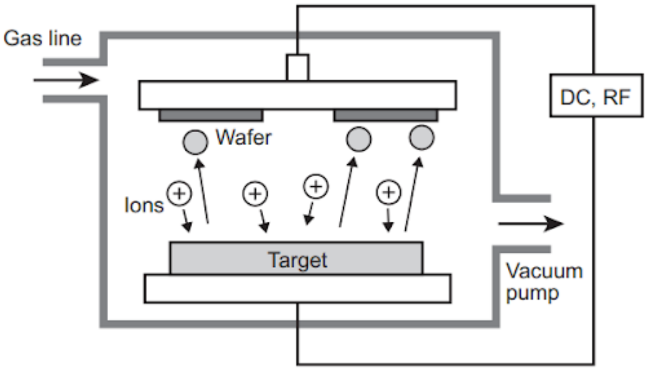

Figure 11: Illustrates the sputtering system *(Zhang and Hoshino, 2019).*

Limitation of Sputtering Deposition

Due to the difference in thermal expansion coefficient of the film and substrate, stress in the film occurs which leads to the wafer bowing or film peeling. This phenomenon usually occurs at high temperatures where the thermal expansion mismatch with the substrate. This limitation is also introduced in evaporation deposition. In addition, sputtering has poor conformality on sidewalls. Thus, the materials were difficult to fill. Scattering events cause the top opening of the hole to seal before appreciable materials have deposited on its floor.

2.4 Silicon Dioxide Growth Factor

2.4.1 Effect of Oxidation Temperature and Time

Solving Equation (2.7) yields the following connection between oxide thickness and growth time:

$$X_{ox} = \frac{A}{2}\left\{ \sqrt{1 + \left[\frac{t+\tau}{\frac{A^2}{4B}}\right] - 1} \right\} \tag{2.12}$$

With two limiting examples of t → 0 (small x_{ox}) and t → ∞ (large x_{ox}), we get the following formulas that match to Equation (7):

$X_{ox} \rightarrow \frac{B}{A}t$ when $t \rightarrow 0$ and $X_{ox} \rightarrow \sqrt{Bt}$ when $t \rightarrow 0$

The thickness of the produced oxide layer changes linearly with temperature and time at the start of oxidation. The reaction occurring at the SiO_2-Si contact at this stage, known as the reaction rate-controlled region, controls the rate of oxide development. The linear stage of oxide growth is valid up to around 15 nm of oxide thickness (Ganem et. al., 1993). Figure 12 below shows the oxidation of silicon where the thickness of oxide grown layers were plotted against temperature and time.

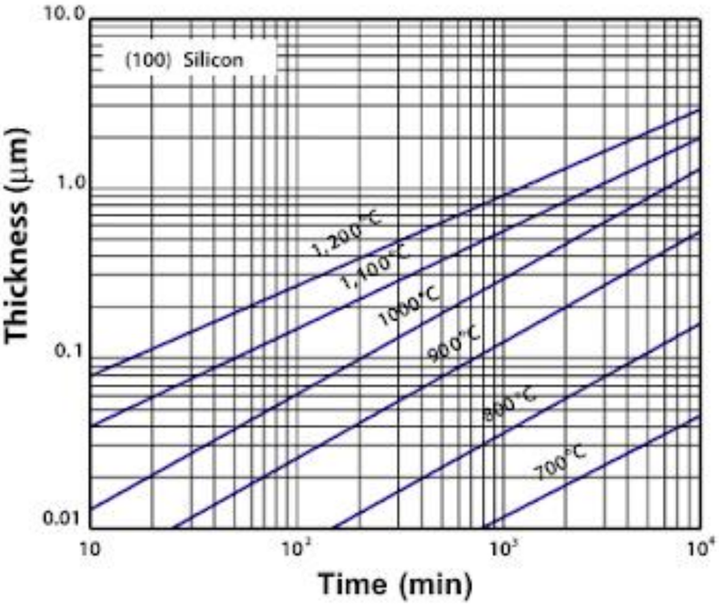

Figure 12: Oxidation of silicon (thickness of oxide grown layer was plotted against temperature and time) (*Lin, 2008).*

2.4.2 Effect of Dopant Concentration

The concentration of dopants in silicon also determines the pace of oxide formation. Doping during the oxidation process is another significant parameter that may alter the oxide development rate. In general, strongly doped silicon oxidises quicker than weakly doped silicon. Boron doping will oxidise quicker than phosphorus during the parabolic stage. However, the linear rate constant between boron and phosphorus doping indicates minimal change in growth rate *(Choi, 1987).*

2.4.3 Effect of Wafer Orientation

The crystal orientation influences the silicon oxidation process. The oxidation rate increases in the linear growth rate area in the same general order as the available surface bond density (100) < (110) < (111) *(Bean and Gleim, 1969)*. The oxidation process occurs between a silicon bond and a water molecule that migrates from an interstitial location in the silica film at the silica-silicon interface.

The number of available bonds per cm^2 increases in the same order as previously stated (100) = 6.77×10^{14}, (110) = 9.39×10^{14} and (111) = 11.76×10^{14} *(Bean and Gleim, 1969)*. It is also worth noting that the oxidation rate rises with decreasing crystallographic plane surface energy (100) 2130 ergs/cm^2, (110) 1510 ergs/cm^2, and (111) 1230 ergs/cm^2 respectively.

The following oxidation rates versus orientation have been recorded for thermally produced steam oxide at 1100 °C along the linear section of the thermal oxidation curve:

(100) = 5.02 Ǻ/s

(110) =5.77 Ǻ/s

(111) = 5.80 Ǻ/s

This corresponds to a 13% quicker growth rate on the (111) than on the (100). It should be noted that the reasoning and statistics presented here only pertain to the linear component of the growth rate versus time curve.

At the same oxidation temperature and oxidant pressure, substrates with orientated surfaces oxidise more rapidly than substrates with (100) orientations *(Raider, 1980)*. Single crystal Si substrates with (111) oriented surfaces oxidise more rapidly in oxygen and water vapour ambient at a given oxidation temperature and oxidant pressure than substrates with (100) orientations.