INVESTIGATION OF BORON SPIN ON DOPANT ON SOI WAFER

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INVESTIGATION OF BORON SPIN ON DOPANT ON SOI WAFER

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DECLARATION

I hereby declare that I have conducted, completed the research work and written the dissertation entitled '**Investigation of Boron Spin On Dopant on SOI Wafer**'. I also declare that it has not been previously submitted for the award of any degree and diploma or other similar title of this for any other examining body or University.

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SIASATAN TERHADAP BORON PENDOP PUTARAN DI ATAS WAFER SOI

ABSTRAK

Dalam penyelidikan ini, kerja-kerja tertumpu kepada teknik doping wafer SOI jenis p dengan menggunakan proses resapan haba. Matlamat penyelidikan ini adalah untuk menyediakan doped wafer SOI jenis p oleh SOD dengan dopan boron. Kaedah ini digunakan untuk menyediakan sumber kekotoran untuk wafer SOI. Dopan mula-mula merebak ke dalam substrat melalui SOD dan kemudian meresap dengan proses resapan haba pada 700˚C, 800˚C, 800˚C dan 1000˚C. Pelbagai instrumen pencirian digunakan untuk menyiasat sifat teknik SOD pada doping. Kuar empat mata telah dilakukan untuk mendapatkan kerintangan dan rintangan kepingan wafer SOI terdop. Kerintangan berkurangan serta rintangan kepingan dengan peningkatan masa dan suhu resapan. Kepekatan dopan meningkat apabila masa resapan dan suhu meningkat. Kekasaran permukaan wafer SOI terdop selama 120 minit resapan dianalisis menggunakan AFM. Daripada analisis, nilai RMS diperoleh untuk menggambarkan kekasaran permukaan selepas resapan haba. Daripada keputusan, kekasaran permukaan sekitar 30.0 nm hingga 80.0 nm diperoleh dengan peningkatan suhu resapan. Walau bagaimanapun pada 900˚C, nilai RMS telah berkurangan disebabkan oleh kesan etchant. Sebagai kesimpulan, suhu resapan terma yang dipilih adalah pada 900˚C akan membawa kepada hasil SOD yang terbaik kerana ia mempunyai kepekatan tinggi, ketumpatan pembawa yang tinggi, mobiliti yang lebih rendah dan kekasaran permukaan yang paling rendah iaitu nilai 7.17E+15cm^{-3}, 8.506E+14 $1/\mathrm{cm}^2$, 4.885E+2 $\mathrm{cm}^2/\mathrm{vs}$ and 34.92nm dan masing-masing 34.92nm.

INVESTIGATION OF BORON SPIN ON DOPANT

ON SOI WAFER

ABSTRACT

In this research, works were focused on the doping technique of p-type SOI wafers by using thermal diffusion process. The aim of this research was to prepare doped of p-type SOI wafer by SOD with boron dopant. This method is used to provide an impurity source for SOI wafer. The dopant was first spread into the substrate via SOD and then diffused by a thermal diffusion process at 700˚C, 800˚C, 800˚C and 1000˚C. Various characterization instruments were used to investigate the properties of SOD technique on doping. Four-point probe was done to obtain the resistivity and sheet resistance of doped SOI wafer. The resistivity was decrease as well as sheet resistance with increasing the diffusion time and temperature. The dopant concentration was increased as the diffusion time and temperature increased. The surface roughness of doped SOI wafer for 120 minutes of diffusion were analyse using AFM. From the analysis, RMS values were obtained to describe the surface roughness after thermal diffusion. From result, the surface roughness around 30.0 nm to 80.0 nm were obtained with increasing diffusion temperature. However, at 900˚C, the RMS value was decrease due to etchant effect. To conclude, the selected thermal diffusion temperature is at 900˚C would lead to the best result SOD as it has high concentration, high carrier density, lower mobility and lowest surface roughness which the value of 7.17E+15cm^{-3}, 8.506E+14 $1/cm^2$, 4.885E+2 cm^2/vs and 34.92nm respectively.

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LIST OF SYMBOLS

Rq	RMS roughness
Rs	Sheeet resistance
μ_p	Mobility

LIST OF ABBREVIATIONS

SOI	Silicon on Insulator
XRD	X-Ray Diffraction
SEM	Scanning Electron Microscope
AFM	Atomic Force Microscopy
RMS	Root Mean Square
USM	Universiti Sains Malaysia

INTRODUCTION

1.1 Research Background

SOI technology was developed during the 1980s for high-frequency and radiation-hard circuit applications (Lasky,1986). High-frequency and power devices have mostly been fabricated using silicon on insulator (SOI) wafers which perform very efficiently for MEMS (microelectronics-mechanical-systems), and CMOS integrated circuit fabrication purposes. This is because SOI wafers have abilities to improve many processes efficiently compared to other Si wafers because a tiny layer of insulator separates the layer of single-crystalline silicon from the bulk substrate. SOI technology offers many advantages in microelectronic devices compared to bulk silicon such as increase operating speed of devices by 20-30% because of the devices fabricated over the bulk silicon operate at relatively low switching speed because of the presence of the large volume of semiconductor material underlying the devices and hence more charge is needed to turn on and off. Other than that, this technology also helps to minimizes the current leakage and lower the power consumption in semiconductor devices because of lower parasitic device capacitances due to isolation from the bulk silicon substrate (Oleg and Bich, 2014).

Overall, SOI structures acquired specific interest because they overcome the electrical issues facing standard bulk silicon devices. However, contamination with metallic impurities can occurs during fabrication of SOI wafer originate from number of sources such heating element release volatile contaminant which diffuse through quartz furnace tube. Therefore, it can result in problem of degradation the electrical properties which significantly impact the reliability of semiconductor devices. Therefore, there are some techniques that can undergo to improve the properties of semiconductor devices.

The electrical properties of semiconductor can be improved to make them useful for electronic devices fabrication is their conductivity which can modified by process called doping. This process using chemical impurities has been crucial to the formation of today's cutting-edge semiconductor technologies (Gupta et al., 2017).

This is because the doping is a process of introducing impurities into the intrinsic semiconductor to improve the electrical which produce n-type and p-type semiconductors. The intrinsic semiconductor is normally doped with trivalent and pentavalent elements. When a material is doped with a trivalent impurity such as boron or gallium, it will produce p-type semiconductor. A p-type semiconductor is a semiconductor that has been doped with electron acceptor atoms. The P (positive) indicates that semiconductor has a lot of holes or positively charged particles. However, when the material is doped with group five element such as phosphorus or arsenic, n-type of semiconductor is produced. A n-type semiconductor is an extrinsic semiconductor that has been doped with electron acceptor atoms. The N (negative) indicates negatively charged ions, or extra electrons. Donors and acceptors are the two types of impurities that can be used to modify the conducting characteristics of a semiconductor. Donors are atoms with five electrons in their outer orbital, and acceptor are atoms with four electrons in their outer orbital.

There are some processes of doping that can be used which is spin on dopant and ion implantation. In this research, the process of doping was done on p-type of SOI wafer by using spin on dopant technique. This technique is widely use in market as it low cost and easier to handle in the semiconductor industry. This technique uses chemical agent such as boron, phosphorus arsenic, antimony and other substances are commonly used. However, the use of this agent depends on what type of semiconductor that will be

produced. In this study, boron dopant was applied on p-type SOI wafer using spin on dopant technique using spin coater. It can be applied by spinning, spraying or dip-coating methods. Application of spinning using spin coater is a preferred method because the thickness of the coating can be controlled by varying the spin rotation.

The process of activating dopant atoms is referred to as thermal diffusion such as thermal diffusion and drive-in. The semiconductor receives energy in the form of heat. This energy must be high enough for dopant atoms to displace silicon and form bonds with their neighbours. The temperature at which the dopants are annealed is a main indicator of how many of the dopant activate. There is no formation of p-n junction because the SOI wafer was doped with the same type of dopant with the host region. Therefore, it will increase the concentration of dopant atom in the localize4 region. However, if this technique uses different type of doping, it will create p-n junction which will activate the dopant.

1.2 Problem Statement

In this technology era, we are more dependent on electronic devices which help us to make our daily work become easier either for communication and other application. Thus, the reliability and efficiency of electronic devices is becoming more important in our lives. There are competitive of innovation and solution to meet the requirement of devices to work better. However, some of the technique is not worth as it has common issue such as high cost and difficult to handle the process successfully. There are several techniques that can be used to improve the electrical properties of semiconductor devices which will help to overcome the issue.

Doping is the technique that help to solve this issue in order make the device performance better by modify its electrical properties. The doping techniques of

diffusion and ion implantation help to introduce a controlled quantity of dopants into semiconductors and to improve conductivity. In this work, the electrical measurement of boron doped SOI wafer by SOD via diffusion were investigated. During that process, the concentration of the dopants can be tuned by changing the reaction conditions, such as temperature and time. (Nolan and co-worker, 1999) were the first to fabricate boron diffusion from a spin on dopant source during rapid thermal processing. (Nolan and co-worker, 1999) analyse phosphorus diffusion in silicon on insulator thin film via SOD (Chiara et al., 2020). This method was utilized to provide an impurity source for the development of semiconductor junctions.

In this work, the aims of experiment were to investigate the boron spin on dopant via thermal diffusion process. This is because this technique is cost-effective that can focus on the same purpose of improving the electrical properties of semiconductor. The dopant concentration and electron mobility were characterized at room temperature by four-probe and Hall Effect measurements. The ease of implementation of the process, the low cost of the technique, uniform doping show that the methodology applied is very promising as an alternative to the doping methods for this works.

1.3 Objectives

This thesis focusses on the method of spin on dopant by diffusion which is controlled by a few parameters such as diffusion time and temperature. Therefore, the objectives of this study are:

i) To investigate the effect of thermal diffusion temperature and time on boron spin on dopant into p-type SOI wafer by measuring the sheet resistance of boron doped p-type SOI wafer using four-point probe.

ii) To measure electron mobility and carrier density of boron doped p-type SOI wafer using Hall Effect measurement.

iii) To analyse the surface roughness of boron doped p-type SOI wafer using Atomic Force Microscopy.

1.4 Thesis Outline

This thesis is organized into five chapters and each of the chapter was written to be largely self-contained and complete. Chapter one discusses an overall introduction about the research background, problem statement, and objectives of the study. Chapter two is on the literature review of doping techniques of semiconductor. This chapter encompassed of several technique of doping, types of dopants, type of semiconductor that had been produce. Chapter three illustrates materials, instrumentation and methods of the research, which consists of two main sections. First section explains the details of boron spin on dopant technique on SOI wafer which presents step by step procedure for all work in this research. Other than that, the detail of characterization technique of research's samples were described. Chapter four presents the results and discussion on the influential parameters related to the study. This chapter also will interpret the characterized data from some interesting point of views. Finally, chapter five is the conclusions which briefly describe the summary for the entire work regarding to the research. Some suggestions for continuation work were also included.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

Semiconductor devices plays an important role in our life. A semiconductor is a substance that is between conductors and insulators for electrical conductivity. In microelectronic fabrication, semiconductors devices depend on added impurities into intrinsic (pure) materials such as silicon on insulator wafer to change their electrical, physical, and optical properties. This process is known as “doping”. Doping of semiconductors requires specialty machines, personal, and facilities. In traditional semiconductor device fabrication, the doping is done using ion implantation, thermal diffusion, chemical vapor deposition, or speciality doping furnaces has been stated by (Chiara et al.,2020). Therefore, the performance of devices depends on the functionality of semiconductors which relies strongly on the impurities that can be added to the intrinsic materials to change their electrical, physical, and optical properties.

2.2 Doping

Doping is a process of intentionally introducing impurities into pure semiconductor in order to improve its electrical properties. Therefore, semiconductor properties such as conductivity and carrier density can be adjusted to make them useful for electronic application which may easily modified by introduced impurities into their crystal lattice. An extrinsic semiconductor is one in which impurities contribute a significant fraction of the conduction band electrons and/or valence band holes. In many cases, impurities are added using well-defined doping techniques to improve the material conduction properties. Impurities can be either donors or acceptors. By

contributing an electron to the conduction band, a donor impurity can be easily ionised in the crystal medium.

This process usually done to the intrinsic semiconductor which mean there are no impurity added in it that make it behave like an insulator at low temperature. Therefore, rather than being affected by impurities, the electrical properties of the material itself control the number of holes and electrons. Hence, the free electron will flow toward the positive terminal while the hole will move toward the negative terminal if the voltage is connected across the semiconductor. Therefore, in intrinsic semiconductors, n = p which mean the ratio of excited electrons to holes would be the same. They are also referred to as undoped semiconductors which has low conductivity.

In order to increase the conductivity of intrinsic semiconductor, the number of holes and electron should be increased by adding impurity into the pure semiconductor. This process is achieved by introduce atoms of element into the host lattice of the semiconductor (Ristein, 2006). Thus, the type of semiconductor that had undergo doping process is called extrinsic semiconductor. It also helps the formation of p-n/n-p junction which make the electronic devices work (Blase X and co-worker ,2009). Uniform doping to achieve ultra-shallow junctions at transistor-like device source and drain has been a critical component of the device scaling effort. To conclude, by adding the impurities in the semiconductor material, the intrinsic semiconductor become extrinsic semiconductor which has better electrical properties.

2.2.1 Dopant Activation by Creating P-N Junction

The p-n junction is important in modern electrical applications and in understanding semiconductor devices. It is the most basic type of homojunction,

consisting of p-type and n-type impurities doped into a single crystal intrinsic semiconductor. The electrons and holes in the junction show interesting behaviour. An inherent material, such as a SOI wafer, is doped by an addition of dopant atoms to generate a p-n junction. Small quantities of impurities known as dopants regulate the conducting characteristics. By substituting one of the silicon atoms in the bonding configuration, dopant atoms modify the conduction of the silicon. There are two types of impurities that can be used to change the conductive properties of a semiconductor; donors or acceptors.

2.2.2 Type of dopants

Depending on the type of the impurity atom, doped of extrinsic semiconductors can be either p or n type. Dopants are divided into two types: n-type ("n" for negative) and p-type ("p" for positive). The dopants either release excess of electrons to the semiconductor as free negative charge carriers (n-type doping) or they take extra electrons for chemical bonding (p-type doping) (Ristein, 2006).

2.2.2 (a) P-type

Trivalent impurity from the III group of elements is added as the impurity in a p-type semiconductor. Trivalent impurities like Boron, Aluminium, Indium and Gallium are added to the intrinsic semiconductor and then provides extra holes known as the acceptor atom. Therefore, majority carriers in a p-type semiconductor are holes.

When a group IV semiconductor(silicon) is doped with a p-type trivalent group III dopant (such as boron, B), the dopant works as an electron acceptor because it has one less valence electron than the semiconductor. An empty state called "hole" is generated when a few atoms of trivalent dopant replace silicon atoms in the lattice as shown in Fig. 2.1. Therefore, it can operate as an electron carrier through the structure,

resulting in a p-type semiconductor. A deficiency of electrons and positive holes characterises p-type semiconductors, which has the same effect as a positive charge. These positive holes receive electrons, allowing the semiconductor to conduct current more efficiently.

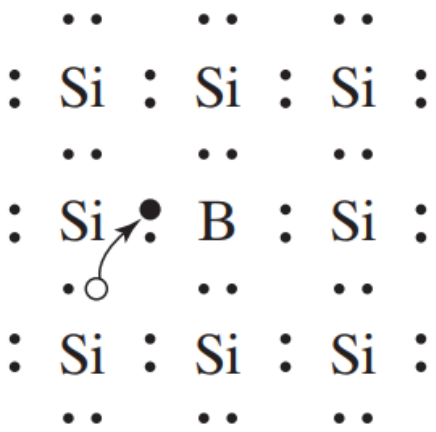

Figure 2.1 Doping of a semiconductor is illustrated with the bond model which B is an acceptor (Chenming, 2009)

Semiconductors doped with acceptors have many holes and few mobile electrons, and are called P type because holes carry positive charge. Most theories treat this "hole" as a positively charged particle because electrons are negatively charged. This positively charged molecule generated between the boron and silicon atoms is now repeated throughout the substrate material, yielding an overall positively doped material or p-type.

2.2.2 (b) N-type

In an n-type semiconductor, pentavalent impurity from the V group is added to the pure semiconductor such as Arsenic, phosphorus, Antimony, Bismuth. The pentavalent impurities provide extra electrons and acts as donor atoms. Therefore, majority charge carriers in n-type semiconductors are electrons**.** When a group IV

semiconductor (silicon) is doped with a n-type pentavalent group V dopant (such as arsenic) which has one more valence electron than the semiconductor, the dopant acts as an electron donor. When this occurs, a dopant atom replaces a silicon atom in the lattice, adding an extra valence electron to the structure as shown in Fig 2.2. Therefore, it has an excess of electrons due to its fifth valence electron. An n-type semiconductor is created when a few of the dopant atoms replace silicon atoms in the lattice. Thus, the n-type semiconductor may conduct current more effectively than the pure semiconductor.

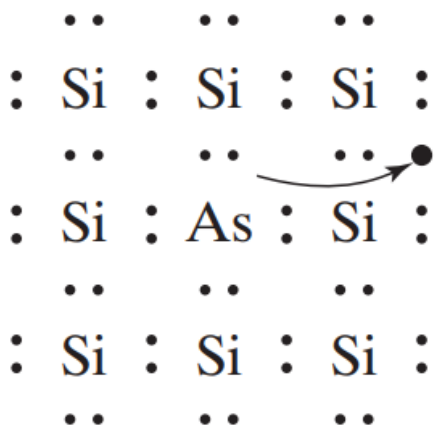

Figure 2.2:Doping of a semiconductor is illustrated with the bond model which As is an acceptor. (Chenming, 2009)

The impurity centres become positively charged, allowing these electrons to engage in transport activities. While for acceptor impurity, it absorbs one electron from the crystal, causing the impurity centre to become negatively charged and a hole to emerge in the valence band. Furthermore, at sufficiently low temperatures, the intrinsic carrier concentration is smaller than the impurity concentration, which begins to control the majority of electronic properties of doped semiconductors.

2.2.3 Diffusion

Diffusion in a semiconductor is defined as a series of atomic motions in the crystal lattice of the dopant. Atomic diffusion is the movement of atoms in semiconductors, including host, dopant, and impurities. The movement of atoms in vacancies and interstitial regions of the crystal lattice is called as diffusion in solids. In the same reason as surface diffusion vibrates around its equilibrium site, lattice atoms vibrate around their equilibrium site.

The two main atomic diffusion mechanisms are represented in Fig. 2.3. The host atoms occupying the equilibrium lattice sites are represented by the open circles. Impurity atoms are expressed by solid dots. The lattice atoms vibrate about the equilibrium lattice positions at high temperatures. A host atom has a finite chance of acquiring enough energy to leave the lattice site and become an interstitial atom, resulting in a vacancy. The mechanism of vacancy diffusion occurs when a nearby impurity moves to the vacancy area, as shown in Fig. 2.3a. While Fig. 2.3b show interstitial diffusion which occurs when an interstitial atom moves from one location to another without occupies a lattice site.

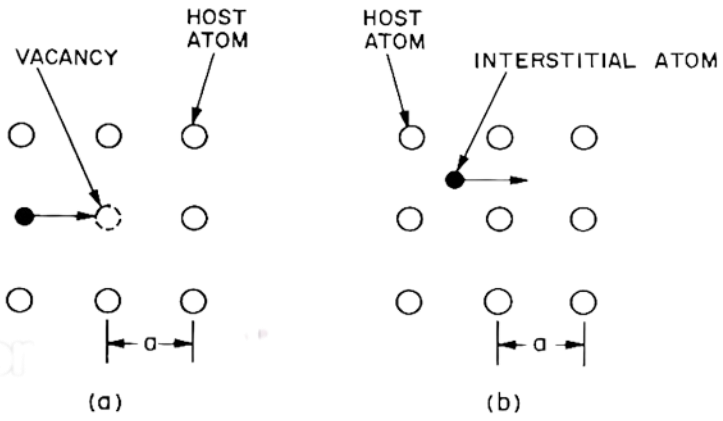

Figure 2.3: Models of diffusion with lattice constant a) vacancies b) interstitial (Tuck,1974)

2.2.3 (a) Fick's Law for diffusion process

The number of impurities that can be incorporated in Si depends on the solid solubility. This depends on the impurity atom and temperature, given by Fig. 2.4. To calculate the concentration of the impurities as a function of depth from the wafer surface, Fick's laws of diffusion can be used. Fick's first law is written in equation 2.1:

$$J = -D \frac{\partial c\,(x,t)}{\partial x} \quad \text{.....(Equation 2.1)}$$

where J is the flux of impurity atoms, which is a constant with respect to time (steady state diffusion) and c(x, t) is the concentration of dopant atom at depth x and time t and D is the diffusion coefficient of dopant atom. Because semiconductors include impurities (dopant atoms), diffusion and hence diffusity are highly influenced by the impurity concentration of the substrate. Dopant atoms diffuse from a high-concentration region to a low-concentration region, and the flow is proportional to the concentration gradient. The negative sign on Equation 2.1 right-hand side indicates that energy moves in the direction of decreasing dopant concentration, implying that the concentration gradient is negative.

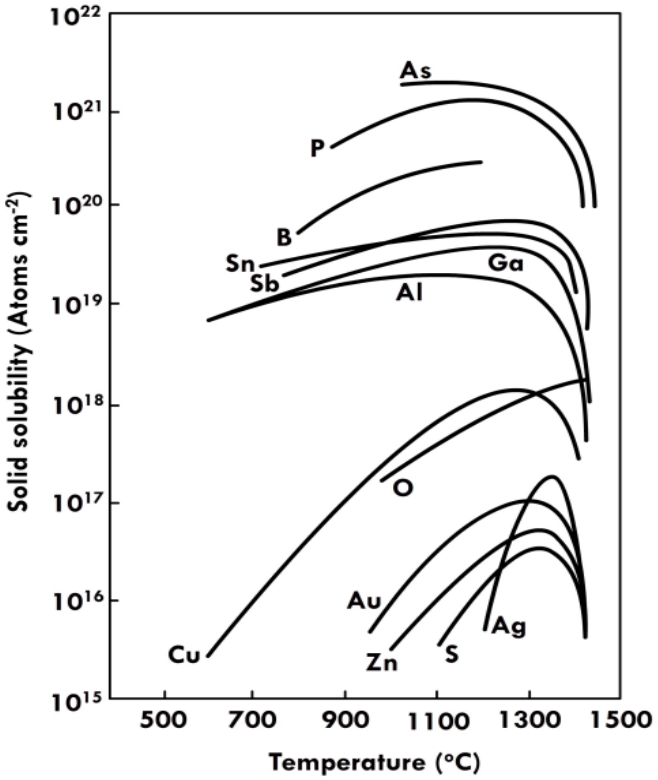

Figure 2.4: Solid solubility of various impurities in Si as a function of temperature. (Peter vant zant,)

2.2.3 (b) Thermal diffusion process step

The process by which a species moves as a result of the existence of a chemical gradient is known as diffusion. The development of p-n junctions and device fabrication is based on the diffusion of controlled impurities or dopants into Si. The process of activating dopant atoms is referred to as thermal diffusion. The semiconductor receives energy in the form of heat. This energy must be high enough for the dopant atoms to replace the silicon atoms and form bonds with their neighbours. The temperature of the thermal diffusion process is a major factor in determine how much dopants are activated. In general, as the temperature rises, the amount of activation also increases.

The silicon wafer is placed in an environment containing the impurity or dopant to include it in SOI doping through diffusion. After the spin on dopant process, the technique of activating dopant atoms is a thermal diffusion process, which helps the dopant materials introduced into the exposed top surface of the wafer through hole in the top of wafer layer. Thermal diffusion is a process, similar to the steps in oxidation process by consuming the underlying Si which are thermal diffusion and drive-in. This method is used to add dopant atoms to the wafer surface. The dopant atoms are introduced from the gas phase into the diffusion process using doped oxide sources, as shown in Fig. 2.5.

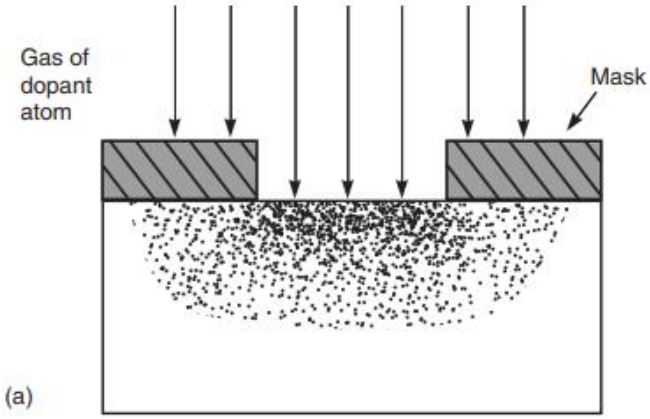

Figure 2.5: Distribution of dopant in wafer by diffusion.

Diffusion of dopant into the substrate is promoted by heating the wafers for the time needed to achieve the desired doping profile. Dopants diffuse into the wafer at a maximum concentration at the surface. As demonstrated in Fig. 2.6, the doping concentration decreases monotonically from the surface, and the in-depth distribution of the dopant is mostly influenced by temperature and diffusion time. In silicon, boron is the most frequent p-type impurity. In the diffusion temperature range (between 800°C

and 1200°C), these elements are very soluble in silicon, with solubilities over 5×10^{20} atoms / cm^3.

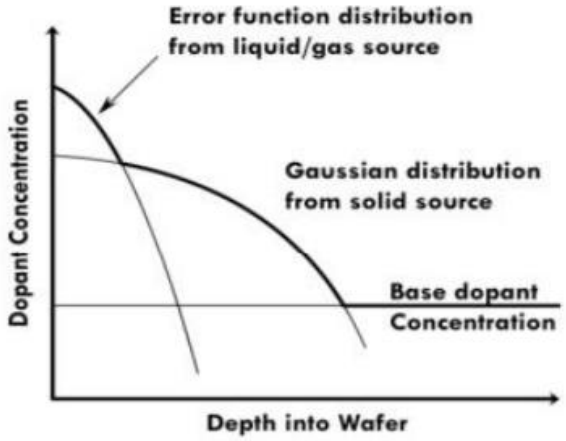

Figure 2.6: Dopant atom profile after thermal diffusion

In, there are two process that involve in this doping process to diffuse the dopant which are thermal diffusion and drive-in.

- ***Thermal diffusion***

To generate a strongly doped oxide layer on the surface of silicon, thermal oxidation of silicon in an ambient containing dopant atom is first conducted. This procedure is called the thermal diffusion process (Makoto Miyoshi et al., 2005). The silicon wafer is heated to a precise and regulated temperature during thermal diffusion, and an excess of the necessary dopant is kept above the wafer. The dopants diffuse into the crystal until their concentration near the surface equals that of the surrounding ambient above it.

- ***Drive-in***

The dopant atoms need to be redistributed into the bulk once they have reached the wafer surface which called as drive-in method. Additionally, the carrier gas may react with the wafer surface simultaneously, especially if there is a reactive gas present, such as dry oxygen or water vapour. These might lead to dopant diffusion and Si oxidation. While in certain cases this would be advantageous, it would also have an impact on the distribution of dopants because the presence of an oxide layer can increase n-type dopants and reduce p-type dopants just below the interface.

2.2.3 (c) Thermal diffusion source

There are different sources for the dopant atoms. These can be solid, liquid, or gaseous sources. Some examples of dopant materials for SOI are antimony, arsenic, phosphorus and boron were shown in Table 2.1 which the compound and its stated are included. The form of the concentration profile inside the wafer is determined by the usage of dopants in various states.

Table 2.1: Dopant materials with comping and state.

Type	**Element**	**Compound**	**Formula**	**State**
n-type	Antimony	Antimony Trioxide	Sb_2O_3	Solid
		Arsenic Trioxide	As_2O_3	Solid
	Arsenic	Arsine	AsH_3	Gas
		Phosphorous oxychloride	$POCl_3$	Liquid
			P_2O_5	Solid
	Phosphorus	Phosphorous Pentoxide	PH_3	Gas
		Phosphine		

p-type	Boron	Boron Tribromide	BBr_3	Liquid
		Boron Trioxide	B_2O_3	Solid
		Diborane	B_2H_6	Gas
		Boron Trichloride	BCl_3	Gas
		Boron Nitride	BN	Solid

2.2.3 (d) Constant surface concentration

Impurities are always concentrated at the surface of liquid and gaseous sources. The constant concentration is maintained by a vapour of impurity atoms (this is also true for solid sources with remote evaporation). Additionally, the wafer thickness is substantially larger than the diffusion length to simulate the wafer as a semi-infinite solid. Fig 2.7 shows concentration profiles for constant surface concentration with increasing time. The maximum concentration is at the surface. With increasing time, the junction depth goes deeper within the wafer. The junction depth is defined as when the dopant concentration becomes equal to the wafer bulk doping level.

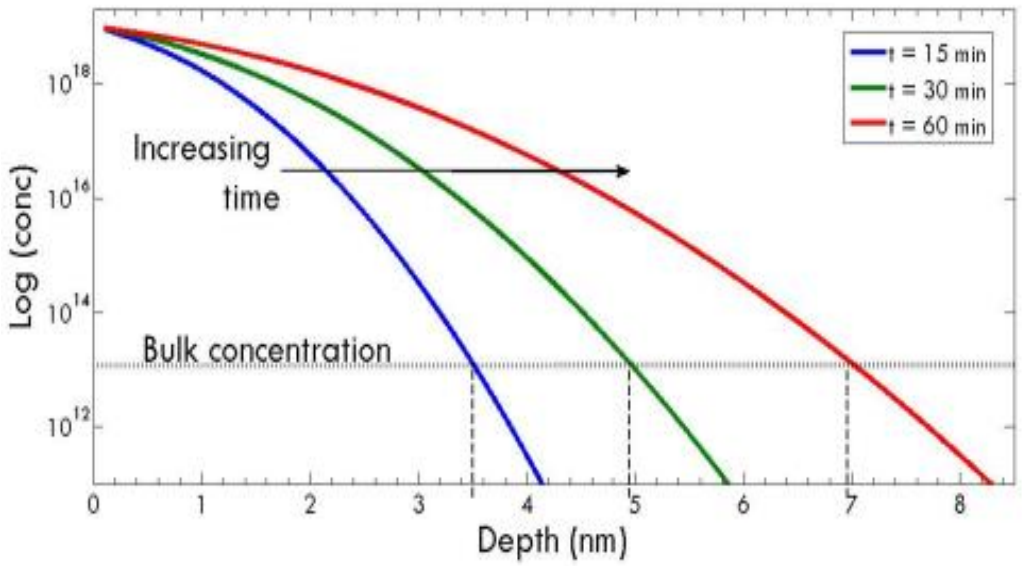

Figure 2.7 Concentration profiles for constant surface concentration with increasing time.

In this case, the impurity concentration, $C(x,t)$, is given by,

$$C(x,t) = C_s \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \quad \text{.....equation 2.1}$$

where C_s is the surface concentration and erfc is the complementary error function. Consider an example of diffusion under a constant surface concentration of $10^{19} cm^{-3}$ and a bulk dopant concentration of $10^{13} cm^{-3}$. The wafer temperature is 1000 K, and the diffusion coefficient at this temperature is $2.9 \times 10^{-22} m^2 s^{-1}$. The error function solution, for this system, is plotted in figure 11, for three different times, 15, 30, and 60 minutes. Equation 4 can also be used to calculate the junction depth for a pn diode. If the base wafer is p type with concentration C_P, the junction depth (where electron and hole concentration is the same) by n type impurity diffusion is given by

$$\frac{C_p}{C_s} = \operatorname{erfc}\left(\frac{x_{pn}}{2\sqrt{Dt}}\right) \quad \text{.....equation 2.1}$$

2.2.4 Ion Implantation

Ion implantation is a more flexible process than diffusion for introducing impurities (dopants) to semiconductors at low temperatures. The act of implanting does not depend on a chemical reaction between the dopant and the wafer material because ion implantation is a physical operation. Over 30 years ago, ion implantation was used for the first time to introduce precisely controlled concentrations of n- and p-type dopants into semiconductors (Williams, 1998). Prior to being directed at a target, which is typically a silicon substrate, dopant atoms are first accelerated, ionised, volatilized, and separated based on their mass-to-charge ratios. The atoms enter the crystal lattice, engage in chemical reactions with the host atoms, lose energy in the process, and come

to rest at a specific depth inside the solid wafer as shown in the Fig 2.8. The average penetration depth is influenced by the dopant, substrate components, and acceleration energy.

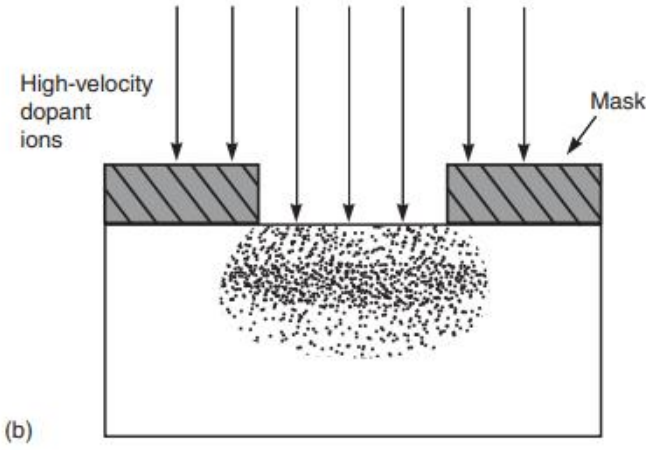

Figure 2.8: Distribution of dopant in wafer by ion implantation.(Vant Zant,

The limitations of diffusion are overcome by ion implantation, which also provides further advantages. Minimal side diffusion occurs during the ion implant procedure, which is carried out at a temperature that is nearly equal to that of room temperature. Below the wafer surface, dopant atoms are positioned, and a variety of concentrations of doping are possible. Ion implantation allows for more control over the number and position of dopants deposited into the wafer. Therefore, the most doping methods for advanced circuits was done by ion implantation.

2.2 Silicon on Insulator (SOI) Wafer

Silicon on insulator (SOI) wafers is a thin circular piece of semiconductor material, such as silicon crystal, that have been used widely in microelectronics and MEMS as a platform for fabrication. SOI wafers are primary substrate materials in the

microelectronic and microelectromechanical area because of its superior properties. In the standard silicon technology, the bulk substrate is associated with undesirable effects such as high leakage currents, parasitic bipolar components, defects and interference between separate active devices or circuits built on the same integrated chip (Alles,1997).

However, an interesting modification of the standard silicon wafer is the silicon-on-insulator (SOI) substrate. It is because SOI technology produces semiconductor devices using an insulating substrate rather than in a semiconductor bulk (Huang, 2011). As seen in Fig. 2.9, SOI wafers have sandwich structures with a top single crystal silicon layer either directly supported by an insulating substrate (such as SiO_2) or separated from the bulk substrate by an insulating layer (such as SiO_2).Similarly, Bernstein and Rohrer found the fundamental difference between the SOI structure and its bulk counterpart is the insertion of the insulation layer beneath the electronics (Bernstein and Rohrer, 2000). Because of their benefits over silicon bulk substrates, technologies based on the use of a buried oxide layer, SiO_2, as an insulator in SOI wafers have been widely developed in microelectronics.

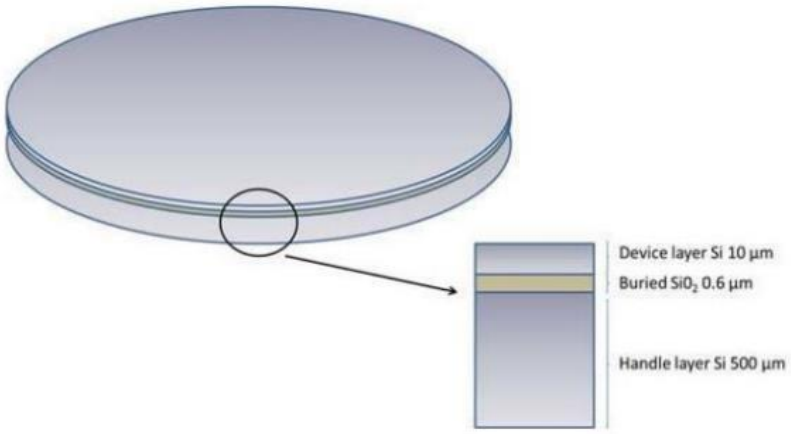

Figure 2.9: Schematic of the Silicon on Insulator (SOI) wafer. (Seyit,2014)

In a range of applications, it has recently been proved that SOI has significantly superior performance and attracts greater attention (Arnold,1994). The lack of latch-up, lower parasitic source and drain capacitances, and the ease with which shallow connections may be made are just three of the obvious benefits of SOI technology over bulk (Huang, 2011). Smart power devices and power integrated circuits, which combine monolithically power devices with control circuitry, are the most common uses. These integrated circuits reduce system volume and weight while increasing system reliability and efficiency. Several factors influence the unique features of SOI structures, including the wide range of Si or BOX layer thicknesses, various Si–SiO_2 contacts, specific film defects, and stress effects.

Furthermore, capacitance across the buried oxide between the junction and the handle wafer must be considered in SOI. As a result of the vertical connections made feasible by SOI, parasitic capacitances, leakage current, and short-channel ejects are significantly reduced, boosting the speed of SOI-based devices.

Moreover, the inverse subthreshold slope for totally depleted SOI devices can be steeper, allowing for lower threshold voltages and reduced leakage current than in bulk devices. As a result, SOI-based devices can function at lower voltages without sacrificing speed. Because lower voltage operation reduces overall device power consumption, SOI technology is recommended in the consumer electronics sector, particularly for mobile wireless applications and other hand-held devices (Andreas and Gertrud, 2000).

CHAPTER 3
METHODOLOGY

3.1 Introduction

This chapter provides the description and procedures for chemicals, instruments, and characterization tools used in the research. This research was started by sample preparation and sample cleaning of SOI wafer. The process of cleaning SOI wafer used standard solution (SC) which is SC-1 and SC-2. The chemical that used in this research are Hydrogen Peroxide, Ammonium Hydroxide, Hydrochloric Acid, Hydrofluoric Acid and B155 Spin on dopant. Therefore, in this chapter has provide the detail of chemical use for this research.

There are the main methods which are SOD and thermal diffusion were explained in this chapter. The SOD was undergo to create dopant layer on SOI wafer while the thermal diffusion was help to diffuse the dopant solution into the surface of SOI wafer. The diffusion process was undergo with different temperature and diffusion time to achieve the purpose of this research.

Furthermore, there were many types of characterization technique that has been describe in this chapter. The characterization technique has proceeded are X-Ray diffraction (XRD), scanning electron microscope (SEM), atomic force microscopy (AFM), four-point probe and Hall Effect. The purpose of these characterization and measurement were described in this chapter.

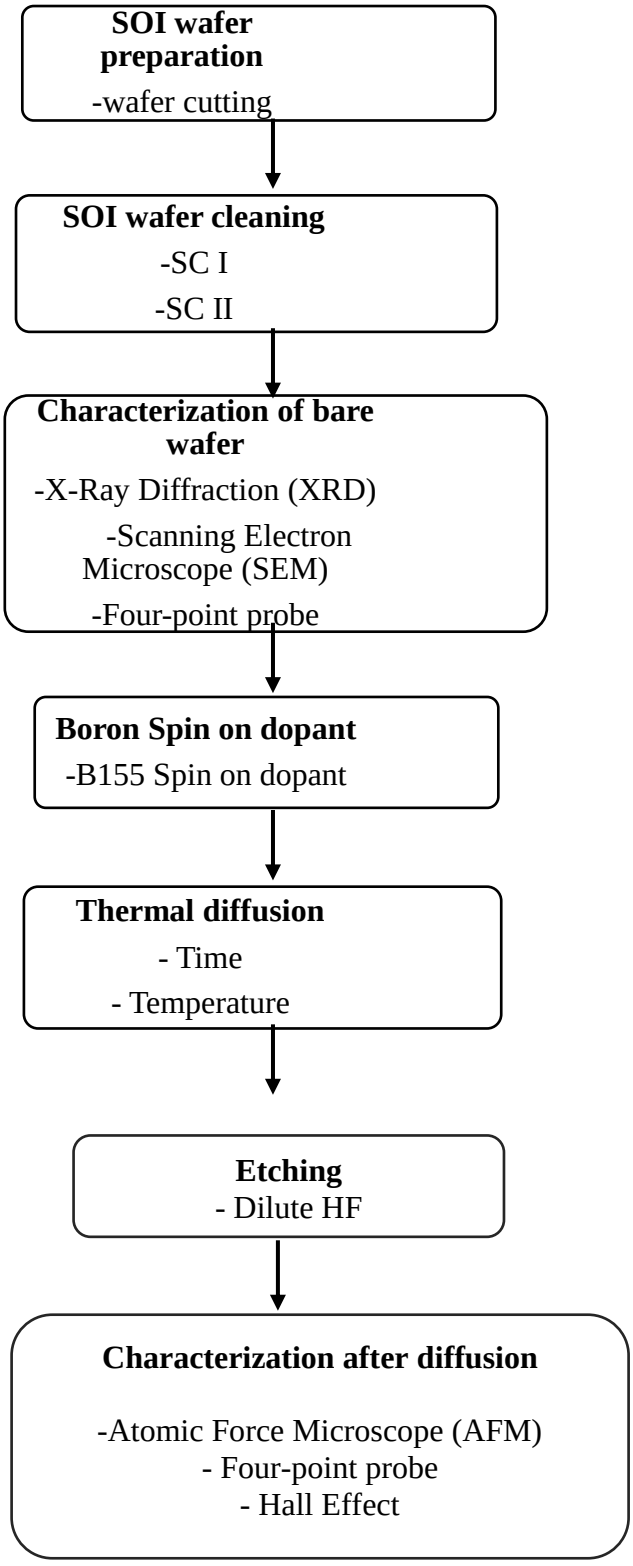

Figure 3.1: Flow chart of summarize methodology

3.2 Material and chemical

3.2.1 Silicon on Insulator (SOI) wafer

SOI is a semiconductor structure consisting of a layer of single crystalline silicon separated from the bulk substrate by a thin layer of insulator. In SOI wafers the insulator is almost invariably a thermal silicon oxide (SiO_2) layer, and the substrate is a silicon wafer. Fig 3.2 show SOI wafer that used in this study is p-type doped with boron with (100) orientations which made in Japan. This SOI wafer has thickness of 725µm with bulk resistivity of 1-20 Ω·cm. The layer thickness of Si is 70 nm while thickness of buried oxide (BOX) layer of SiO_2 was approximately 200 nm with a uniformity of ±5 nm. The illustration of the layer thickness of SOI thickness was shown in Fig. 3.3.

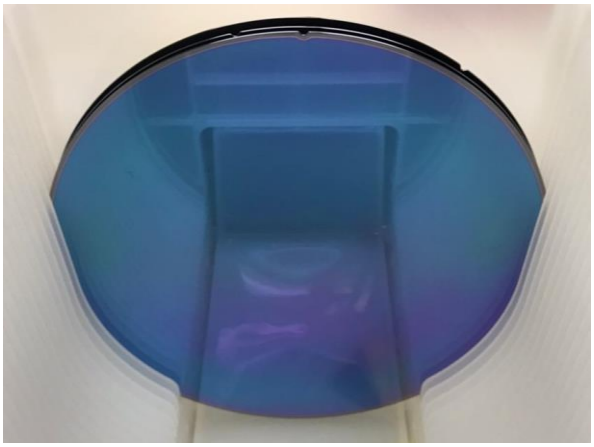

Figure 3.2: The 3-inch silicon on insulator (SOI) wafer.

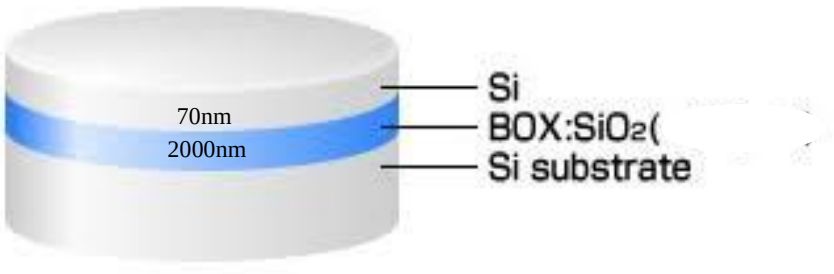

Figure 3.3: Illustration of layer thickness of SOI wafer.