UNIVERSITI SAINS MALAYSIA

First Semester Examination
Academic Session 1998/99

August/September 1998

CSI501 - Computer Organisation

Duration : [3 hours]

INSTRUCTION TO CANDIDATE:

- Please ensure that this examination paper contains SIX questions in FIVE printed pages before you start the examination.
- Answer Questions 1, 2 and 3 and choose **any two** questions from Questions 4, 5 and 6.
- You can choose to answer either in Bahasa Malaysia or English.

ENGLISH VERSION OF THE QUESTION PAPER

1. (a) Convert the hexadecimal number 425.24 to its equivalent in:

(i) Decimal

(ii) Octal

(iii) Binary

(iv) a number to the base 4

(4 marks)

(b) What is a gray code? Give a set of 4 bit gray code to represent the decimal digits.

(3 marks

(c) A 16 bit floating point register uses a sign bit and a six bit exponent and a nine bit mantissa. If the exponent is stored in sign-magnitude form and the mantissa is a normalised fraction,

(i) What is the decimal equivalent of the contents of the register when it is storing the binary number 1100011110000000?

(4 marks)

(ii) Find the range of positive numbers that can be stored in the register.

(6 marks)

(d) Construct the truth table of the following Boolean function without expanding or simplifying the function:

(x+y').(x'+y)

(3 marks)

2. (a) Convert the following Boolean function to product of sum form:

x+x'y + x'z'

(4 marks

(b) Find the complement of the function wx'+y'z'+w'yz' and express it in the sum of products form.

(6 marks

(b) Show that the AND, OR and NOT operations of Boolean Algebra can be realized with NAND gates only.

(4 ma

(d) Simplify the following Boolean function using Karnaugh Map:

wx'+y'z'+w'yz'

Assume that wxyz', w'xyz and w'xy'z are don't cares.

(6 marks

3. (a) What are the three essential registers for a DMA controller?

(3 marks)

(b) Why is a DMA controller sometimes referred to as cycle stealing?

(2 marks)

(c) What is a vectored interrupt? What is an alternative to a vectored interrupt?

(4 marks)

(d) Draw a daisy chain of three I/O devices connected to a CPU.

(4 marks)

(e) Given the control sequence of **only** Add and Branch instructions, write a logic function and draw a logic circuit to generate the control signal PC_{IN}.

(7 marks)

Add Instruction:

1. PC_{OUT} , MAR_{IN} , Read, Clear Y, Set carry-in to ALU, Add, Z_{IN}
2. Z_{OUT} , PC_{IN} , Wait for MFC
3. MDR_{OUT}, IR_{IN}
4. Address-field-of-IR_{OUT} , MAR_{IN}, Read
5. $R1_{OUT}$, Y_{IN} , Wait for MFC
6. MDR_{OUT}, Add, Z_{IN}
7. Z_{OUT} , $R1_{IN}$, End.

Branch Instruction

1. PC_{OUT} , MAR_{IN} , Read, Clear Y, Set carry-in to ALU, Add, Z_{IN}
2. Z_{OUT} , PC_{IN} , Wait for MFC
3. MDR_{OUT}, IR_{IN}
4. PC_{OUT} , Y_{IN}
5. Address-field-of-IR_{OUT} , Add, Z_{IN}
6. Z_{OUT} , PC_{IN} , End.

4. (a) Design a combinational circuit that detects an error in the representation of a decimal digit in 8-4-2-1 code. The output of the circuit must be logic-1 when the inputs contain any one of the six unused bit combinations in the 8-4-2-1 code.

(6 marks)

(b) Design a sequential circuit with two T flip-flops, A and B, which goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats.

(6 marks)

(c) Show as to how a J-K flip-flop can be converted into a (i) T flip-flop and (ii) D flip-flop.

(2 marks)

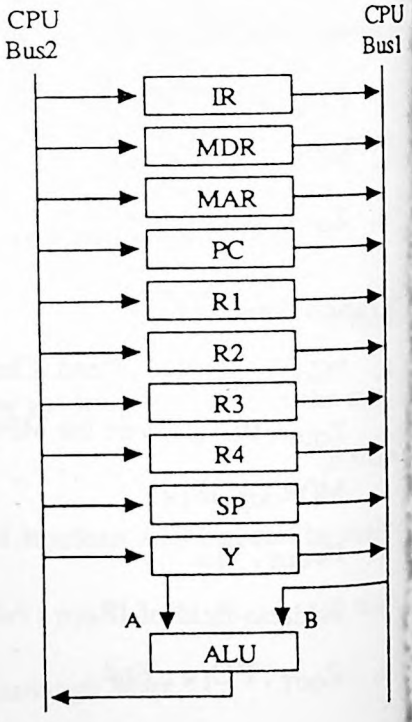
(d) Explain with the help of suitable examples the execution of fetch and execute cycles in a computer.

(6 marks)

5. Given below is a control sequence to fetch/execute a two-word instruction on the two bus CPU shown. Note that three paths to/from the ALU are always connected.

opcode	R3	R4
200		

1. PC_{OUT}, F=B, MAR_{IN}, Y_{IN}, Read
2. F = A+1, PC_{IN}, Wait for MFC
3. MDR_{OUT}, F=B, IR_{IN}
4. PC_{OUT}, F=B, MAR_{IN}, Y_{IN}, Read
5. F = A+1, PC_{IN}, Wait for MFC
6. MDR_{OUT}, F=B, $R1_{IN}$
7. $R1_{OUT}$, F=B, Y_{IN}
8. $R3_{OUT}$, F=A+B, MAR_{IN}, Read
9. $R4_{OUT}$, F=B, Y_{IN}, Wait for MFC
10. MDR_{OUT}, F=A-B, $R4_{IN}$, End



(a) What is the content of R1 after step 6?

(4 marks)

(b) What is the content of MAR after step 8? Use [ ] to indicate the "content of", if necessary?

(4 marks)

(c) In the first word of the given instruction, is R3 a source operand or a destination operand?

(2 marks)

(d) Describe the given instruction as a single equation. Use [ ] to indicate the "content of", if necessary.

(4 marks)

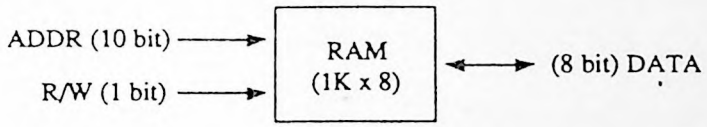
(e) Explain the differences between SRAM and DRAM. Would using BCs (Binary Cell) as a building block result in a SRAM or DRAM module? Are these memory models synchronous or asynchronous? Explain.

(6 marks)

6. (a) Explain the differences between real (physical) and virtual memory.

(4 marks)

(b)



Use the RAM module above and additional hardware to design a (8 Kbit x 8) = (8 Kbyte) memory module.

(4 marks)

(c) Modify the design in (b) so as to implement a 4K word module, in which 1 word = 8 bytes.

(4 marks)

(d) A computer uses a 200Mhz processor and 50ns RAM. How many CPU-cycles does the processor has to wait for memory function complete (MFC) signal after issuing a memory write operation.

(4 marks)

(e) The bipolar memories are faster than the MOS memories. True or false?

(2 marks)

(f) All dynamic memories are MOS memories. True or false?

(2 marks)

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