DESIGN OF LOW-NOISE AMPLIFIER UTILISING ACTIVE SHUNT FEEDBACK FOR MEDRADIO BAND APPLICATIONS

MUTANIZAM ABDUL MUBIN

UNIVERSITI SAINS MALAYSIA

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by

MUTANIZAM ABDUL MUBIN

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LIST OF ABBREVIATIONS

AC	Alternating current
CEDEC	Collaborative Microelectronic Design Excellence Centre
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-analogue converter
DC	Direct current
DRC	Design Rule Check
DUT	Device Under Test
FBB	Forward body biasing
FCC	Federal Communications Commission
FOM	Figure of Merit
GND	Ground
IC	Integrated circuit
IIP_3	Input third-order intercept point
IP_{1dB}	Input-referred 1-dB compression point
ISM	Industrial, Scientific and Medical
LNA	Low-noise amplifier
LVS	Layout-Vs-Schematic

MedRadio	Medical Device Radiocommunications Service
MICS	Medical Implant Communication Service
MIM	Metal-Insulator-Metal
MOS	Metal-Oxide-Semiconductor
MOSCAP	MOS transistor utilised as capacitor
NF	Noise figure
nhp	High-power NMOS transistor
NMOS	N-type Metal-Oxide-Semiconductor
P_{1dB}	1-dB compression point
PDK	Process Design Kit
PEX	Parasitic extraction
php	High-power PMOS transistor
PMOS	P-type Metal-Oxide-Semiconductor
PVT	Process, voltage and temperature
RF	Radio-frequency
RL	Return loss
RL_{in}	Input return loss
SRD	Short Range Device
WPAN	Wireless Personal Area Network

LIST OF SYMBOLS

a_b	Gain of basic amplifier
A_{CL}	Closed-loop gain
a_f	Gain of feedback network
A_v	Voltage gain
C	Capacitance
C_1	Capacitor 1
C_2	Capacitor 2
C_3	Capacitor 3
C_4	Capacitor 4
C_5	Capacitor 5
C_6	Capacitor 6
C_{db_M1}	Drain to bulk parasitic capacitance of M_1
C_{db_M2}	Drain to bulk parasitic capacitance of M_2
C_{db_M3}	Drain to bulk parasitic capacitance of M_3
C_{db_M4}	Drain to bulk parasitic capacitance of M_4
C_{db_M6}	Drain to bulk parasitic capacitance of M_6

C_{dg_M6}	Drain to gate parasitic capacitance of M_6
C_f	Feedback capacitance
C_{gd_M1}	Gate to drain parasitic capacitance of M_1
C_{gd_M2}	Gate to drain parasitic capacitance of M_2
C_{gd_M3}	Gate to drain parasitic capacitance of M_3
C_{gd_M4}	Gate to drain parasitic capacitance of M_4
C_{gd_M5}	Gate to drain parasitic capacitance of M_5
C_{gs_M1}	Gate to source parasitic capacitance of M_1
C_{gs_M2}	Gate to source parasitic capacitance of M_2
C_{gs_M3}	Gate to source parasitic capacitance of M_3
C_{gs_M5}	Gate to source parasitic capacitance of M_5
C_{js}	Depletion-region capacitance per unit area
C_{ox}	Gate-oxide capacitance per unit area
C_{P1}	Capacitor P1
C_s	Source capacitor
C_{sb_M5}	Source to bulk parasitic capacitance of M_5
dB	Decibel
dBm	Decibel-milliwatt

F	Noise factor
f_R	Resonant frequency
f_T	Transition frequency
GHz	Gigahertz
g_m	Transconductance
g_{mb_M5}	Body transconductance of M_5
g_{m_M1}	Transconductance of M_1
g_{m_M2}	Transconductance of M_2
g_{m_M3}	Transconductance of M_3
g_{m_M4}	Transconductance of M_4
g_{m_M5}	Transconductance of M_5
g_{m_NMOS1}	Transconductance of NMOS Transistor 1
g_{m_PMOS1}	Transconductance of PMOS Transistor 1
Hz	Hertz
I_{CSCR}	Supply current of main driver
I_D	Drain current
I_{D0}	Drain current when V_{GS} equals V_{TH}
I_{DC}	DC current

i_{in}	Small-signal input current
i_{out}	Small-signal output current
$\overline{i_{n,M1}^2}$	Mean-squared noise current per unit bandwidth for M_1
$\overline{i_{n,M2}^2}$	Mean-squared noise current per unit bandwidth for M_2
$\overline{i_{n,M3}^2}$	Mean-squared noise current per unit bandwidth for M_3
$\overline{i_{n,M4}^2}$	Mean-squared noise current per unit bandwidth for M_4
I_{SASF}	Supply current of feedback network
I_{SOB}	Supply current of output buffer
k	Boltzmann constant
kΩ	Kiloohm
L	Gate length
L	Inductance
LC	Inductor-capacitor
L_g	Gate inductor
L_{M1}	Gate length of M_1
L_{M2}	Gate length of M_2
L_s	Source inductor
M_1	Transistor 1

M_2	Transistor 2
M_3	Transistor 3
M_4	Transistor 4
M_5	Transistor 5
M_6	Transistor 6
M_c	Transistor c
M_{C1}	Transistor C1
M_{C2}	Transistor C2
mA	Milliampere
MHz	Megahertz
mm^2	Millimeter-squared
M_n	Transistor n
M_{N1}	Transistor N1
M_{n1}	Transistor n1
M_{N2}	Transistor N2
M_{nb}	Transistor nb
M_p	Transistor p
M_{P1}	Transistor P1
M_{p1}	Transistor p1

M_{P2}	Transistor P2
M_{pb}	Transistor pb
M_{PF1}	Transistor PF1
M_{PF2}	Transistor PF2
mS	Millisiemen
mV	Millivolt
mW	Milliwatt
n	Ratio of sum of gate-oxide capacitance and depletion-region capacitance over gate-oxide capacitance
nF	Nanofarad
nH	Nanohenry
nm	Nanometer
$NMOS_1$	NMOS Transistor 1
P_{DC}	DC power consumption
pF	Picofarad
$PMOS_1$	PMOS Transistor 1
Q	Quality factor
R	Resistance
R_1	Resistor 1

R_2	Resistor 2
R_3	Resistor 3
R_4	Resistor 4
R_F	Feedback resistor
R_{in}	Input resistance
r_{in}	Small-signal input resistance
R_{in_b}	Input resistance of basic amplifier
R_{L1}	Resistor L1
R_{L2}	Resistor L2
r_o	Small-signal output resistance
r_{o_M1}	Small-signal output resistance of M_1
r_{o_M2}	Small-signal output resistance of M_2
r_{o_M3}	Small-signal output resistance of M_3
r_{o_M4}	Small-signal output resistance of M_4
r_{o_M5}	Small-signal output resistance of M_5
r_{o_M6}	Small-signal output resistance of M_6
r_{o_NMOS1}	Small-signal output resistance of NMOS Transistor 1
r_{o_PMOS1}	Small-signal output resistance of PMOS Transistor 1

R_{out}	Output resistance
R_{out_f}	Output resistance of feedback network
R_{P1}	Resistor P1
R_{P2}	Resistor P2
R_{P3}	Resistor P3
R_{P4}	Resistor P4
R_s	Source resistance
S_{11}	Input reflection coefficient
S_{21}	Forward transmission coefficient
S_i	Input signal
S_o	Output signal
S_f	Feedback signal
S_e	Error signal
T	Temperature
V	Volt
V	Voltage
v_1	Simplified small-signal voltage at gate of M_1 and M_2
V_{bASF}	Gate voltage of M_3

V_{bcsASF}	Gate voltage of M_4
V_{bcsOB}	Gate voltage of M_6
V_{bN}	Gate voltage of M_1
V_{bOB}	Gate voltage of M_5
V_{bP}	Gate voltage of M_2
v_{bs_M5}	Small-signal bulk-source voltage of M_5
V_{CSCR}	Supply voltage of main driver
V_{DS}	Drain-source voltage
V_{DC}	DC voltage
V_{GS}	Gate-source voltage
v_{gs_M3}	Small-signal gate-source voltage of M_3
v_{gs_M5}	Small-signal gate-source voltage of M_5
v_{in}	Small-signal input voltage
v_{in_1}	Small-signal voltage at gate of M_1
v_{in_2}	Small-signal voltage at gate of M_2
$\overline{v_{n,M1}^2}$	Mean-squared noise voltage per unit bandwidth for M_1
$\overline{v_{n,M2}^2}$	Mean-squared noise voltage per unit bandwidth for M_2
$\overline{v_{n,M3}^2}$	Mean-squared noise voltage per unit bandwidth for M_3

$\overline{v_{n,\,M4}^2}$	Mean-squared noise voltage per unit bandwidth for M_4
$\overline{v_{n,\,out}^2}$	Output mean-squared noise voltage per unit bandwidth
$\overline{v_{n,\,Rs}^2}$	Mean-squared noise voltage per unit bandwidth for R_s
v_{out}	Small-signal output voltage
V_{SASF}	Supply voltage of feedback network
V_{SB}	Source-bulk voltage
V_{SOB}	Supply voltage of output buffer
V_{supply}	Supply voltage
V_T	Thermal voltage
V_{TH}	Threshold voltage
V_{TH0}	Threshold voltage with V_{SB} = 0
W	Gate width
W_{M1}	Gate width of M_1
W_{M2}	Gate width of M_2
z_0	Characteristic impedance
z_{in}	Input impedance
γ	Threshold voltage parameter
γ_{M1}	Thermal noise coefficient for M_1

γ_{M2}	Thermal noise coefficient for M_2
γ_{M3}	Thermal noise coefficient for M_3
γ_{M4}	Thermal noise coefficient for M_4
Γ_{in}	Input reflection coefficient
λ	Channel-length modulation coefficient
μ	Average charge carrier mobility
µA	Microampere
µm	Micrometer
ϕ_f	Fermi level
Ω	Ohm
ω	Angular frequency

REKABENTUK PENGUAT HINGAR-RENDAH MENGGUNAKAN SUAP-BALIK PIRAU AKTIF UNTUK APLIKASI-APLIKASI JALUR MEDRADIO

ABSTRAK

Sebuah penguat hingar-rendah (LNA) CMOS 0.18-µm berkuasa rendah untuk aplikasi-aplikasi MedRadio telah direkabentuk dan disahkan di dalam kerja penyelidikan ini. Perisian Cadence IC5 bersama Kit Rekabentuk Proses CMOS C18G dari Silterra telah digunakan untuk semua kerja rekabentuk dan simulasi. LNA ini menggunakan topologi guna-semula-arus punca-sepunya pelengkap dan pincang subambang untuk mencapai operasi kuasa rendah dengan gandaan tinggi dan angka hingar rendah serentak. Sebuah litar suap-balik pirau aktif digunakan sebagai rangkaian padanan masukan untuk memberikan kehilangan kembali masukan yang sesuai. Untuk kegunaan pengujian dan pengukuran, sebuah penimbal keluaran telah direkabentuk dan disepadukan dengan LNA ini. Pendekatan rekabentuk tanpa-induktor LNA ini bersama penggunaan MOSCAP sebagai kapasitor, membantu meminimumkan saiz dadu. Berkenaan simulasi pasca-bentangan dengan jumlah penggunaan kuasa yang disimulasikan sebanyak 0.5 mW, kesemua spesifikasi yang disasarkan telah dicapai walaupun terdapat sedikit-sebanyak penurunan daripada keputusan-keputusan simulasi pra-bentangan. Dari simulasi pra-bentangan ke simulasi pasca-bentangan, gandaan dan kehilangan kembali masukan yang disimulasikan mengurang kepada 16.3 dB dan 10.1 dB, sementara angka hingar yang disimulasikan merosot kepada 4.9 dB. Bagaimanapun, IP_{1dB} dan IIP_3 yang disimulasikan menjadi bertambah baik sedikit kepada -26.7 dBm

dan -18.6 dBm. Pada keseluruhannya, prestasi pasca-bentangan yang disimulasikan untuk LNA yang dicadangkan ini boleh dikatakan setanding dengan beberapa LNA yang terbaik untuk masa kini bagi aplikasi-aplikasi MedRadio. Bagaimanapun, kemerosotan kehilangan kembali masukan dan angka hingar yang disimulasikan pada peringkat pasca-bentangan disebabkan oleh kemuatan dan rintangan berparasit di dalam bentangan litar bersepadu berkenaan harus diberi perhatian yang serius. Ini adalah kerana keputusan-keputusan simulasi pasca-bentangan untuk kedua-dua parameter ini boleh dikatakan tidak mempunyai jidar ke spesifikasi yang disasarkan.

DESIGN OF LOW-NOISE AMPLIFIER UTILISING ACTIVE SHUNT FEEDBACK FOR MEDRADIO BAND APPLICATIONS

ABSTRACT

A low-power 0.18-µm CMOS low-noise amplifier (LNA) for MedRadio applications has been designed and verified in this research work. Cadence IC5 software with Silterra's C18G CMOS Process Design Kit were used for all design and simulation work. This LNA utilises complementary common-source current-reuse topology and subthreshold biasing to achieve low-power operation with simultaneous high gain and low noise figure. An active shunt feedback circuit is used as input matching network to provide a suitable input return loss. For test and measurement purpose, an output buffer was designed and integrated with this LNA. Inductorless design approach of this LNA, together with the use of MOSCAPs as capacitors, help to minimise the die size. On post-layout simulations with simulated total power consumption of 0.5 mW, all targeted specifications are met albeit with some degradations from the pre-layout simulation results. From pre-layout to post-layout simulations, the simulated gain and input return loss are reduced to 16.3 dB and 10.1 dB respectively whilst the simulated noise figure worsens to 4.9 dB. However, the simulated IP_{1dB} and IIP_3 slightly improve to -26.7 dBm and -18.6 dBm respectively. Overall, the post-layout simulated performance of this proposed LNA is fairly comparable to some current state-of-the-art LNAs for MedRadio applications. However, the worsening simulated input return loss and noise figure at post-layout level due to parasitic capacitances and resistances in the integrated circuit layout need to be given

serious attention. This is because the post-layout simulation results of these two parameters virtually have no margin to their respective targeted specifications.

CHAPTER ONE

INTRODUCTION

1.1 Background Information & Research Motivation

As global life-expectancy increases, the number of elderly around the world continues to rise and so is the need for cost-effective medical service. Lately, for the past several years, we have seen some vigorous research and development activities in the field of wireless communications for biomedical purposes, specifically for diagnostic and therapeutic medical devices either in the form of implants or as body-worn devices. These new findings have made some significant contributions in the development of some next generation medical devices such as remote-controlled cardiac pacemakers, neuro-muscular stimulators and drug delivery implants (Bradley 2006; Copani et al. 2011). Figure 1.1 is an illustration of a wireless neuro-muscular sensing and stimulation system with the sensors and stimulators being implanted underneath the patient's skin.

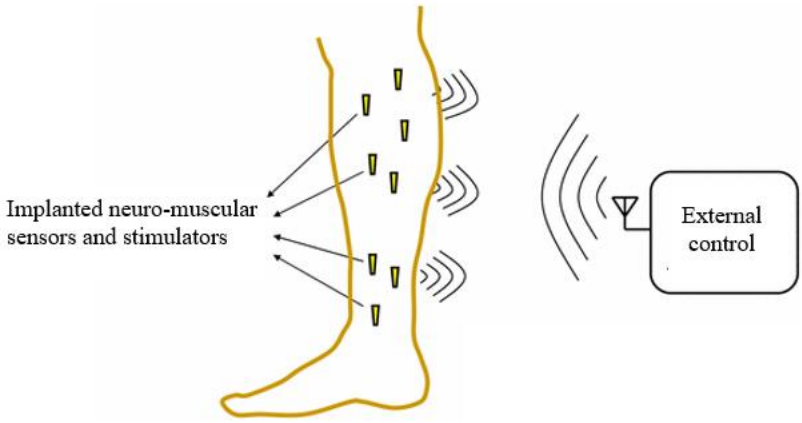

Figure 1.1: An illustration of a wireless neuro-muscular sensing and stimulation system (Liu et al. 2013).

The Medical Device Radiocommunications Service (MedRadio) frequency spectrum is usually the main frequency band option for wireless communications of such biomedical devices. Way back in 1999, the Federal Communications Commission (FCC) of the United States had established the Medical Implant Communication Service (MICS) frequency spectrum between 402 MHz to 405 MHz which was dedicated for medical implant devices. 10 years later, MICS was replaced by MedRadio. This new frequency spectrum extends from 401 MHz up to 406 MHz which means that it is basically the MICS but with a 1-MHz extension at both lower and upper ends of the spectrum (FCC n.d.).

Other frequency band options for wireless communication of biomedical device include the ISM band around 2.4 GHz and the European SRD band between 868 MHz to 928 MHz. The ISM band has the disadvantage of higher transceiver power consumption and greater free-space path loss due to its considerably high frequencies. The disadvantage of the SRD is the fact that it is not globally recognised. In addition, both ISM and SRD are also being utilised by other applications thus making them susceptible to interferences that may compromise the reliability of the wireless communication system of the biomedical device (Cha et al. 2011).

In general, biomedical implants and body-worn medical devices require very low power consumption to prolong battery life, thus reducing the number of times the battery needs to be replaced with a new one (Anis et al. 2010; Bradley 2006; Copani et al. 2011; Cha et al. 2011; Yang et al. 2011; Jeong et al. 2011). This will therefore provide more continuity, reliability and cost-efficiency of the biomedical device. The fact that the wireless communication part of the medical device is usually the one that consumes most power seems to emphasize the need to have low-power components in

the wireless communication portion of the device. These components hence must be operated with low supply voltage and reduced current consumption.

Apart from having low power consumption, these biomedical devices need to have high sensitivity (Copani et al. 2011). This is for the devices to be able to detect very low and weak radio-frequency (RF) signals due to attenuation or loss caused by the human body. Also, because transmission of excessively large RF signals should be avoided as they can be dangerous and detrimental to the human body.

It is also desirable to minimize the size of the device for convenience as they are either to be implanted underneath the skin or to be body-worn by the patient (Jeong et al. 2011). Besides, small size of the integrated circuits and the device as a whole will help in further cost reduction.

One of the most important components in the wireless communication part of biomedical devices is the low-noise amplifier (LNA). Being the first active block of the receiver portion, the function of the LNA is to provide sufficient gain to the input signal received by the antenna whilst at the same time only adding a minimum amount of noise to the signal. The LNA should also be able to handle larger input signals without distortion. On top of that, a specific impedance, which is normally 50 Ω, must be presented at the input of the LNA for maximum power transfer (Lee 2004).

1.2 Problem Statement

Just as for MedRadio biomedical device in general, the MedRadio LNA, which forms part of the receiver portion of the biomedical device, needs to have very low power consumption thus must be operated with low supply voltage and reduced current

consumption. At the same time, this low power requirement should not compromise on the high gain and low noise figure of the LNA. Work by (Pan et al. 2017) exhibits a very high gain of 21 dB and low noise figure of 3 dB in the MedRadio frequency range. However, due to its differential topology with some capacitive cross-couplings, its power consumption is 2 mW which is very high for biomedical applications. Work by (Liu & Zhang 2017) on the other hand, only consumes 0.2 mW of DC power despite also having differential topology with some capacitive cross-couplings. However, in the MedRadio band frequencies, the noise figure is quite high at 5.5 dB due to the low current. It is therefore a great challenge to obtain a suitable balance between low power consumption, high gain and low noise figure for a MedRadio band LNA.

In addition, the die size for this LNA must be minimized for convenience purpose and also for cost reduction. Minimizing the size of this LNA will ultimately contribute in reducing the total size of the receiver part thus the biomedical device as a whole. Some of the works on MedRadio LNAs such as (Srivastava et al. 2016) and (Cha et al. 2011) are utilising inductors in the integrated circuit thus resulting in a considerably large overall size of the LNA. It will therefore be an advantage to come out with inductorless LNA as far as size is concerned.

1.3 Objective

The objective of this work is therefore to design and simulate a low-power CMOS LNA for MedRadio applications. The simulated performance of this LNA is targeted to be comparable with some current state-of-the-art LNAs for MedRadio which are reviewed in Chapter Two. General specifications of this MedRadio LNA are defined in Table 1.1.

Table 1.1: Targeted general specifications of the LNA in this work.

Parameter	**Specification**
Frequency range	401 MHz to 406 MHz
Power consumption	≤ 0.5 mW
Gain	≥ 15 dB
Noise figure	≤ 5 dB
Input return loss	≥ 10 dB
Input-referred 1-dB compression point	≥ -30 dBm
Input third-order intercept point	≥ -20 dBm
Die area	≤ 0.1 mm^2

The specification for power consumption is set to be less or equal to 0.5 mW as a starting point to design a LNA with reasonably very low power consumption. This specification is slightly lower than the average power consumption of all the LNAs for MedRadio applications reviewed in Chapter Two, which is 0.69 mW.

The minimum input power (or the sensitivity) at the receiver of a MedRadio device is approximately -90 dBm (Cruz et al. 2015; Cha et al. 2011; Srivastava et al. 2016). The gain of the LNA therefore, needs to be sufficiently high to amplify this very weak signal prior to the downconversion by the mixer. (Srivastava et al. 2016) suggested a very high gain specification of greater than 35 dB. (Cruz et al. 2015) on the other hand, proposed a much more lenient gain specification of just greater than 10 dB.

In this work, due to the planned inductorless topology and very low power consumption specification of 0.5 mW, it is realistically very difficult to obtain LNA gain of greater than 20 dB and at the same time exhibiting satisfactory performance for other LNA parameters. The gain specification therefore is set to be greater than or equal to 15 dB which is fairly moderate and acceptable.

The specification for noise figure can also be estimated from the sensitivity of MedRadio devices. With a sensitivity of approximately -90 dBm, (Srivastava et al. 2016) calculated an overall noise figure value of about 19 dB for the whole receiver portion and suggested a noise figure specification of less than 6 dB for the LNA since it is the first active component of the receiver chain. In this work however, a more stringent noise figure specification of less than or equal to 5 dB is chosen since the worst noise figure amongst all the LNAs for MedRadio applications reviewed in Chapter Two is just 5.8 dB.

For input return loss, the specification is set to be greater than or equal to 10 dB. This is generally a minimum acceptable level for return loss to limit the amount of reflected signal.

Since MedRadio applications only involve very low and weak RF signals, the linearity of the LNA is not much of a concern. (Srivastava et al. 2016) estimated that the maximum received power at the receiver input of MedRadio devices is approximately -30 dBm. Therefore, for this work, the specification for input-referred 1-dB compression point is set to be greater than or equal to -30 dBm. For input third-order intercept point, the specification is set to be greater than or equal to -20 dBm. This is due to the theory that states that in general, the input third-order intercept point

is greater than the input-referred 1-dB compression point by approximately 10 dB (Razavi 1998).

Lastly, the specification for die area is mainly determined by the 0.18-µm CMOS process technology being utilised in this design work. The smallest die area amongst all the LNAs with 0.18-µm CMOS process technology reviewed in Chapter Two is 0.2 mm^2. The specification therefore is set to be less than or equal to 0.1 mm^2.

1.4 Scope of Research

The LNA is designed in Cadence IC5 as the main design and simulation software with Silterra's 0.18-µm C18G CMOS technology Process Design Kit (PDK). Common-source current-reuse technique has been chosen as the main circuit technique to achieve low-power operation with simultaneous high gain and low noise figure. This is supported by the use of active shunt feedback technique for input matching network to provide a suitable input return loss. In addition, one of the transistors in this LNA circuit is being biased at its subthreshold voltage level thus further lowering the power consumption. The output of this LNA is to be channelled directly into a downconverter mixer, thus no output matching network is required. Fabrication and measurements are planned to be carried out but are not included in this thesis. Due to limitations in measurement facilities at CEDEC, a simpler single-ended topology is chosen for the LNA instead of a differential one.

1.5 Thesis Organization

This thesis consists of five chapters. Chapter One is the introduction where some background information and motivation behind this research are being described. This is followed by problem statement definition and the objective of this research. The scope of this research is also outlined.

Chapter Two discusses the circuit techniques utilised in this LNA design, namely current reuse, active shunt feedback and subthreshold biasing. The next section in this chapter reviews some previous state-of-the-art LNAs that are suitable for MedRadio applications. For each work, circuit description, performance, advantages and disadvantages are discussed.

In Chapter Three, the full design flow of the MedRadio LNA is outlined and all steps in the design flow are described. The first step is to identify the specifications and to decide on the circuit techniques to be employed. Next is to design the main driver section of the LNA. This is followed by the design of a feedback network and its integration with the main driver. The next stage is to design the output buffer and to integrate it with the main driver and feedback network. Pre-layout (or schematic-level) simulations are then carried out on the completed circuit. Once the simulation results are deemed satisfactory, the layout of the circuit is designed. The completed layout is then verified with DRC and LVS. Finally, parasitic extraction and post-layout simulation are performed on the layout.

The results from pre-layout and post-layout simulations in Chapter Three are presented and discussed in Chapter Four. These results are also compared with the targeted specifications and the current state-of-the-art LNAs for MedRadio applications reviewed in Chapter Two.

Finally, Chapter Five concludes this thesis by summarising the whole research work including its achievements and shortcomings. Some suggestions for future work are also proposed.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

Over the years, a number of works on low-power LNAs including those that are suitable to work in MedRadio frequencies have been reported. Various circuit techniques have been employed and demonstrated by these LNAs to achieve low-power operation without compromising too much on gain, noise figure, linearity and size. Most of the time, it is impossible to win everything, thus some trade-offs will have to be made. But in the end, what really matters is getting the right balance amongst all the parameters of the LNA.

This chapter discusses and reviews the three main circuit techniques employed for the design of MedRadio LNA in this research work. These are:

1. Current-reuse technique
2. Active shunt feedback technique
3. Subthreshold biasing technique

Some relevant literatures are used as examples to illustrate these techniques. Also in this chapter, some previous works on LNAs for MedRadio applications are reviewed and discussed. These LNAs include those with wideband capabilities which are not specifically designed for MedRadio frequency band in the first place, but nonetheless may perform rather well in the said frequency range. Each of these LNAs has its own strengths and flaws which can be related back to their topologies and circuit techniques that are being utilised.

2.2 Current-reuse Technique

The main objective of this technique is to obtain a much larger transconductance of the LNA without further increasing the total current drawn. Another way of looking at it is to reduce the total current drawn whilst approximately maintaining the same amount of transconductance of the LNA. Figure 2.1 helps to illustrate this technique.

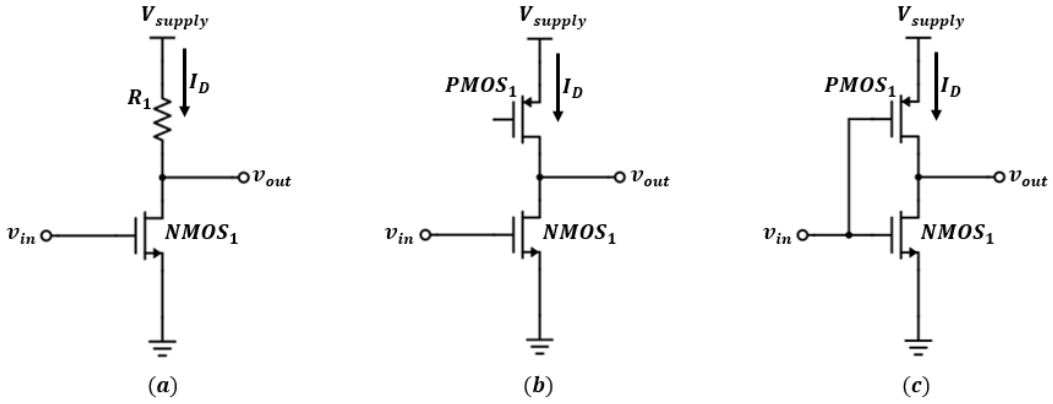

Figure 2.1: Illustration of current-reuse technique. DC-blocking capacitors and biasing for all transistors have been omitted.

Figure 2.1(a) is a typical common-source amplifier that is made up of driving transistor $NMOS_1$ and resistive load R_1 with current I_D passing through the resistor and transistor. The low-frequency small-signal voltage gain of this amplifier is simply given by:

$$A_v = -g_{m\_NMOS1}.(R_1 \parallel r_{o\_NMOS1}) \tag{2.1}$$

In Figure 2.1(b) the resistive load is being replaced with an active load $PMOS_1$. The current I_D passing through this $PMOS_1$ is therefore being reused by $NMOS_1$. With the current passing through both $NMOS_1$ and $PMOS_1$ still being I_D, the low-frequency small-signal voltage gain now is given by:

$$A_v = -g_{m\_NMOS1}.(r_{o\_PMOS1} \parallel r_{o\_NMOS1}) \tag{2.2}$$

When the input signal is also being driven by $PMOS_1$ in addition to $NMOS_1$ as depicted by Figure 2.1(*c*), with the same current I_D passing through both transistors, the low-frequency small-signal voltage gain can now be expressed as:

$$A_v = -\left(g_{m\_PMOS1} + g_{m\_NMOS1}\right).(r_{o\_PMOS1} \parallel r_{o\_NMOS1}) \tag{2.3}$$

Now, the effective transconductance of this amplifier has increased from mere g_{m_NMOS1} to $\left(g_{m\_PMOS1} + g_{m\_NMOS1}\right)$ with the drawn current remaining unchanged. All in all, this shows how the current-reuse technique can help the circuit to be more economical in terms of total current drawn and the effective transconductance it produces. Conversely, the total current drawn can be reduced without reducing the initial effective transconductance.

This current-reuse technique has been implemented through a number of different ways by various authors (Hsu et al. 2009; Khoshroo et al. 2016; Tan et al. 2010; Reddy 2017; Pan et al. 2017; Salimath et al. 2014; Wang et al. 2006; Taris et al. 2008; Karanicolas 1996; Cruz et al. 2015; Cha et al. 2011; Choi et al. 2016; Parvizi et al. 2016; Noh et al. 2010); most commonly by stacking a PMOS transistor on top of a NMOS transistor in the same DC current path as shown previously by Figure 2.1(*c*). With both PMOS and NMOS transistors in the same DC current path, one can opt for either complementary common-source current-reuse or complementary common-gate current-reuse configuration as illustrated in Figures 2.2 and 2.3.

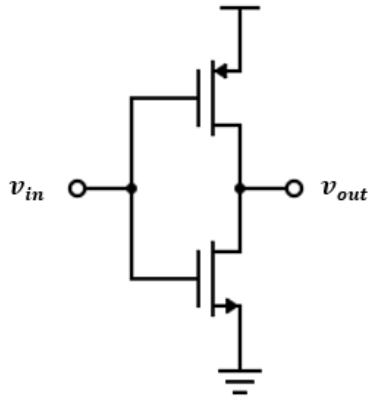

Figure 2.2: Complementary common-source current-reuse configuration.

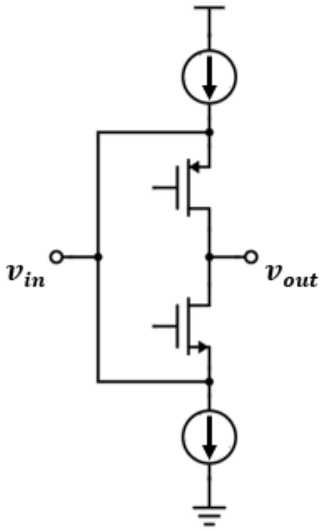

Figure 2.3: Complementary common-gate current-reuse configuration.

For both configurations, the effective transconductance can be almost double to that with only a NMOS transistor and a load in the same DC current path while drawing the same current. It is not going to be exactly doubled since the transconductance of the PMOS transistor is slightly lower than that of the NMOS transistor due to lower mobility of the main charge carrier in the PMOS transistor.

Works from (Hsu et al. 2009; Khoshroo et al. 2016; Noh et al. 2010; Taris et al. 2008; Karanicolas 1996; Cha et al. 2011; Choi et al. 2016) utilise complementary common-source current-reuse configuration for their LNAs. (Cha et al 2011) however, use this configuration in a slightly different way where the NMOS transistor is stacked on top of the PMOS transistor instead of the other way around as described above. This is so that both the NMOS and PMOS portions of the common-source current-reuse LNA can share the same source degeneration inductor. However, with this slightly different configuration, a load (either active or passive) is needed at the drain of each transistor unlike in the usual complementary common-source current-reuse configuration where both the NMOS and PMOS transistors also function as active loads as well as driving the input signal. This is the same for the work by (Parvizi et al. 2016) with their slightly different complementary common-gate current-reuse configuration where the NMOS transistor is stacked on top of the PMOS transistor. As a result, they need to include additional passive loads at the drains of the transistors.

Some authors have gone a step further by combining both complementary common-gate and common-source current-reuse configurations through capacitive cross-coupling technique in a differential LNA topology (Cruz et al. 2015; Salimath et al. 2014; Pan et al. 2017; Wang et al. 2006). This configuration is more widely-known as common-gate current-reuse with capacitive cross-coupling configuration and is depicted in Figure 2.4.

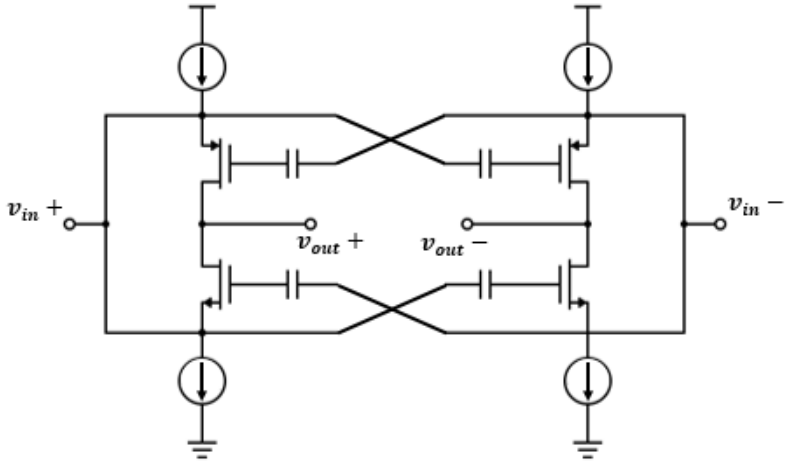

Figure 2.4: Common-gate current-reuse with capacitive cross-coupling configuration.

This capacitive cross-coupling is viable with differential topology since the output of a common-source amplifier is 180° out-of-phase whilst that of common-gate amplifier is in-phase. With the transistors being utilised as both common-gate and common-source amplifiers simultaneously, the resulting gain will be doubled for each half-circuit. This capacitive cross-coupling technique applied on complementary common-gate current-reuse configuration therefore is a type of g_m-boosting technique. By adding up both half-circuits of the differential LNA, the gain will therefore be quadrupled but of course, with the total drawn current being twice larger to supply both half-circuits.

The downside of this current-reuse technique is that it compromises the linearity of the LNA as a result of the high gain it produces. It also has tighter voltage headroom (Wang et al. 2006). This technique therefore is less suitable for applications with high input power at the receiver. Fortunately, this is not the case for MedRadio applications where the input signals arriving at the receiver are low-power RF signals as the human body cannot be exposed to excessive RF radiation.

2.3 Active Shunt Feedback Technique

This technique is normally applied in a LNA to present an appropriate impedance at the input of the LNA for input impedance matching. Commonly, this technique is utilised on wideband LNAs and LNAs with inductorless topology to minimise the size of the IC (Cruz et al. 2015; Adom-Bamfi & Entesari 2016; Bharade et al. 2011; Borremans et al. 2008; De Souza et al. 2017; Im 2013). It is suitably implemented on common-source and cascode LNAs where the input resistance is basically infinite due to the silicon dioxide insulation between the gate and the drain-source channel of the driving transistor. This active shunt feedback technique then helps to bring down the high input resistance of the LNA to a much lower and more appropriate impedance, which is normally close to 50 Ohm. However, when size of the IC is not really a constraint (thus the use of inductors is not an issue), the inductive source degeneration technique is a much more effective and preferred method for input impedance matching of common-source and cascode LNAs.

Typically, an active shunt feedback network takes the form of a common-drain amplifier (or better known as source-follower) with the gate terminal of the driving transistor receiving the output signal from the LNA, and its source terminal sharing the same node with the input of the LNA (Adom-Bamfi & Entesari 2016; Bharade et al. 2011; Cruz et al. 2015). This is depicted by Figure 2.5.

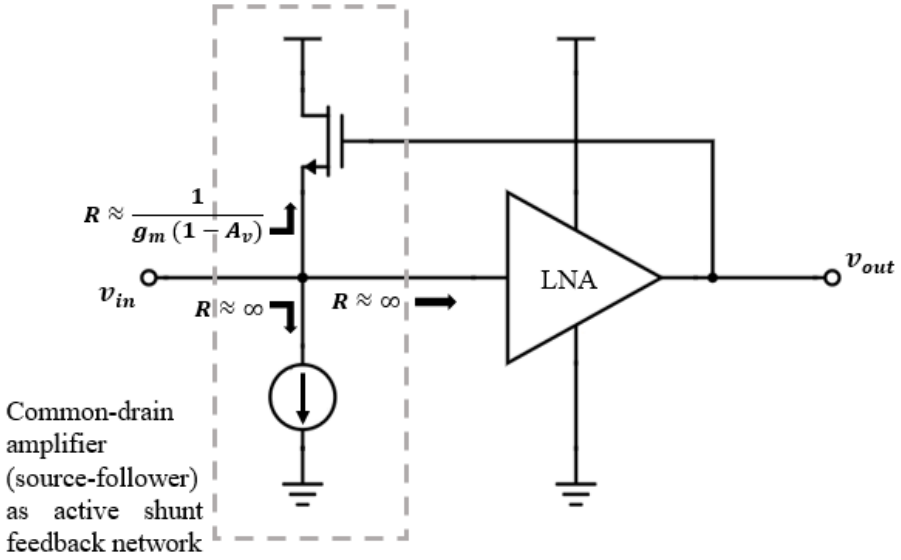

Figure 2.5: Illustration of active shunt feedback technique for a LNA utilising a common-drain amplifier (source-follower) network.

In Figure 2.5, the input of the LNA, the source terminal of the common-drain amplifier's driving transistor and the positive terminal of the common-drain amplifier's current source are sharing the same node. For low-frequency signals entering this node, the approximate input resistance is the resistance looking into the source terminal of the common-drain amplifier's driving transistor, since the resistances looking into the LNA and the positive terminal of the common-drain amplifier's current source are both extremely high. Applying Miller's Theorem (see Appendix) to Figure 2.5, the input resistance of the whole circuit is approximately given by the resistance looking into the source terminal of the common-drain amplifier's driving transistor, and can be expressed by:

$$r_{in} \approx \frac{1}{g_m(1-A_v)} \tag{2.4}$$

where g_m is the transconductance of the common-drain amplifier's driving transistor and A_v is the small-signal voltage gain of the LNA. The input resistance can then be drawn closer to 50 Ohm by obtaining a suitable value for g_m via increasing the current in the source-follower. This also depends on the gain of the LNA; the higher the magnitude of the gain, the less value of g_m needed to obtain close to 50 Ohm input resistance.

Some authors prefer to add a resistor between the source terminal of the common-drain amplifier's driving transistor and the input of the LNA (De Souza et al. 2017; Im 2013; Borremans et al. 2008). This is usually for the purpose of improving the noise figure albeit at the expense of additional power consumption (Borremans et al. 2008). With this additional resistor, the overall schematic can be illustrated by Figure 2.6.

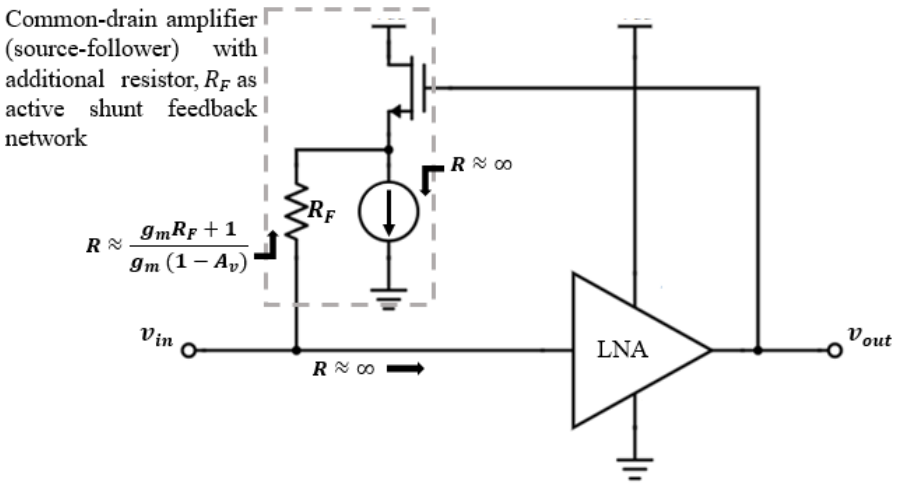

Figure 2.6: Illustration of active shunt feedback technique for a LNA utilising a common-drain amplifier (source-follower) network with additional resistor, R_F between source terminal of driving transistor and LNA's input.

In Figure 2.6, the input of the LNA is only sharing the same node with the resistor of the source-follower network. Again, by applying Miller's Theorem, the input resistance of the whole network, which is approximately the resistance looking into the active shunt feedback network, can now be expressed by:

$$r_{in} \approx \frac{g_m R_F + 1}{g_m(1 - A_v)} \tag{2.5}$$

where g_m is the transconductance of the common-drain amplifier's driving transistor, R_F is the additional resistor of the active shunt feedback network and A_v is the small-signal voltage gain of the LNA.

One obvious disadvantage of any active shunt feedback technique is that there will be some inevitable DC power consumption by this feedback network in addition to that consumed by the main driver of the amplifier. It is therefore important to be frugal in utilising this technique in terms of voltage supply for the source-follower network and its dissipated current.

2.4 Subthreshold Biasing Technique

This is a popular low-power design technique and is also known as weak inversion. Works by (Zafarian et al. 2013; Tang et al. 2011; Kumar et al. 2017; Reddy 2017; Yang et al. 2011; Jeong et al. 2011; Liu & Zhang 2017) amongst others have effectively demonstrated the use of this technique in their respective designs to obtain very low power consumption thus prolonging battery life. Subthreshold biasing occurs when the gate-source voltage V_{GS} of the MOS transistor is less than the extrapolated threshold voltage V_{TH} of the device, but sufficient enough to cause the formation of a depletion region at the surface of the silicon substrate adjacent to the drain-source

channel. The drain current for subthreshold biasing is caused by the flow of diffusion current due to the minority charge carrier concentration gradient, rather than the drift of majority charge carriers in the channel which is negligible. For a NMOS transistor operating in subthreshold region, this is analogous to a *npn* bipolar transistor where the silicon substrate acts as the base whilst the source and drain terminals represent the emitter and the collector respectively.

The drain current for subthreshold biasing can be expressed as (Gray et al. 2010):

$$I_D = \frac{W}{L} I_{D0} exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)\left[1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right] \quad (2.6)$$

where W = gate width, L = gate length, I_{D0} = drain current when gate-source voltage equals threshold voltage, V_{GS} = gate-source voltage, V_{TH} = threshold voltage, n = ratio of sum of gate-oxide capacitance and depletion-region capacitance over gate-oxide capacitance, V_T = thermal voltage and V_{DS} = drain-source voltage. Figure 2.7 depicts the plot of log I_D against V_{GS} where the straight line around the region $V_{GS} < V_{TH}$ represents Equation (2.6) and is known as the subthreshold exponential region (Gray et al. 2010; Razavi 2001).

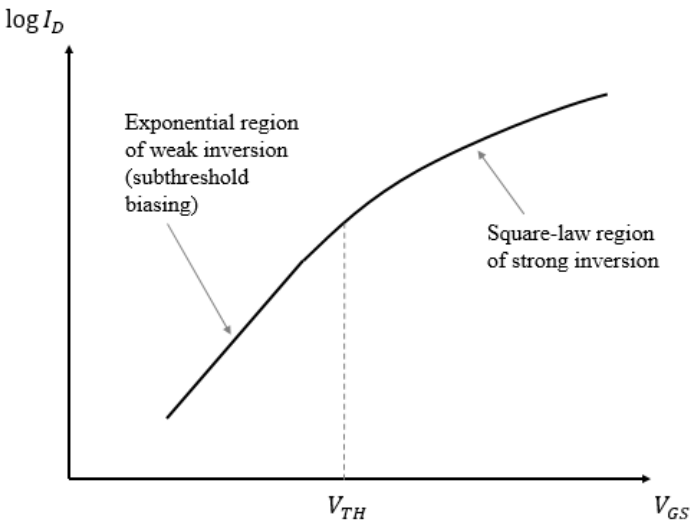

Figure 2.7: Plot of log I_D against V_{GS} showing the exponential region of subthreshold biasing and the square-law I_D-V_{GS} relationship in strong inversion (Razavi 2001).

Also from Equation (2.6), as V_{DS} increases to more than approximately $3V_T$, the drain current becomes almost constant because the last term in the equation approaches unity. This is illustrated in Figure 2.8.

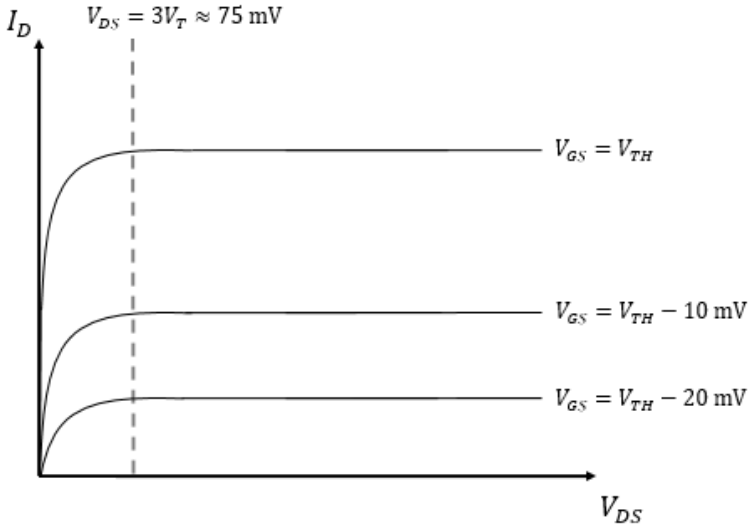

Figure 2.8: Plots of I_D versus V_{DS} with varying V_{GS} for subthreshold biasing (Gray et al. 2010).

It implies that for subthreshold biasing, the MOS transistor merely needs around 0.1 V of drain-source voltage to operate in its saturation region as V_T is only about 25 mV at room temperature. This very low minimum saturation V_{DS} for MOS transistors is therefore very appealing for low-power analogue circuits as less supply voltage is needed to power up the devices.

The transconductance for subthreshold biasing can be obtained by differentiating Equation (2.6) with respect to V_{GS} and can be further simplified to be:

$$g_m = \frac{I_D}{nV_T} = \frac{I_D}{V_T}\frac{C_{ox}}{C_{js}+C_{ox}} \tag{2.7}$$

where C_{ox} = gate-oxide capacitance per unit area and C_{js} = depletion-region capacitance per unit area. From Equation (2.7), the ratio of transconductance to drain current in subthreshold biasing is given by:

$$\frac{g_m}{I_D} = \frac{1}{nV_T} = \frac{1}{V_T}\frac{C_{ox}}{C_{js}+C_{ox}} \tag{2.8}$$

In subthreshold biasing, the ratio of g_m over I_D is significantly higher than that for strong inversion. This implies that for the same amount of drain current, subthreshold biasing produces greater transconductance thus giving better current efficiency. However, to increase the current in subthreshold biasing whilst maintaining the same V_{GS} in the subthreshold region, the width of the MOS transistor will need to be increased as given by Equation (2.6). This eventually will result in a much larger MOS device size hence larger total size of the IC layout.

The use of subthreshold biasing technique for low-power applications is restricted only to those with relatively low operating frequencies. This is due to very

small transition frequency f_T for subthreshold biasing that renders it unsuitable for higher frequencies especially those beyond 1 GHz. The transition frequency f_T is defined as the frequency at which the MOS transistor's current gain falls to unity. However, as the CMOS technology becomes smaller, the transition frequency has been found to be increasing (Yang et al. 2011).

2.5 Previous Works on Low-Noise Amplifiers for MedRadio Applications

Several previous works on LNAs for MedRadio applications are reviewed and discussed in this section. Some of these works are not specifically intended for MedRadio applications, but nevertheless, they possess wideband capabilities to perform reasonably well in the MedRadio frequency range.

2.5.1 Complementary common-source current-reuse MedRadio LNA

Way back in 2011, (Cha et al. 2011) proposed a low-power MedRadio receiver RF front-end using 0.18-μm CMOS technology. This front-end module includes a single-ended LNA that utilises a complementary common-source current-reuse topology. On standalone measurements of the LNA, it achieves gain of 20 dB, NF of 2.8 dB, input RL of 15 dB and IIP_3 of -8.1 dBm with power consumption of only 0.15 mW. Figure 2.9 shows the circuit schematic of the proposed complementary common-source current-reuse LNA.

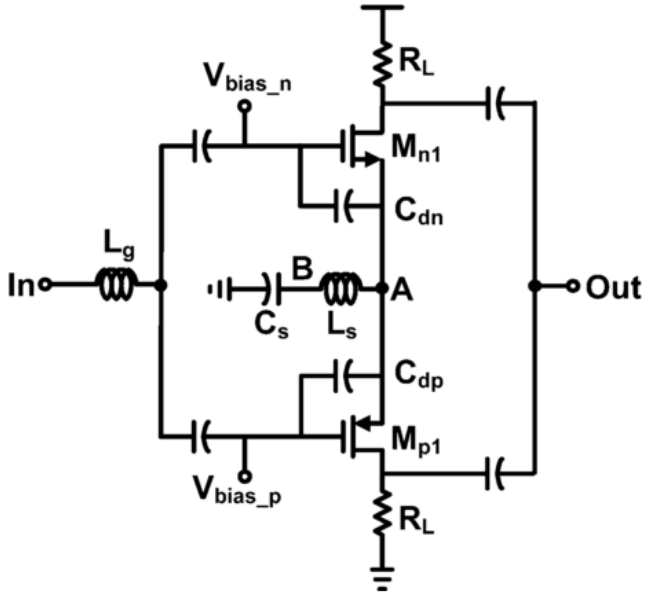

Figure 2.9: Complementary common-source current-reuse MedRadio LNA circuit schematic proposed by (Cha et al. 2011).

In this LNA, a NMOS inductive source degeneration common-source amplifier is being stacked on top of that of a PMOS. Both NMOS and PMOS amplifiers are sharing the same source inductor L_s, AC-grounding source capacitor C_s and AC GND point at their source terminals. The drain current that passes through NMOS transistor M_{n1} is being reused by PMOS transistor M_{p1}. The gate inductor L_g and the gate DC-blocking capacitors of the NMOS and PMOS transistors are external components that form a high-Q passive resonant network before the input of the LNA. The combination of this network and source degeneration inductor L_s gives a very good simultaneous noise and impedance matching at the input of the LNA. This is the main strength of this complementary common-source current-reuse LNA where even with a very low current of 0.15 mA from a 1-V supply, it can still obtain a very low NF of 2.8 dB with a good input RL of 15 dB. The external resonant network also helps to boost the gain of this