STUDY OF CRACK PROPAGATION ON COMPONENT (MULTILAYER CERAMIC CAPACITOR) DURING REFLOW SOLDERING PROCESS

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LIST OF SYMBOLS

Π	Potential energy of the system
A	Crack area
σ_{ij}	Stress distribution
f_{ij}	A dimensionless function of θ
K_n	SIF and the corresponding mode of loading
Kc	Material's characteristic resistance to fracture
v	Poisson's ratio
E'	Elastic modulus of the material depending on the plane analysis
w	Strain energy density
u_i	The displacement field
n_j	The unit outward normal to the contour of integration
δ_{ij}	Kronecker delta
q	Displacement field due to virtual crack extension
J	Fracture mechanics parameter
G	Energy release rate under linear elastic assumptions

LIST OF ABBREVIATIONS

MLCC	Multi-Layer Ceramic Capacitor
SMD	Surface Mounted Device
SMT	Surface Mount Technology
Cu	Copper
Ni	Nickel
Sn	Tin
$BaTiO_3$	Barium Titanite
SIF	Stress Intensity Factor
ERR	Energy Release Rate
FEM	Finite Element Method
VCCT	Virtual Crack Closure Technique
IC	Integrated Circuit
LEFM	Linear Elastic Fracture Mechanics
XFEM	Extended Finite Element Method
SEM	Scanning Electron Microscope
PCB	Printed Circuit Board
CAD	Computer-Aided Design
CTE	Coefficient of Thermal Expansion

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ABSTRAK

Kapasitor Seramik Pelbagai Lapisan (KSPL) adalah sejenis kapasitor Peranti Melekap Permukaan (PMP) yang sekarang ini sering digunakan dalam pelbagai jenis fungsi kapasiti. Disebabkan oleh peningkatan ciriciri frekuensi, kebolehpercayaan yang lebih tinggi, dan kebolehtahanaan voltan yang tinggi, KSPL menerima banyak perhatian berbanding kapasitor lain pada hari ini. Untuk aplikasi yang memerlukan kapasitor yang kecil, KSPL merupakan kapasitor yang terbaik dan sering menjadi pilihan. KSPL sering digunakan sebagai kapasitor pintas, di dalam litar op-amp, penapis, dan juga pelbagai aplikasi lain. Walaubagaimanapun, semasa proses teknologi melekap permukaan (TMP), sebagai contoh, pematerian aliran semula, kapasitor ini mungkin mengalami kecacatan dan patah disebabkan oleh kejutan terma dan juga tekanan yangtidak dapat ditentukan di dalam kapasitor yang berpunca daripada pelbagai sebab. Di dalam kajian ini, dua jenis kapasitor telah dibandingkan dari hasil simlasi dan dipelajari. Proses pematerian aliran semula telah disimulasikan dan diaplikasikan ke atas geomteri untuk diperhatikan kesannya. Beberapa teknik untuk melakukan kajian ini telah dikaji dan satu yang paling sesuai telah dipilih. Kesan tekanan wap dan tekanan terbina di daam kapasitor telah dipelajari. Juga, kesan bahan pateri yang berlainan telah dianalisa dan dipelajari sepanjang projek ini.

ABSTRACT

Multilayer Ceramic Capacitor (MLCC) is a Surface Mounted Device (SMD) type capacitor that is currently used in wide ranges of capacitance functions. Because of its improved frequency characteristics, higher reliability, and higher withstanding voltage, MLCC receives more attention than other capacitors these days. For applications requiring tiny capacitances, MLCC are typically the capacitor of choice. They are employed as bypass capacitors, as well as in op-amp circuits, filters, and other applications. However, during surface mounted technology (SMT) process, for example, reflow soldering process, this capacitor might have defected and fracture due to the thermal shock and undetermined pressure inside the capacitor that comes from many factors. Two types of MLCC are compared from the simulation and studied. The reflow soldering process is simulated and applied to the geometry to be simulated. A few techniques on how to conduct the research has been discussed and one has been chosen. Effects of vapor pressure and the build-up pressure inside the capacitor is reviewed. Also, the effect of different solder materials has been analysed and studied throughout this project.

CHAPTER 1

INTRODUCTION

1.1 Overview

Capacitors are an important part of electronic circuits. Surface-mounted multi-layered ceramic capacitors are one of the most often utilized components in circuit board assemblies. MLCCs offer a wide range of applications due to their small size and high capacitance density, ranging from household gadgets to telecommunication and automobile engineering.[1]

Figure 1.1 shows a cross section of MLCC's basic structure. It is made up of many thin layers of ceramic dielectric material that alternate with silver and palladium metal electrodes in a regular manner. Electrical contact is provided by two metal terminations made up of silver, tin, and nickel layers, which are also used to solder the capacitor to the printed circuit board (PCB).[2]

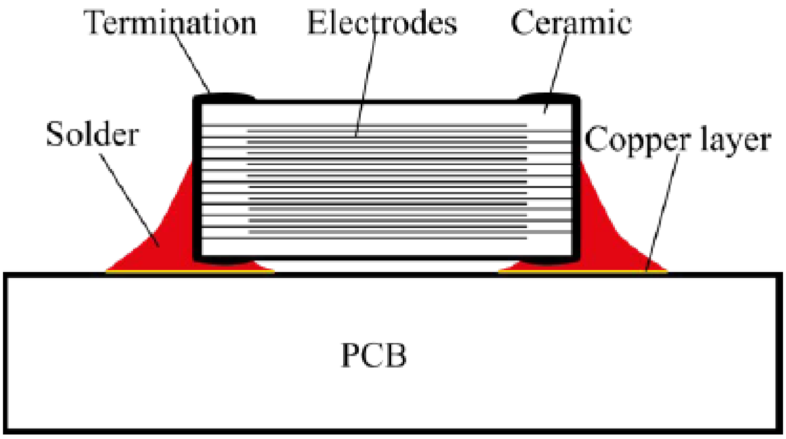

Figure 1.1: Schematic of a MLCC on PCB (cross section)[2]

According to a study conducted by the centre for advanced life cycle engineering, MLCC failures are the most common cause of electronic product malfunction or damage. Because of the wide range of applications and the number of parts employed, high capacitor reliability is necessary to ensure high safety and extended lifetime for electronic systems and assemblies.[2]

Mechanical cracking is the most common type of component failure. The brittleness of ceramic materials is a major contributor.[1] Defects can be present in raw materials or introduced during the production process in the form of fractures and voids. Cracking can also occur during assembly, such as while positioning the capacitor on the PCB, or as bending cracks after soldering in situations with high board flexure.

A finite element model of MLCCs is described in this paper. The thermal burden resulting from the cooling trajectory after soldering has been taken into account. Following that, a mechanical load was applied in the form of board bending. Fracture mechanics methods were applied to initiated cracks based on the finite element analysis stress and displacement distributions, and the related fracture parameters were computed and compared with the associated fracture toughness.

1.2 Project Background

Multilayer ceramic capacitors (MLCC) are important components in electronic systems and are widely employed in a variety of applications by the electronics industry. They are made up of layers of ceramic and metal electrodes that alternate. They have a capacity range of 1 pf to 30μF and are frequently employed as energy storage devices as well as electronic filters.[1]

The reliability question is becoming more important as a result of their application possibilities and the trend of high volumetric efficiency of capacitance with reduced component size. Raw material problems can impair component reliability, but they also go through multiple load fluctuations during their lifetime, which might cause problems. Starting with thermo-mechanical stresses encountered during the manufacturing process, such as fire or delamination. Flaws can also occur during component processing, such as "pick and place" and board bending, especially during board flexing, during assembly, handling, and placement activities.[3] Cracks can also be caused by thermal shock, such as during the reflow soldering process.

The faults produced during the manufacturing process, such as micro fractures and pores in the ceramic, have a significant impact on the reliability of MLCCs. When tensile stress is applied, these anomalies cause stress concentrations, which lead to crack propagation through the ceramic and component fracture.

External stresses combined with pre-existing faults result in high stress levels, fracture propagation, part separation, and a significant reduction in capacity. Internal shorts can also occur, causing damage to the capacitor and adjacent components.

The MLCC 1206 is a capacitor with a capacity of 100 pF and a rated voltage of 1000 VDC that was used in this analysis. Figure 2 shows a cross section of the structure. The dielectric is made of $BaTiO_3$ alloy and has an X7R temperature characteristic, which means it has a tiny capacitance tolerance over a wide temperature range, such as 55°C to + 125°C. Terminations made of Tin, Silver, and Nickel are used to make electrical and mechanical connections. The electrodes indicate a floating design in which the proximity of the top electrodes does not come into close touch with the end termination outside the part, unlike the brick shift design. This type is chosen for overcoming voltage breakdown of the dielectric layer during high voltage applications due to strong electrical field strength.

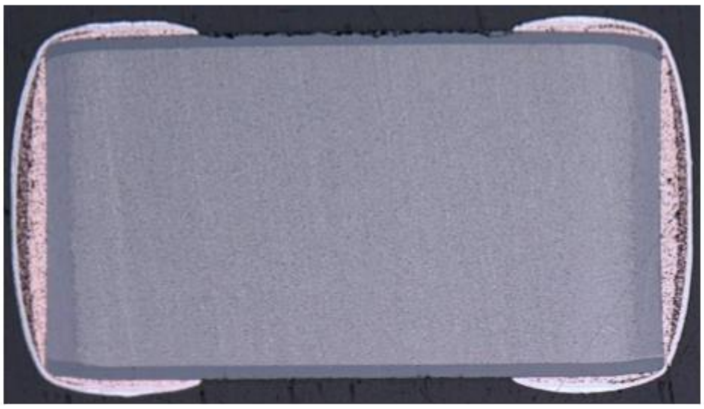

Figure 1.2: Cross Section of MLCC 1206

The major purpose of this research is to look at the behaviour of the ensuing micro fractures in ceramic after soldering and see if they can propagate due to bending strain and if so, in which direction. ANSYS was used to create a finite element model of the 1206 capacitor for this purpose. Critical stress zones have been explored and thermal cool down simulation after soldering has been considered. Furthermore, using linear elastic fracture mechanics, a four-point bending simulation was performed and the crack behaviour was examined.

1.3 Problem Statements

Crack can be said as a type of discontinuity in a solid body that can be characterized by possessing an initiation or nucleation point and this point can grow to a finite size with time, either leading, or not, until the moment that a material is fracture. During reflow process, a lot of factors can contribute to the formation of crack where these factors are about to be investigated and identified.

It has been observed that vapor pressure that is trapped between the components and the solder contribute to the initiation of crack during the reflow process. Also, pressure that has been building up around the cornering lead to the formation of a high-stress concentration area during the reflow process that eventually contribute to the initiation and propagation of crack. Apart from that, different materials of the solder in contact during the reflow process becomes one of the main factors in crack initiation. Moreover, crack size also plays an important role on the propagation of a crack and its behaviour. Lastly, effects of reflow on crack initiation and propagation also must be identified to solve the problems stated above.

1.4 Objectives

1. To choose the appropriate technique of the numerical simulation for the crack analysis.
2. To investigate the effect of vapor pressure on the crack initiation.
3. To evaluate the build-up pressure near the cornering that leads to high-stress concentration zone in the crack initiation process.
4. To assess the effect of different solder material in contact leading to crack initiation.
5. To examine the effect of crack initial size to crack propagation and fracture.
6. To investigate the effect of reflow process on crack.

1.5 Scope of Work

The scope of work in this research is to study the crack propagation on electronics components during reflow soldering process using numerical simulation. In order to understand the delamination mechanism, it is important to understand the properties of (Epoxy-Cu)-Cu interface in the range of temperature from reflow back to room temperature. Also, it is crucial to identify if there is moisture or vapor. If there is, does it weaken the interface and what is the concentration during reflow. These properties need to be characterized.

Next, the second firing temperature that is about the residual stress in the thin electrode layers need to be identified. The possibilities of it to become compressive at the reflow peak temperature need to be identified. Apart from that, it is to be understood the fracture of $BaTiO_3$. To do this, characterization of its defect condition is to be done.

Once all these criteria and properties is determined, the crack initiation and propagation during reflow can be understood and prevented in the future. Numerical simulation is one of the effective ways to do this.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Prior studies must be understood before moving on to the study and analysis of the suggested approach. This chapter also reviews past studies and methodologies utilised in other research projects. Many researchers conducted fracture experiments in order to explain crack analysis using various approaches and improve the formulation. The stress intensity factor (SIF) and the energy release rate (ERR) are two metrics that are used to assess the structure's failure [4]. SIF and ERR calculations utilising various methods in combination with the finite element method (FEM) are examined. The reviews enable the suggested technique to be improved and developed.

2.2 Review of Fracture Mechanics

Griffith observed that the rupture phenomena of interior fractures and defects play a key influence in the beginning and spread of fracture in a previous research. In this work, the total energy change throughout the cracking process was used to establish a connection between fracture strength and crack size [5]. Westergaard, Irwin, Sneddon, and Williams used a different technique to obtain a solution based on the stress field near a sharp crack-tip. They expanded Griffith's theory by adding yield and utilising a coordinate system cantered at the crack-tip [5]. Rice proposed a non-linear energy release rate based on the J-integral, a route independent line integral. The J-integral around the crack-tip is defined as illustrated in Figure 2.1, where the energy release rate is computed using a line integral along the curve [6]. Rice and Rosengren and Rice and Levy were the first to use generic finite element methods to solve fracture mechanics issues [7]. The J-integral is a path-independent contour integral that equals the potential energy rate of change for a nonlinear elastic solid during crack expansion. In a two-dimensional finite element analysis, Rybicki and Kanninen [8] presented a fundamental idea of Virtual Crack Closure Technique (VCCT) to calculate stress intensity factor by assessing the energy release rate as the crack widens [9].

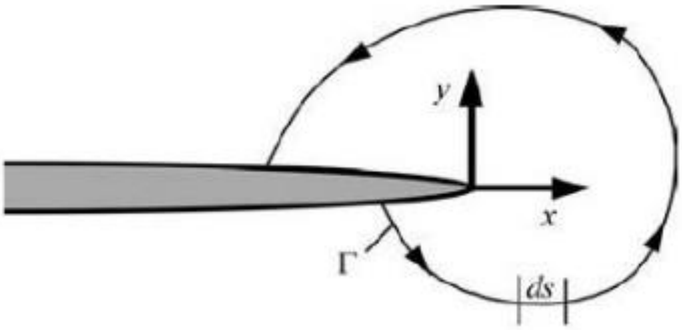

Figure 2.1: Arbitrary Contour around the crack-tip [9]

2.3 Vapor Pressure and Residual Stress as Brittle Crack Growth Enhancement

Moisture-induced popcorn cracking of electronic packages during surface mounting to the printed circuit board remains a major reliability risk in IC packaging [10]. Depending on where the interface delamination begins, popcorn cracking can be classified into three types [11]. In Type I, the package crack is caused by delamination of the die pad/moulding compound interface. Package cracks of Type II originate from the die attach/die pad interface delamination, whereas package cracks of Type III originate from the die surface/moulding compound interface delamination [12]. Using traditional fracture mechanics, the three types of cracking have been extensively studied [13]. These studies, as well as Liu et al.'s and Fan et al.'s discussions of the limitations of approaches based on conventional fracture mechanics [14].

Polymeric materials are used in a variety of electronic packaging applications. Epoxy resin and silica filler are the main ingredients in polymeric moulding compounds and adhesives like die-attach and underfill [15]. The polymeric materials contain numerous pores and cavities, particularly at the filler particle-polymer matrix interfaces and the polymer-silicon interfaces. Moisture diffuses through the polymeric materials and condenses within the micropores in humid conditions [16]. The package is subjected to soldering shock temperatures ranging from 220 to 260 °C during reflow soldering [17]. The elastic modulus and yield strength of moulding compounds decrease by an order of magnitude at these temperatures. At the same time, rapidly vaporising moisture can produce vapour pressures of 3–6 MPa within the voids [18]. During reflow soldering, these pressures are comparable to the yield strengths of moulding compounds and adhesives.

Intrinsic and extrinsic moisture effects on interface delamination and package cracking can be classified. The extrinsic level includes two interconnected effects [19]. The rapidly vaporising moisture exerts tractions on the delaminated interface, resulting in a mode I crack driving force that increases as the crack size increases. Background stresses in IC packages, on the other hand, which are mostly thermal in nature, cause a mode II loading component on polymer-silicon interfaces [11]. The increasing magnitude of the vapour pressure-induced driving force shifts the interface loading from mode II to mode I dominant as the crack grows. Both of these effects are extremely damaging to the interface's integrity.