

UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Tambahan
Sidang Akademik 2000/2001

April/Mei 2001

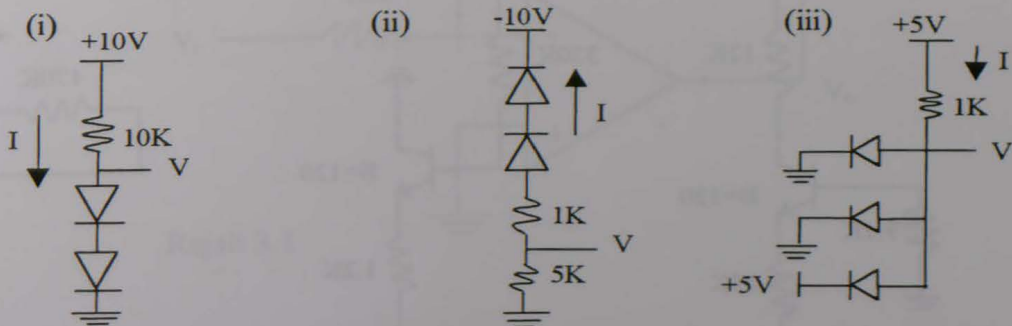
ZCT 106/3 - Elektronik

Masa : 3 jam

Sila pastikan bahawa kertas peperiksaan ini mengandungi **DUABELAS** muka surat yang bercetak sebelum anda memulakan peperiksaan ini.

Jawab kesemua **EMPAT** soalan. Calon-calon boleh memilih menjawab kesemua soalan dalam Bahasa Malaysia. Jika calon-calon memilih untuk menjawab dalam Bahasa Inggeris, sekurang-kurangnya satu soalan wajib dijawab dalam Bahasa Malaysia.

1. (a) Tentukan voltan V dan arus I seperti yang ditunjukkan dalam rajah 1.1 semasa pengaliran, voltan diod adalah $0.7V$.

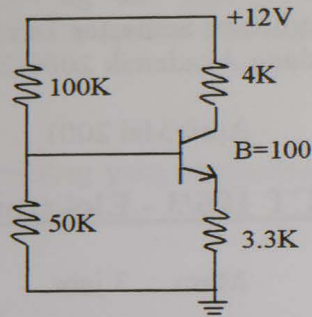


Rajah 1.1

(30/100)

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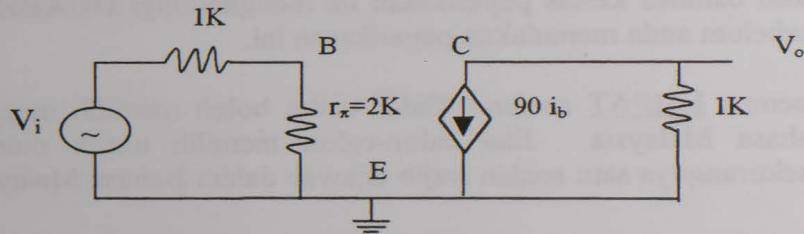
(b) Tentukan dengan tepat nilai I_B , I_C , I_E dan V_C untuk rajah 1.2.



Rajah 1.2

(40/100)

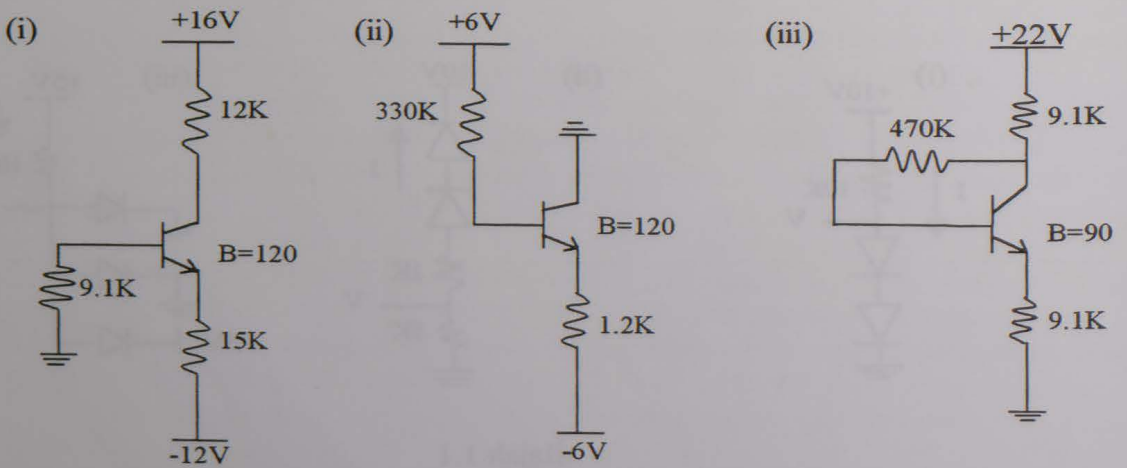
(c) Dapatkan V_o/V_i untuk litar model transistor yang ditunjukkan pada rajah 1.3.



Rajah 1.3

(30/100)

2. Untuk litar dalam rajah 2.1 tentukan I_B , I_C dan V_{CE} .

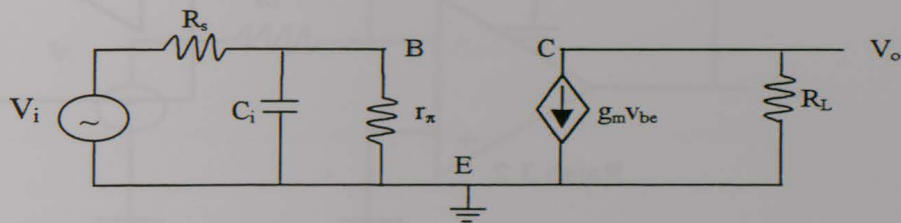


Rajah 2.1

(60/100)

(b) Untuk model litar transistor dalam rajah 2.2:

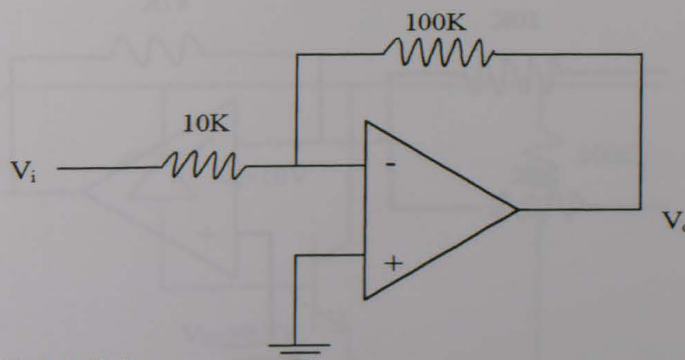
- (i) Terbitkan suatu ungkapan untuk gandaan voltan V_o/V_i sebagai fungsi frekuensi. Seterusnya dapatkan gandaan DC dan frekuensi 3-dB.
- (ii) Hitung gandaan DC dan frekuensi -3-dB untuk $R_s = 20K\Omega$, $r_\pi = 100K$, $C_i = 6pF$, $g_m = 144 \text{ mA/V}$ dan $R_L = 1K$.
- (iii) Hitung frekuensi pada keadaan gandaan adalah 0dB.



Rajah 2.2

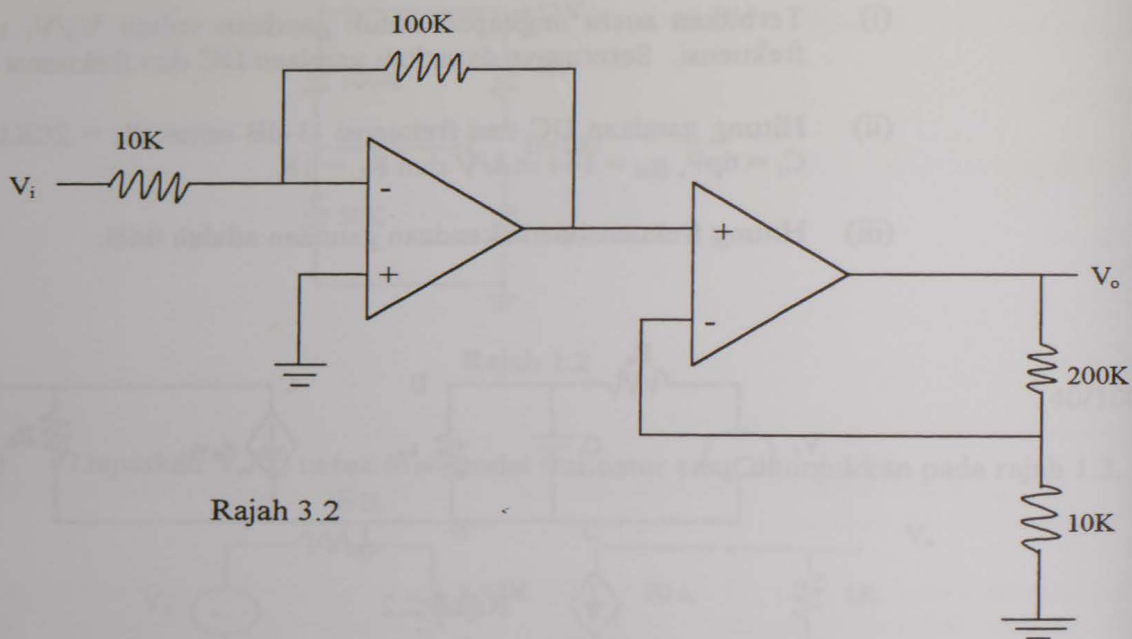
(40/100)

3. (a) (i) Hitung voltan output untuk $V_i = 1V$, untuk litar rajah 3.1.



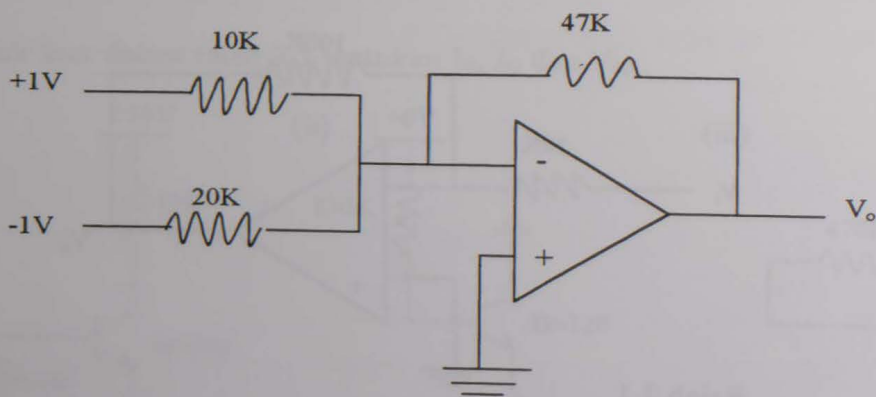
Rajah 3.1

(ii) Hitung voltan output untuk $V_i = 10\text{mV}$ bagi litar rajah 3.2.



Rajah 3.2

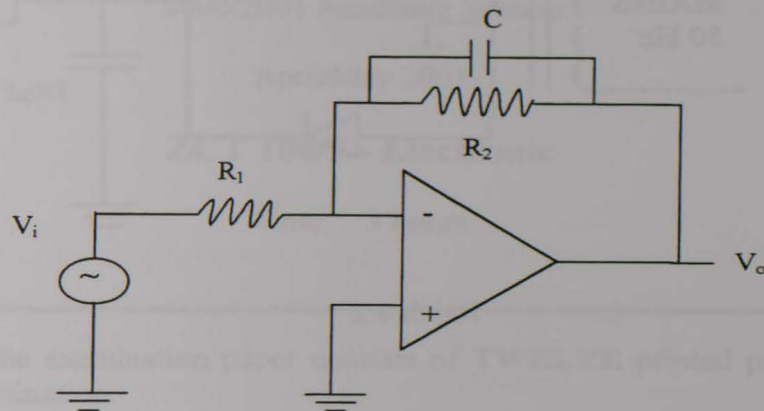
(iii) Hitung voltan output untuk litar rajah 3.3.



Rajah 3.3

(60/100)

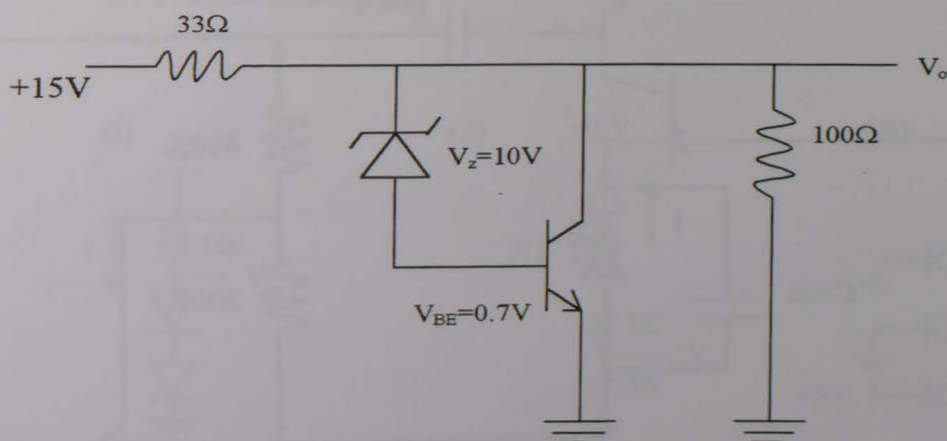
- (b) (i) Dalam rajah 3.4 tetapkan peranti-peranti yang sesuai untuk mencapai suatu frekuensi penggalan 1kHz dengan gandaan DC 20 dB dan rintangan input sekurang-kurangnya 10 k Ω .
- (ii) Pada frekuensi berapakah gandaan menjadi uniti



Rajah 3.4

(40/100)

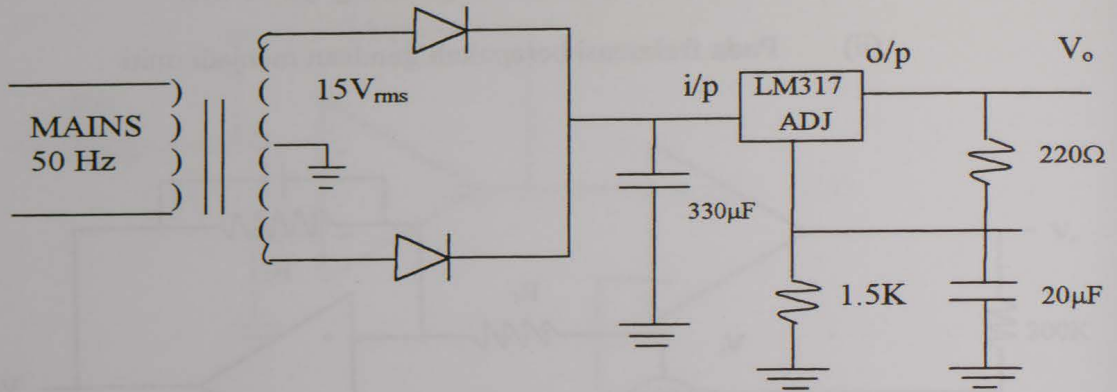
4. (b) Tentukan voltan teratur dan arus litar untuk pengatur pirau seperti rajah 4.1



Rajah 4.1

(30/100)

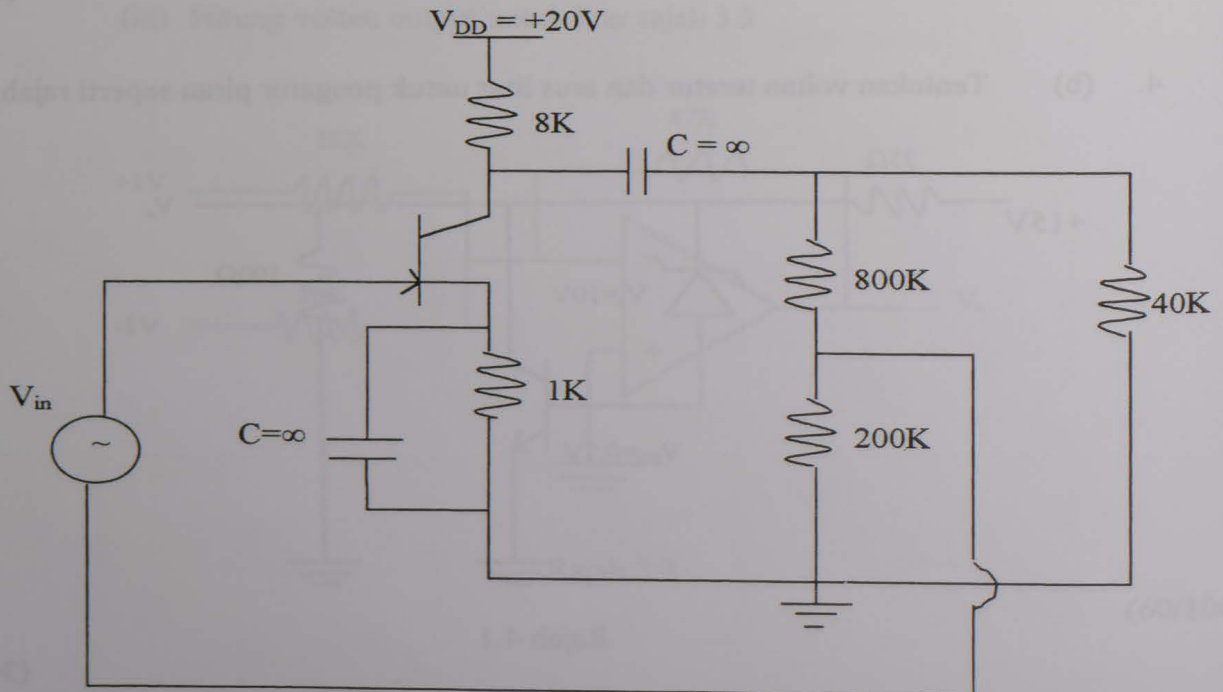
- (b) Tentukan voltan output teratur daripada litar rajah 4.2 jika $V_{REF} = 1.25V$.



Rajah 4.2

(30/100)

- (c) Hitung gandaan dengan dan tanpa suapbalik untuk JFET saluran-N seperti rajah 4.3, jika $g_m = 5000 \mu s$.



Rajah 4.3

(40/100)

TERJEMAHAN

UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2000/2001 Academic Session

April/May 2001

ZCT 106/3 - Electronic

Time : 3 hours

Please check that the examination paper consists of **TWELVE** printed pages before you commence this examination.

Answer all **FOUR** questions. Candidates may choose to answer all questions in the Malay Language. If candidates choose to answer in the English Language, it is compulsory to answer at least one question in the Malay Language.

1. (a) In Fig. 1.1 find the voltage V and the current I as indicated. The diodes drop $0.7V$ when conducting.

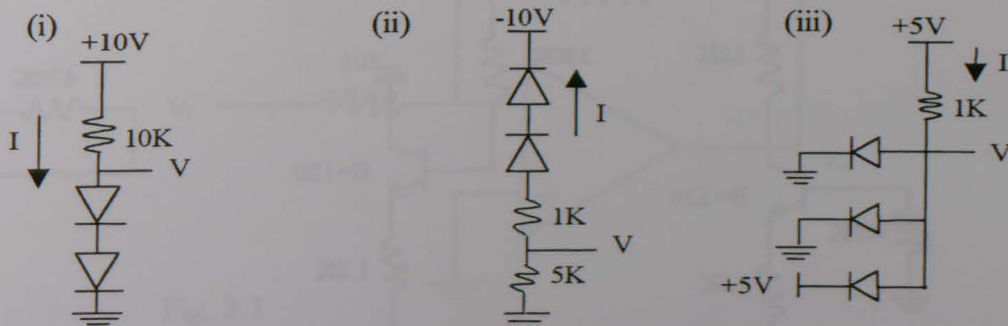


Fig. 1.1

(30/100)

... 8/-

- (b) Find exactly the DC values of I_B , I_C , I_E and V_C for Fig. 1.2.

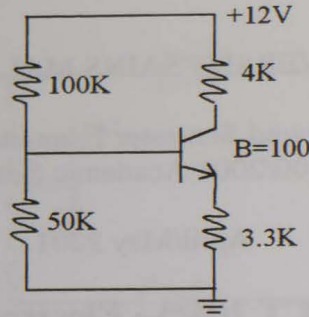


Fig. 1.2

(40/100)

- (c) Find V_o/V_i for the transistor model circuit shown in Fig. 1.3.

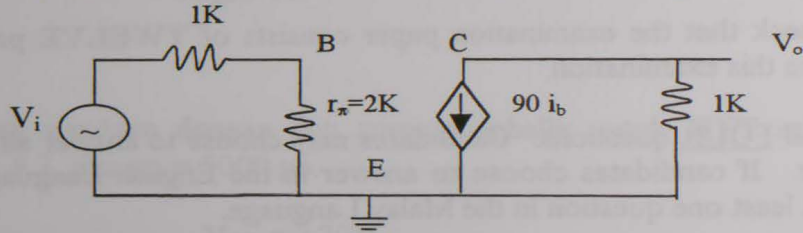


Fig. 1.3

(30/100)

2. For the circuits shown in Fig. 2.1 determine I_B , I_C and V_{CE} .

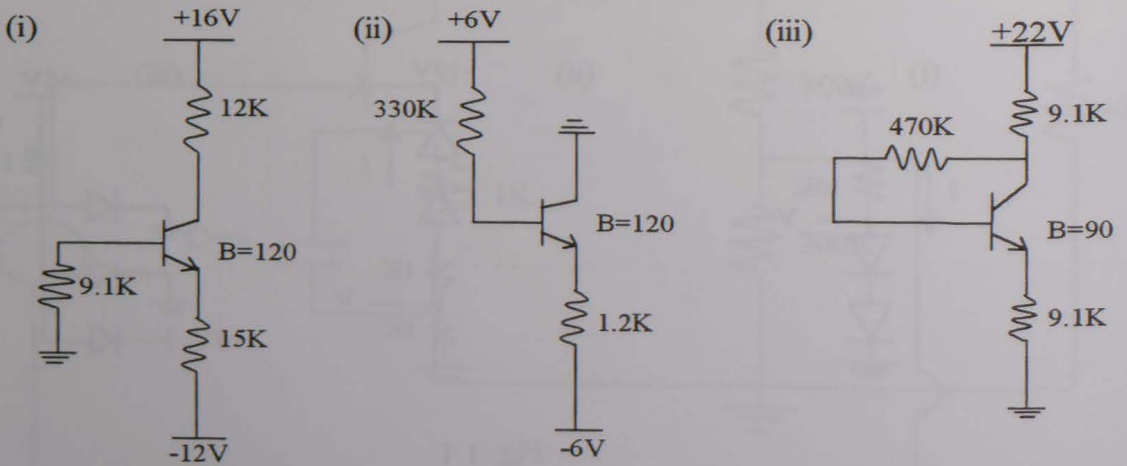


Fig. 2.1

(60/100)

... 9/-

(b) For the transistor circuit model shown in Fig. 2.2:

- (i) Derive an expression for the amplifier voltage gain V_o/V_i as a function of frequency. From this find expressions for the DC gain and the 3-dB frequency
- (ii) Calculate the DC gain and the -3-dB for $R_s = 20K\Omega$, $r_\pi = 100K$, $C_i = 6pF$, $g_m = 144 \text{ mA/V}$ and $R_L = 1K$.
- (iii) Calculate the frequency at which the gain become 0dB.

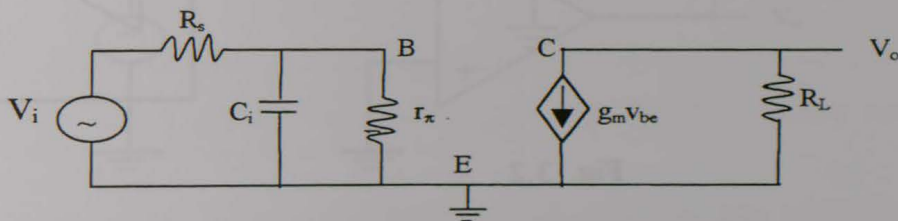


Fig. 2.2

(40/100)

3. (a) (i) Calculate the output voltage for an input of $V_i = 1V$, for the circuit in Fig. 3.1.

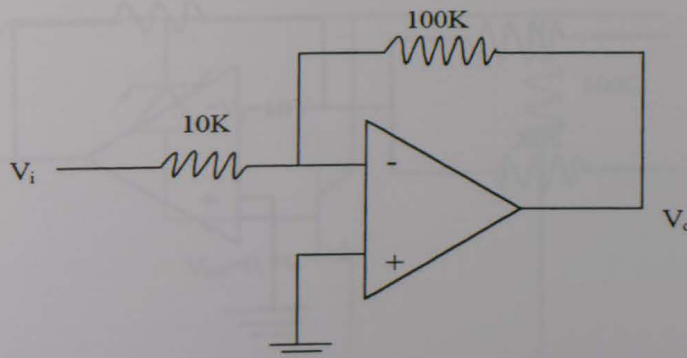


Fig. 3.1

... 10/-

- (ii) Calculate the output voltage for an input of $V_i = 10\text{mV}$ for the circuit in Fig. 3.2

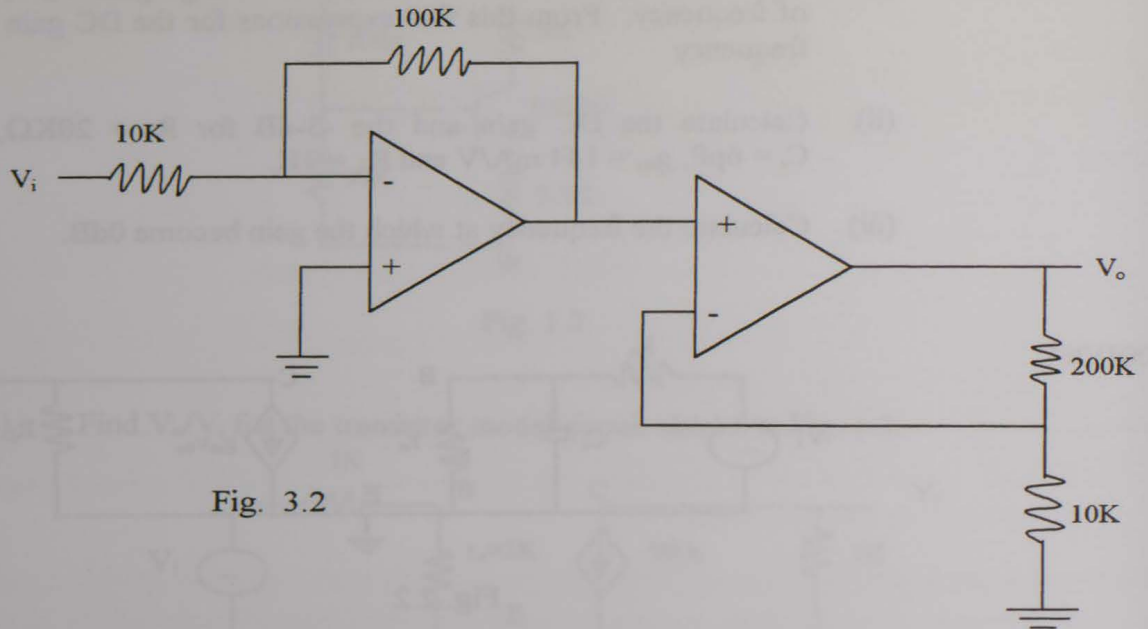


Fig. 3.2

- (iii) Calculate the output voltage for the circuit in Fig. 3.3

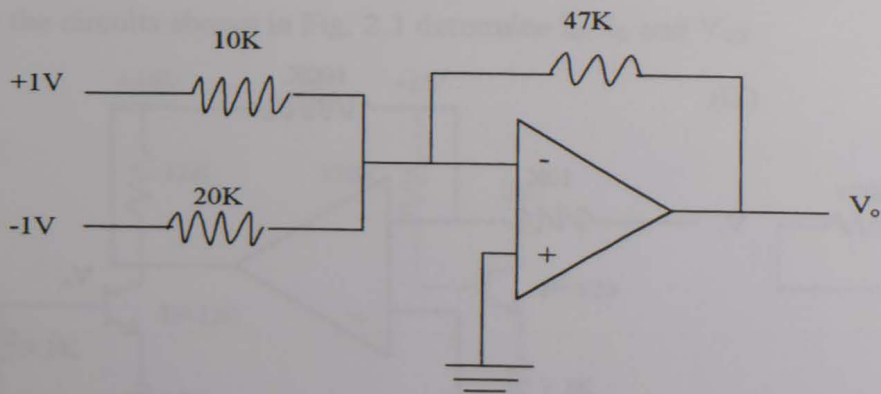


Fig. 3.3

(60/100)

... 11/-

- (b) (i) In Fig. 3.4 specify suitable components to achieve a cut off frequency of 1 kHz, with a DC gain of 20dB and input resistance of at least 10K.
- (ii) At what frequency does the gain drop to unity.

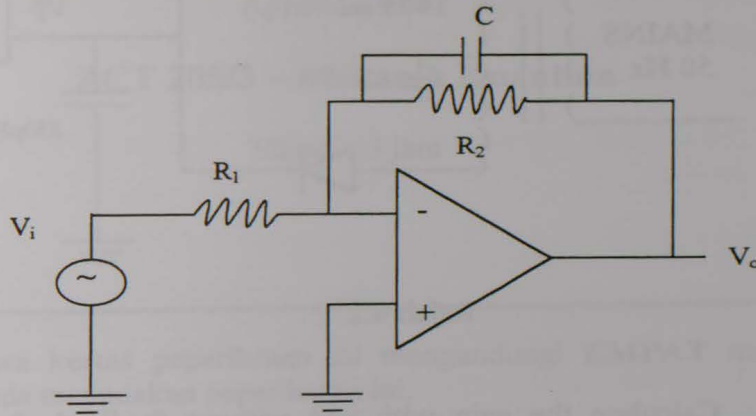


Fig. 3.4

(40/100)

4. (a) Determine the regulated voltage and circuit currents for the shunt regulator, as in Fig. 4.1.

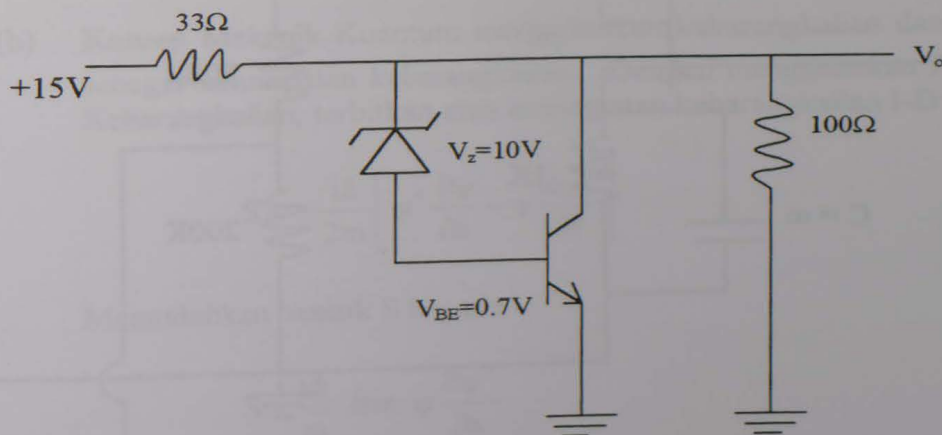
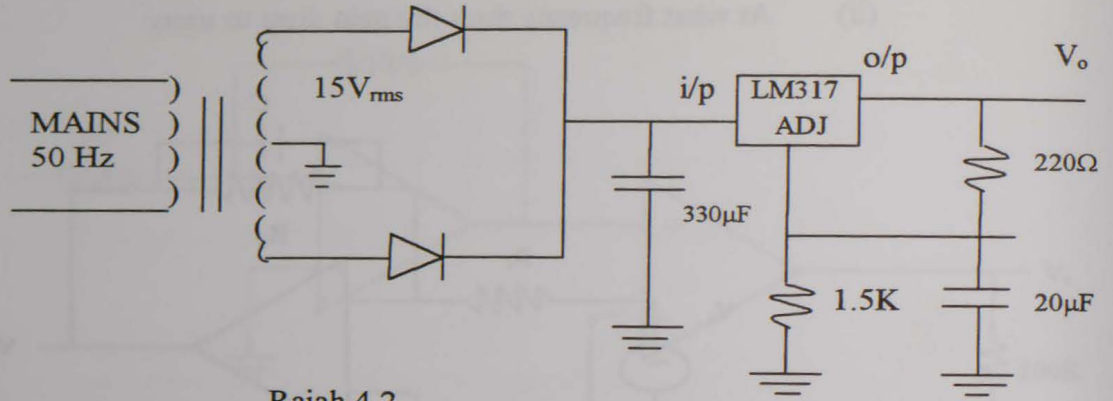


Fig. 4.1

(30/100)

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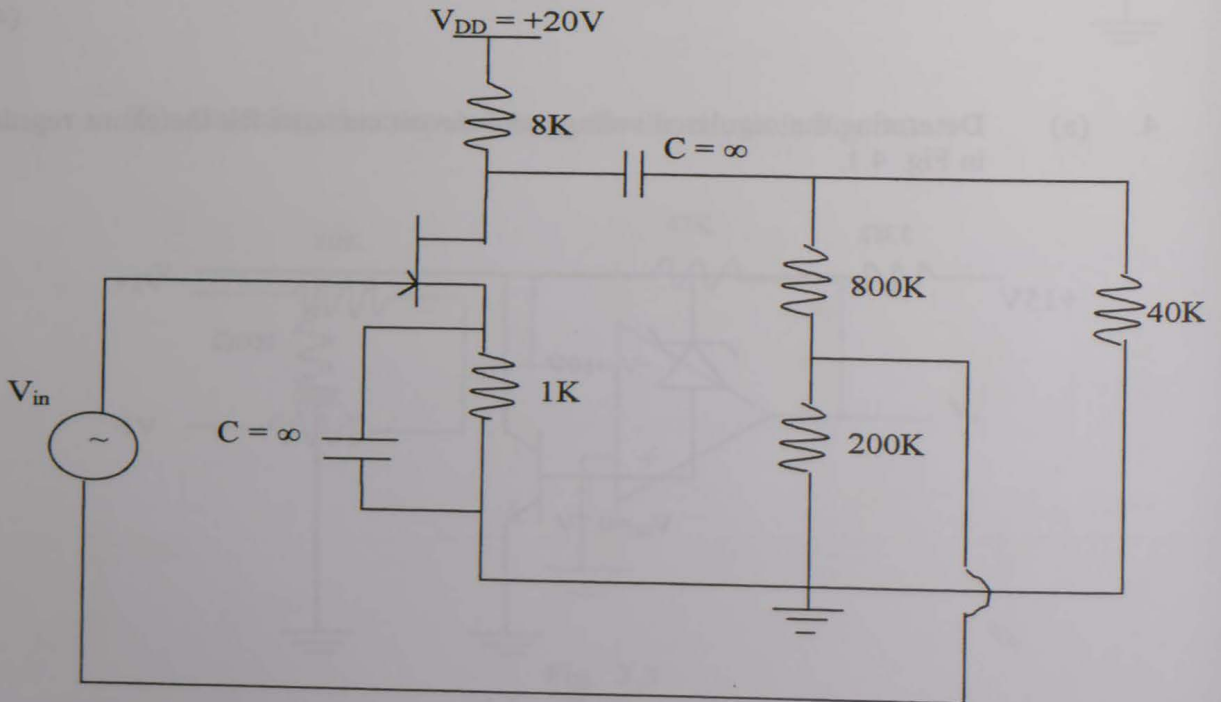
- (b) Determine the regulated output voltage from the circuit of Fig. 4.2 if $V_{REF} = 1.25V$.



Rajah 4.2

(30/100)

- (c) Calculate the gain with and without feedback for an N-channel JFET as shown in Fig. 4.3 if $g_m = 5000 \mu s$.



(40/100)

Rajah 4.3