POWER DELIVERY NETWORK MODELING AND SIMULATION BY USING DELAUNAY-VORONOI TRIANGULATION AND THE LATENCY INSERTION METHOD

CHIN WEI CHUN

UNIVERSITI SAINS MALAYSIA

2018

POWER DELIVERY NETWORK MODELING AND SIMULATION BY USING DELAUNAY-VORONOI TRIANGULATION AND THE LATENCY INSERTION METHOD

by

CHIN WEI CHUN

Thesis submitted in partial fulfillment of the

requirements for the degree of

Bachelor of Engineering (Electronic Engineering)

JUNE 2018

ACKNOWLEDGEMENT

First of all, I would like to express my greatest gratitude to my family for their support throughout the journey I carrying with the project. Without their positive encouragement, I may not have a good progress on my project.

Secondly, I would like to send my appreciation to my dedicated supervisor, Dr. Patrick Goh Kuan Lye for his guidance and supervision throughout the period of the research. He always shows great patience during our discussion and his constructive comments and suggestions have contributed a lot to the success of the project.

Next, I would like to express my appreciation to my colleagues and friends. They have shared with me on idea and suggestions which might helpful for my project. Besides that, their moral support to me was another key for me to complete the project successfully.

Last but not least, I would like to thank School of Electrical and Electronic Engineering, Universiti Sains Malaysia which showed full support on the project and all those that indirectly contributed to this project. I really appreciated it and I would like to express my gratitude to all of you again.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ADE	Alternating Direction Explicit
ADE-LIM	Alternating Direction Explicit-Latency Insertion Method
DC	Direct Current
DGTD	Discontinuous Galerkin Time-Domain
FFT	Fast Fourier Transform
IC	Integrated Circuit
LILIM	Locally Implicit LIM
LIM	Latency Insertion Method
PDE	Partial Differential Equation
PDN	Power Delivery Network
PI	Power Integrity
PCB	Printed Circuit Board
RPD	Return Path Discontinuities
SI	Signal Integrity
SPI	Signal and Power Integrity
SPICE	Simulation Program with Integrated Circuit Emphasis
Via	Vertical interconnect access
VRM	Voltage Regulator Modulator

LIST OF SYMBOLS

C	Capacitance
G	Conductance
I	Current
$\tan(\delta)$	Dielectric loss tangent
σ	Electrical conductivity
ρ	Electrical resistivity
Z	Impedance
L	Inductance
μ_o	Permeability free space
μ	Permeability of a dielectric
ε_o	Permittivity free space
ε	Permittivity of a dielectric
μ_r	Relative permeability of a dielectric
ε_r	Relative permittivity of a dielectric
R	Resistance
δ_c	Skin depth
Δt	Time step
V	Voltage

POWER DELIVERY NETWORK MODELING AND SIMULATION BY USING DELAUNAY-VORONOI TRIANGULATION AND THE LATENCY INSERTION METHOD

ABSTRACT

Power integrity of a design plays an important role in affecting the signal integrity and the overall performance of the design. Therefore, the concern of the project is on the performance of power delivery network (PDN) on power plane. The research is focused into the analysis of PDN by modeling and simulation of the power plane. In the project, power plane is modeled using Delaunay-Voronoi algorithm and for simulation, a fast transient simulation algorithm which is latency insertion method (LIM) is applied. However, typical LIM algorithm is facing problem on its stability. Therefore, in the project, modeled power planes are simulated with basic LIM and voltage-in-current formulated LIM. The transient response and direct current (dc) response of the PDN are simulated and discussed and the simulated results from the two algorithms are compared in term of their accuracy and stability. The results has shown the effect of meshing size and shape to the simulated response. For PDN simulation, the results have shown the change in maximum stable time step of basic LIM from 10 ps to 2 ps due to the usage of finer meshing. For improved LIM, the results has shown a stable output over all time steps but with an increase in degradation of accuracy as tabulated in Table 4.4 and 4.5. In overall, basic LIM has shown its strength on the accuracy provided that the simulation is stable while improved LIM has shown its strength on stability but its accuracy degrades with the increase of time step.

PEMODELAN DAN SIMULASI RANGKAIAN PENYAMPAIAN KUASA MELALUI TRIANGULASI DELAUNAY-VORONOI DAN THEORI PEMASUKAN LATENSI

ABSTRAK

Integriti kuasa dalam satu produk elektronik memainkan peranan yang penting dalam menentukan integriti isyarat dan prestasi produk tersebut secara keseluruhannya. Berhubungan dengan itu, salah satu tumpuan projek ini adalah berkaitan dengan prestasi rangkaian penyampaian kuasa dalam permukaan kuasa litar bersepadu and papan litar tercetak. Dalam projek ini, penyelidikan telah berfokus kepada penganalisasian rangkaian penyampaian kuasa melalui model dan simulasi. Permukaan kuasa telah dimodel melalui theori Delaunay-Voronoi. Untuk menjalankan simulasi, satu kaedah kaedah pemasukkan latensi (LIM) telah digunakan. Namun begitu, kaedah LIM biasa terdapat masalah dalam kemantapannya. Demi menghadapi masalah ini, satu kaedah LIM yang telah diubahsuai turut digunakan dalam projek ini. Keputusan simulasi yang diperolehi melalui kedua-dua kaedah LIM akan dibandingkan melalui aspect ketepatan dan kemantapan kaedah masing-masing. Keputusan yang diperolehi melalui projek ini telah menunjukkan kesan struktur rangkaian kuasa terhadap performansinya. Bagi proses simulasi, kaedah LIM basia pula menunjukkan penurunan kemantapannya daripada 10 pikosaat kepada 2 pikosaat apabila saiz rangkaian dikurangkan. Kemantapan and ketepatan bagi kaedah LIM baru pula ditunjukan dalam Meja 4.4 dan 4.5. Secara umunnya, LIM biasa menunjukkan ketepatannya dalam linkungan jarak masa yang mantap dan LIM baru pula menunjukkan kemantapannya dengan penurunan di ketepatannya apabila jarak masa dinaikkan.

CHAPTER 1

INTRODUCTION

1.1 Research Background

In electronic design, the performance of a design is closely related to the signal integrity (SI) of the design. The growth of technology makes the demand on system miniaturization, lower power consumption and cost, higher performance and as well as higher speed applications getting greater in semiconductor industry. During the process of scaling down the devices size and improving the operation speed, high speed interconnect effect does exist in the design. Therefore, the task to maintain the SI of a design is getting more complex and challenging [1].

From the analysis conducted on the SI of a high-speed digital design, it was found that power distribution of the design does have a direct effect on the SI. Since the power supply noise across the transistors will influence the efficiency of signal propagation, the concern on power distribution is getting bigger in recent years. Moreover, the effectiveness of power distribution has in turn limited the scaling of transistors due to the voltage level consideration. To further scale the transistor size, a smaller operating voltage is required but when a lower voltage level is applied, the effect of power supply noise will be in turn more obvious, which increases the difficulty in managing the SI of the product. Therefore, with the aim to produce a product with a better SI, the power integrity (PI) of the design should be taken care too. This involves the design and analysis

of PDN for both IC and PCB that make up the whole design. A good PDN should able to deliver clean power to all the devices in the design, however due to design complexity, this is a challenging task.

From last two decades, a target impedance method is used to design a PDN. This approach will analyze on the impedance characteristics of the PDN and use a target impedance as a parameter in designing a PDN that able to generate a lower power supply noise. This changes the design methodology of PDN and nowadays in industry, when managing the SI and PI of a design, the SI and PI design are conducted simultaneously in the design flow and associated with each other to analyze on the overall performance. This again shows the increasing importance of PDN design [2], [3].

To guarantee the performance of PI and SI of an electronic device, the PDN of the design must be simulated in an efficient way. Instead of manually measurement after fabrication which is time consuming, software simulation is a better way in handling the situation as problem can be detected in an earlier stage through such approach. This approach included modeling and simulation of the power plane. In term of modeling, methods like DGTD modeling [4], [5] or lumped model approximation can be applied. In lumped model approximation, power plane modeling comes along with a meshing procedure. Meshing of power plane into nodes and branches is having the purpose to extract the impedance value of a power plane. Meshing can be carried through rectangular or square meshes, and it is a good approach in regular shaped PDN modeling [6]. However, due to miniaturization, arbitrary shaped PDN is used with the purpose of space saving. This rises the selection of meshing approach from rectangular mesh to triangular

mesh in order to improve the accuracy of simulation. Delaunay Triangulation and Voronoi Tessellation is one of the suitable meshing technique to be applied on PDN modeling as it is based on triangular meshing algorithm and its output can be closely associated to simulation algorithms like SPICE and LIM [7], [8].

For PDN simulation, latency insertion method (LIM) algorithm comes with a great advantage on its fast and accurate outcome. The time consumed for LIM simulation is quite independent from the number of nodes on modeled PDN [9]. Therefore, LIM is gaining its attention for PDN simulation especially in handling large signal network. However, basic LIM comes with stability issue. Therefore, it is a great direction to research on improved LIM algorithm on its stability and advantage in fast transient simulation [10].

1.2 Problem Statement

Since the power distribution of a design is getting more concern, more and more methods or algorithms in modelling and simulation of the PDN of a design have been introduced in order to investigate its power integrity. A typical algorithm for large network simulation is using SPICE. However, the algorithm becomes inefficient when the design getting complicated. In term of number of nodes, the lager number of nodes to be simulated, the longer the time taken for SPICE to complete the simulation. This brings down the efficiency of large signal network analysis as more and more transistors are available in a single chip. In order to counteract the problems in those typical algorithms, LIM algorithm has been introduced. LIM provides a faster track in the simulation of large signal network and is suitable for both linear and nonlinear network [9].

LIM is well-known in power plane simulation due to its fast computing time however LIM formula is facing a limitation on its stability. Transient simulation using LIM is carried by updating the node voltages and branch currents per time step. However, basic LIM has a limit on the upper bound time step that can be chosen for simulation. The upper bound of time step is depend on the smallest impedance value that exist in the circuit model and hence, this issue restricts the time step used in simulation to a certain low value. Moreover, this issue becomes significant if circuit approximation is used in LIM simulation by adding on small value of capacitance or inductance to a circuit so that it fulfilled LIM's topology. In order to maintain the accuracy, a very small impedance value will be added for such situation and this in turn scales down the maximum allowable time step to a tiny value. Hence, this causes the increase in simulation time and cost. To improve the performance of LIM in simulation, some versions of improved LIM have been purposed like LILIM [8], matrix-based LIM [11] and voltage-in-current LIM [10].

Although LIM can provide a fast simulation on the performance of PDN, LIM cannot be apply directly on a PDN. As all LIM versions are only applicable to circuit model that fulfills LIM's topology. Therefore, to carry on simulation of PDN through LIM, the equivalent circuit model of the PDN has to be extracted first by modeling of PDN. The modeling of PDN can be carried through lumped model approximation and one of the step for this approximation to be carried is through meshing. Meshing of PDN separates PDN into various portions and with the aid of formulae, the parasitic component of each mesh can be extracted and through that an equivalent circuit model can be formed by combining the circuit model of each mesh. Since, irregular shaped PDN is getting common in semiconductor design to minimize the size and volume of the design, modeling through rectangular mesh is suffered from staircase approximation. In

conjunction with that, Delaunay-Voronoi modeling that uses triangular meshing approach is applied to arbitrary shaped PDN for the accuracy of modeling as well as the accuracy of LIM simulation in the next step [6], [7].

1.3 Objectives

The objectives of the project are:

1. To analyze the behavior of PDN by Delaunay-Voronoi modeling and simulation using basic LIM and voltage-in-current LIM.
2. To compare the properties of basic of LIM and voltage-in-current LIM in term of their stability and accuracy.

1.4 Research Scope

The research is focused on the performance of PDN on power plane. Simulation of the power plane is carried using two approaches which are basic LIM and voltage-in-current formulated LIM. Comparison on the results obtained from the different methods is carried in the research to compare on the stability and accuracy of each approach. In term of power plane modeling, Delaunay Triangulation and Voronoi Tessellation method are used. Power plane is modeled into nodes and branches and the parasitic components at each branch and node are extracted and used in the simulation of the power plane. Based on the transient analysis and dc analysis of the PDN, the behavior of PDN is discussed in term of its meshing size and shape by relating those factors to the high-speed effects that observed from PDN simulation. The platform for the research to carry out is on Matlab.

1.5 Thesis Outline

There are five chapters in the report which are organized as following sequence:

Chapter 1 is about the research background including the motivation for carry the project and problem statements based on limitations of pervious work. The objectives and scopes of the research are also included in the chapter.

Chapter 2 covers the literature review on the fields related to the research. These included the background on PI design, power plane modeling techniques as well as the simulation of the power plane. In PDN modeling, lumped model approximation through rectangular meshing and Delaunay-Voronoi algorithm are presented while for PDN simulation, LIM algorithms including basic LIM, matrix-based LIM, ADE-LIM and voltage-in-current formulated LIM are discussed in detail in this chapter.

Chapter 3 describes on the methods that are used in the research in order to obtain the results. The research is carried using Matlab with Delaunay-Voronoi meshing algorithm for power plane modeling and voltage-in-current formulated LIM for power plane simulation. To carry the research, a pre-simulation using LIM on circuit example is carried first to familiarize with both basic LIM and voltage-in-current LIM equations and ensure the correctness of these equations. It then proceeds to a detailed discussion on the project flow which included the approach used in PDN modeling and followed by PDN simulation. In term of result analysis, transient response and dc response of the power

plane are discussed and by changing on the time step value, accuracy and stability of LIM algorithms used in the project are compared and discussed in detail.

Chapter 4 shows the results and discussion of the study. The PDN performance of the modeled power plane is discussed through the aspect of transmission line effects. Results from transient response and dc response are shown and the effect of meshing size and PDN shape on the responses are discussed. The different LIM algorithms used in simulation which are basic LIM and voltage-in-current LIM are compared and discussed in term of their accuracy and stability based on their simulated result on PDN model using different time step.

Finally, Chapter 5 concludes the research with some suggestions on possible improvements and future work to be done for the study.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

As introduced in previous chapter, the performance of PDN on an electronic device is the indicator of the PI of the device. Demand in lower voltage level, higher operation speed and smaller device size has increased the challenge and complexity in PI design. Therefore, this chapter will begin with the background of PI design which included transmission line effects of high speed interconnects to PI of a design and target impedance approach in PI design. Then, it will proceed to PDN modeling and simulation algorithms.

In this chapter, PDN modeling through lumped model approximation will be reviewed. Through such approximation, power plane can be modeled into circuitry model with nodes and branches with their respective impedance level. This included rectangular or square meshing approach and through Delaunay Triangulation and Voronoi Tessellation algorithm.

For PDN simulation, the topic is started with some background on PDN simulation and then centered to LIM algorithms. LIM is a fast transient simulation tool that shows strong advantage on its short simulation time especially when handling large

signal network. Through the research history, a few improved LIM have been purposed with the aim of improving the performance of basic LIM. In this chapter, LIM algorithms included basic LIM, matrix-based LIM, ADE-LIM and voltage-in-current formulated LIM will be analyzed.

2.2 PI Design

PI design was once receiving less concern in semiconductor industry compared to SI design as SI is the indicator on the quality of signal transmission between devices on IC and PCB. However, with the trend of lower power consumption, higher operating frequency and system miniaturization, the strategy on maintaining the SI of a design entered a bottleneck. In real, the problems that degraded the SI of the design was due to the ineffective power-ground planes. A good PDN is important to ensure the SPI of a product. Therefore, this rises the attention on researcher and designer in PI of the product.

When the operating voltage level is lowered, the noise on the power plane is getting obvious and eventually creating problems as components like transistors are receiving unclean power from the power plane. Since most of the components have their suitable functioning voltage range, noise effect may bring down the performance of the product in overall. Besides that, at high frequency application, the VRM of the power plane is facing difficulty to catch up with the clock speed. In order to minimize those problems, the use of capacitor as charge reservoir on the PDN was suggested as capacitor can maintain the current supply to the chip during switching of voltage level. After that, it was found that the parasitic behaviors of the PDN can be extracted from its impedance characteristics. Therefore, target impedance approach was then introduced for PI design

[2], [3]. This is an approach which ensures the PDN performance by having a target impedance value for the PDN to be designed.

Due to the relationship between PI and SI is not straightforward. For time saving, PI and SI of a product is usually design in a parallel way. Figure 2.1 shows a possible design flow in designing a product's SI and PI. A design is always started with determining the design specification, this included the timing and noise margin. It is followed by topology design then only branches to SI and PI design. The dashed part on the other hand consists of analysis on the design performance after SI and PI design flows have been completed. On the dashed part, power-signal coupling and RPD analysis is one of the test to be carried in order to make sure the SI and PI design of the product perform well under such conditions. Same goes to noise analysis as all these problems may lead to transmission line effects especially for high-speed application [2].

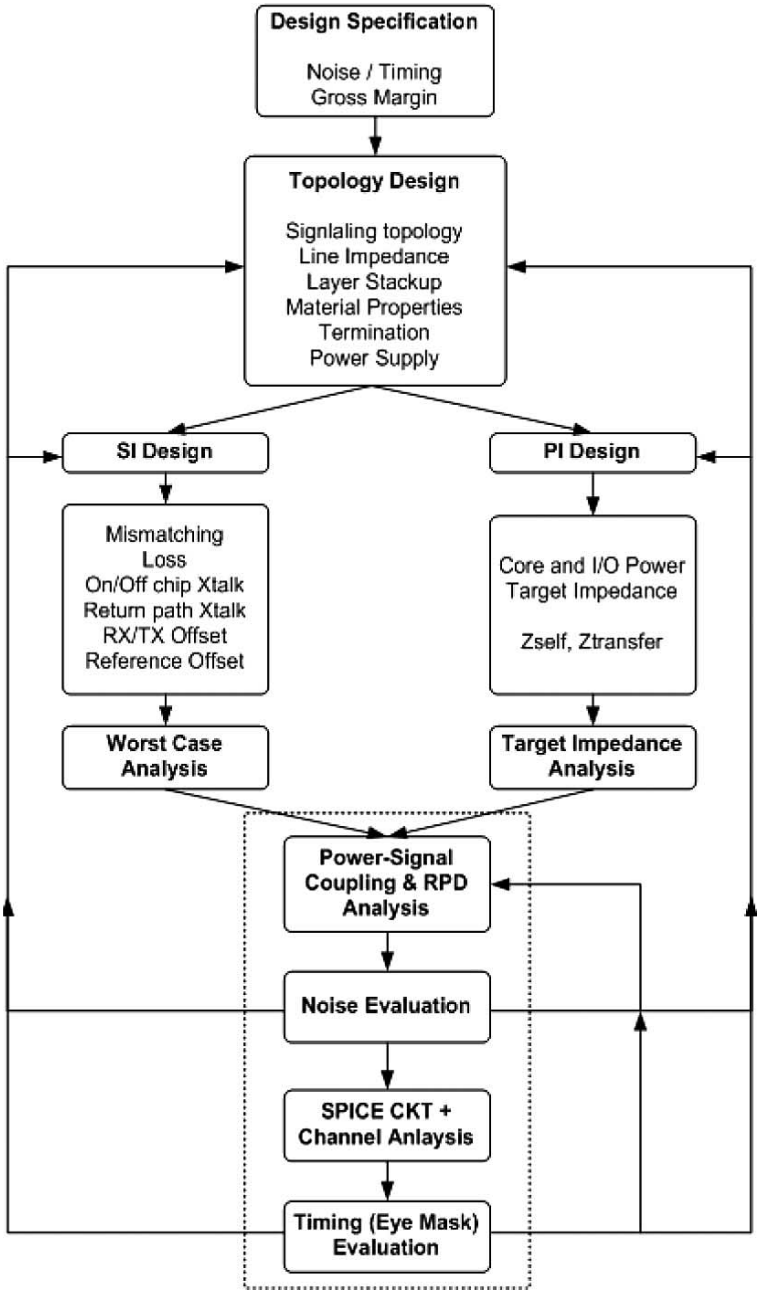

Figure 2.1: SPI design flow [2]

2.2.1 High-Speed Interconnect Effects

Since there is a trend on going towards high-speed application. Therefore, study of device behaviors under lower frequency is no longer enough for semiconductor product nowadays. High-speed application may lead to transmission line effects like propagation delay, attenuation, signal reflection and ringing and crosstalk [1]. All these phenomena

are the challenges for PDN design as they affect the power signal transmission and hence degrade the quality of power received by the components on the chip.

Signals take time to travel from one location to another, such traveling causes a finite delay between the signal at the front point and the end point of the travel path. The longer the distance, the signal will encounter a greater propagation delay. Propagation delay during rising and falling edge of the signal cycle brings down the performance especially for devices that function under precise time.

Attenuation is another effect due to ohmic or conductance loss in the PDN. Great loss in voltage level will alter the voltage level to be received by components like digital device and hence yield incorrect output. Therefore, one of the consideration on PDN design is on the impedance value in order to reduce attenuation on transmission line.

When signal is required to travel through different mediums or different layers on the PCB, discontinuities exist. The mismatch in impedance values creates severe signal distortion like reflection and ringing on the PDN. Overshoot, undershoot and ringing of signal during transmission creates plenty of uncertainties on signal propagation. Again, the impedance level of the entire design has to be considered to minimize the occurring of such unwanted effect.

System miniaturization makes highly dense and closely packed IC and PCB. Interference of electromagnetic field of wires in the PDN during signal transmission

causes the crosstalk phenomena. Crosstalk in turn generates unwanted noise in those electromagnetic coupled wires and it becomes a great issue when such coupled wires increased.

2.2.2 Target Impedance Approach

From previous discuss on transmission effects, it can be observed that impedance of the PDN influences the high-speed effects and hence the overall performance of the PDN. In conjunction with that, target impedance approach was introduced in 1990s. It is a PDN design methodology that design PDN according to the required impedance level for the PDN components like VRMs, capacitors and chips. This makes the design of each component can be carried out individually as their target impedance can be in different value [2].

The concept of target impedance is originated from Ohm's Law. From basic Ohm's Law:

$$V = IR \tag{2.1}$$

where *V* is the voltage across a component, I is the current flowing through the component and *R* is the resistance of the component, target impedance looking from the power supply of the transistor on the PDN to the VRM is given by:

$$Z_T = \frac{\Delta V}{I} \tag{2.2}$$

with Z_T is the target impedance, ΔV is the maximum allowable voltage ripple according to the transistor architecture and I is the current drawn by the transistor [3].

Since power-ground plane impedance consists of both resistive, capacitive and inductive components, the overall impedance of the PDN changes with the operation frequency. With target impedance, the design PDN will have impedance never exist the target impedance over the operating bandwidth. With such controlled impedance value, the PDN performance can be maintained to certain desire level as the parasitic behaviors of the PDN is associated with the impedance characteristics [3].

2.3 PDN Modeling

The PDN of an IC or PCB is basically the power plane of the design. In order to analyze on the performance of PDN, modeling of PDN is a must. One of the approach in PDN modeling is through lumped model approximation. From a power-ground planes with known material (known permittivity, permeability, conductivity and etc.) and size, power-plane can be approximated into circuitry of elements like resistance, inductance, capacitance and conductance. To carry out modeling, power-plane is separated into sections of rectangular [6] or triangular meshes [7] and each section is then modeled into circuitry through lumped model approximation. Power plane in lumped model is ready for simulation through tools like SPICE and LIM to analyze on its characteristics.

2.3.1 Rectangular/Square Meshing Algorithm

This approach provides modeling of PDN in rectangular cells with parameters w, l, and h that represent the width, length and thickness of the power plane respectively and s as the separation between planes as shown in Figure 2.2.

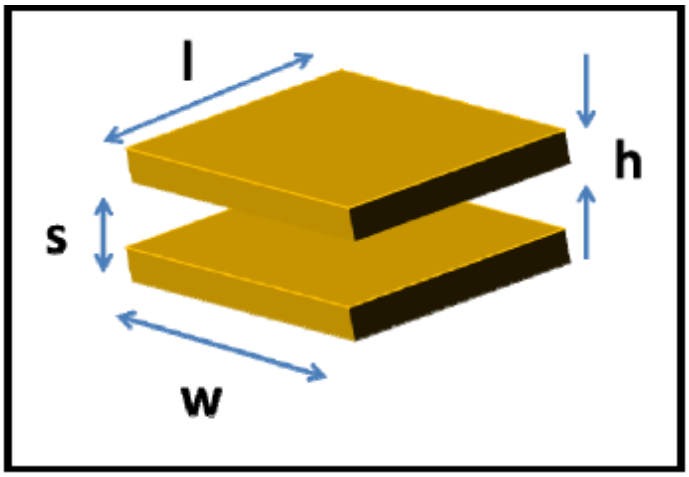

Figure 2.2: Parameters of a unit rectangular cell [6]

After the separation of power-ground planes into rectangular units, each unit is then computed for its capacitive (*C*), conductive (*G*), resistive (*R*) and inductive (*L*) elements through the following equations:

$$R = 2\frac{\rho l}{wh} \tag{2.3}$$

$$L = 32s\frac{l}{w} \tag{2.4}$$

$$C = \varepsilon_o \varepsilon_r \frac{lw}{s} \tag{2.5}$$

$$G = wC\tan(\delta) \tag{2.6}$$

where ρ is the electrical resistivity, ε_o is the permittivity free space, ε_r is the relative permittivity of the dielectric and $\tan(\delta)$ is the dielectric loss tangent. Each single lumped parasitic obtained from equation (2.3) to (2.6) for a unit cell are grouped together to form circuitry that consists of those four parasitic elements.

The next step is to combine all the rectangular unit to a circuit model. This can be done in merged or distributed way. Figure 2.3 shows the equivalent circuit model in merged approach. Through merged approach, power and ground planes are considered as a single plane and therefore it counts double for series resistance and inductance while quarter in value for parallel capacitance and conductance [6]. Distributed approach on the other hand consider power plane and ground plane separately.

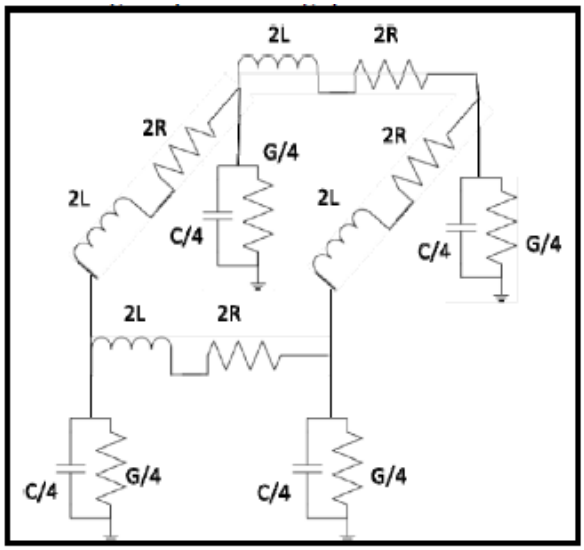

Figure 2.3: Merged equivalent circuitry model [6]

2.3.2 Delaunay Triangulation and Voronoi Tessellation Algorithm

Delaunay Triangulation and Voronoi Tessellation is another of the algorithm that can be applied on power-ground planes modeling [7]. It is somehow considered as a better approach compared to rectangular meshing as irregular shaped PDN is getting popular in PDN design for space saving purpose. Rectangular meshing that suffers from staircase approximation is not suitable to apply on arbitrary shaped PDN. In order to improve the modeling accuracy, the idea of triangular meshing comes into mind.

On a power plane, Delaunay Triangulation is employed first to separate the power plane into triangular meshes. With the power plane in triangular meshes form, a Voronoi tessellation is formed at each node by connecting the circumcenters of all the triangular meshes that surround the respective nodes. Figure 2.4 shows a rectangular power plane with two sources ports, port a and port b while Figure 2.5 shows the same power plane which has been modeled into Delaunay triangles and Voronoi tessellations. In Figure 2.5 as well, the virtual ports are playing the role as nodes of the equivalent PDN circuitry while the connection between nodes are branches that forming the current flow path in the PDN.

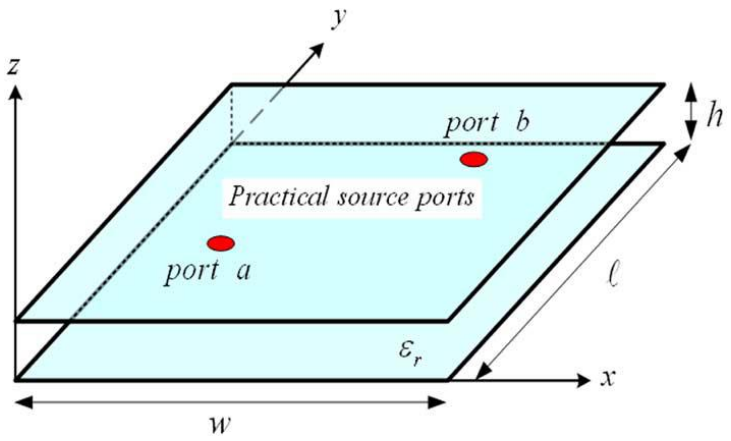

Figure 2.4: Power-ground planes for modeling [7]

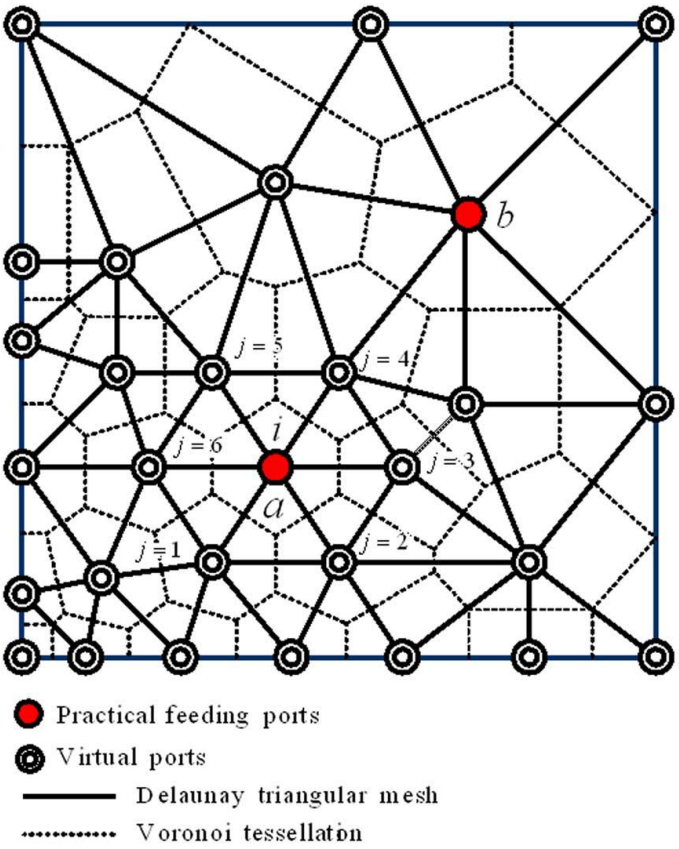

Figure 2.5: Modeling of power plane with Delaunay-Voronoi approach [7]

Power plane showing in Figure 2.5 can then proceed to computation of parasitic elements that exist on each branch and between each node with the ground. Figure 2.6 furthers enlarges Figure 2.5 at port a to provide a better view on the parameters that require to be taken into consideration during this impedance calculation step [7]. The equation in order to compute for the branch inductance, L_{ij} and the node capacitance, C_i are given by:

$$C_i = \varepsilon \frac{A_i}{h} \tag{2.7}$$

$$L_{ij} = \frac{\mu h d_{ij}}{l_{ij}} \tag{2.8}$$

where

ε = the permittivity of the dielectric medium,

A_i = the area of Voronoi tessellation surround the node,

h = the separation between the power and ground planes,

μ = the permeability of the power plane,

d_{ij} = the length between the branch, and

l_{ij} = the length of the Voronoi tessellation boundary exists between the two nodes which perpendicular to d_{ij}.

Another point to be concerned in the equation (2.7) and (2.8) is that the area, A_i and length, d_{ij} calculation may be differ according to the target port, whether it is a node or a vertical interconnect access (via). A more accurate formula for A_i and d_{ij} will be used in the calculation will be

$$A_i = \begin{cases} A_i' & for\ no\ via\ hole \\ A_i' - A_{via} & for\ existing\ via\ hole \end{cases} \tag{2.9}$$

$$d_{ij} = \begin{cases} d_{ij}' & for\ no\ via\ hole \\ d_{ij}' - r_{via} & for\ existing\ via\ hole \end{cases} \tag{2.10}$$

Same for the branch inductance, the existence of via at a particular node will influence the inductances that exist between via and the nodes linked to the via. Therefore, for such situation, another inductance formula will be used, which is

$$L_{ij} = \frac{\mu h}{\theta_{ij}} \ln\left(\frac{d_{ij}}{r}\right) \tag{2.11}$$

where θ_{ij} is the angle between two lines that connecting via and circumcenter and r is the radius of the via. After the computation on the inductance and capacitance for the power plane, the equivalent circuit will be like Figure 2.7 which shows the equivalent circuits at port a with inductance and capacitance extracted.

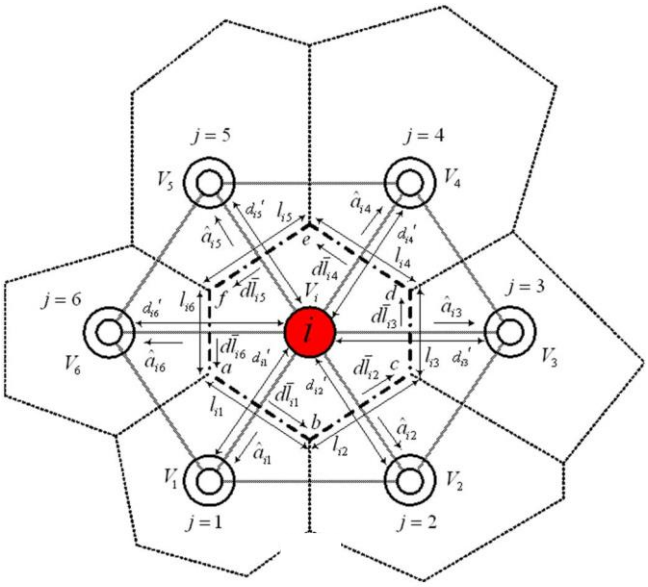

Figure 2.6: Delaunay triangles and Voronoi tessellation at port a [7]

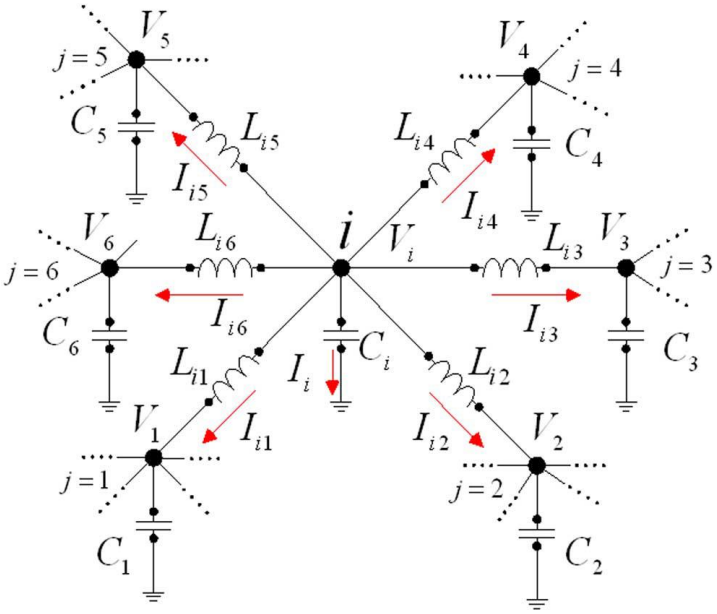

Figure 2.7: Equivalent circuit at port a [7]

The last part on the modeling will be the extraction of branch resistance and dielectric medium conductance. The formulae in order to compute these circuit components are:

$$G_i = \frac{\sigma_d}{h} A_i \tag{2.12}$$

$$R_{ij} = \frac{1}{\sigma b} \frac{d_{ij}}{l_{ij}} \tag{2.13}$$

with $b = \begin{cases} t, & for\ t < \delta_c \\ \delta_c, & for\ t > \delta_c \end{cases}$, where σ_d is the conductivity of the dielectric medium, σ is the conductivity of the power plane, t is the thickness and δ_c is the skin depth of the power plane. After the modeling on the resistive elements of the power-ground plane, the PDN of the IC or PCB in term of circuit components can be formed out and proceed with the simulation of PDN using simulation tools like SPICE and LIM.

2.4 PDN Simulation

For PDN simulations, again there are many available tools that able to process on modeled PDN and acquire the PDN characteristics through the simulation. The biggest issue faces by PDN simulation on pre-layout stage is on the PDN size or can be mentioned as the number of nodes. General purpose simulation tool like SPICE is inefficient enough for large signal analysis. Therefore, there is a need for simulator that provides fast response in PDN simulation [12]. Due to its fast transient simulation property, LIM algorithm able to stand out from other simulation tools.

Table 2.1 shows the comparison of run time between LIM and typical PDN simulation tool which is SPICE according to the number of nodes to be simulated [9], [11]. A clear comparison result is shown on the table where the SPICE simulator consuming a much greater time than LIM in handling PDN simulation. Moreover, the speed up of LIM to SPICE increases significantly when the number of nodes increases. Since, large signal is now a trend in semiconductor industry, LIM simulator is having an outstanding performance in term of time consuming. In term of accuracy as well, LIM algorithm also proved that its result is highly accurate and is comparable to other general simulation tools. Figure 2.8 shows the comparison between the transient analysis of using LIM and another common simulator, ADS for a same circuit model and there is a highly similarity between the results [13].

Furthermore, LIM is not only limited to fast transient analysis nowadays. Through LIM, frequency response of the PDN can be extracted by forming the transfer function of the PDN through S-parameter extraction and then compute with FFT [13] or Stochastic Collocation [14]. Through this new approach, LIM shows its potential in further development on this algorithm.

Table 2.1: Run time comparison between SPICE and LIM [9], [11]

Number of nodes	SPICE	LIM	Speedup
1,000	9	0.25	36
10,000	334	4	84
15,000	701	6	117
20,000	1224	9	136
25,000	1892	11	172
30,000	2935	13	225
40,000	4741	17	278
50,000	7358	21	350

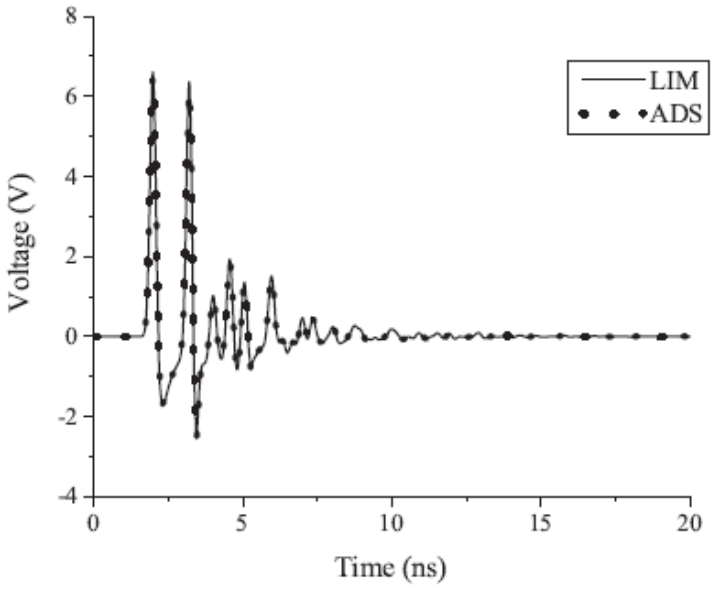

Figure 2.8: Comparison of transient analysis through ADS and LIM [13]

2.4.1 Basic LIM

Basic LIM is the fundamental LIM algorithm that purposed to the commercial. In order to simulate a circuit with LIM, the circuit must fulfill the topology of LIM [9], which are:

1. Each branch must consists an inductance.
2. Each node must consists a capacitive pathway to the ground.

Figure 2.9 shows a circuit model that fulfilled the LIM topology [9], however there may be situation that some nodes or branches do not consist of its capacitive and inductive component. To overcome the problem, an approximation is carried by adding a small value of capacitance or inductance to the respective node or branch that missing such component. Such approximation may cause small deviation on the simulation result but the effect is insignificant and can be neglected.

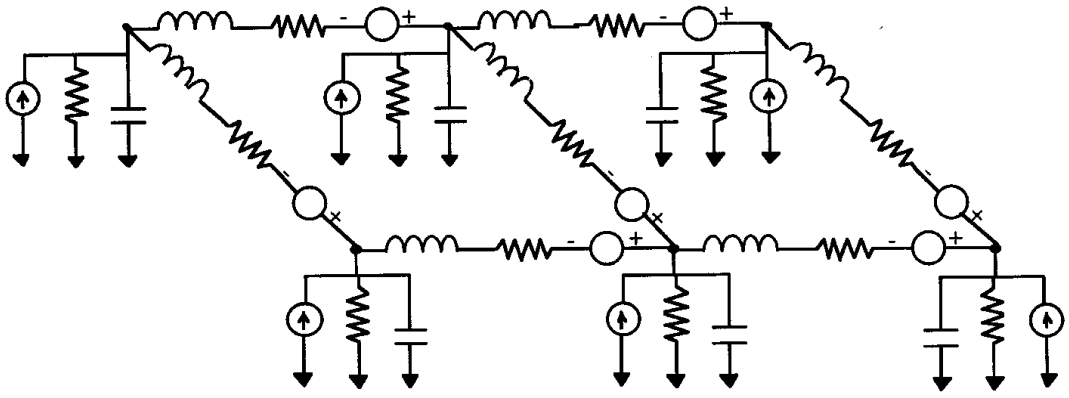

Figure 2.9: Circuit model which fulfilled LIM topology [9]