EFFICIENCY COMPARISON OF DIRECT DC-AC POWER CONVERSION SYSTEM AND CONVENTIONAL POWER CONVERSION SYSTEMS

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by

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LIST OF ABBREVIATIONS

MML	Modular Multilevel
DC	Direct Current
AC	Alternating Current
PWM	Pulse Width Modulation
PQ	Real Power-Reactive Power
PI	Proportional-Integral
DQ	Direct-Quadrature
BESS	Battery Energy-Storage System
PCS	Power Conversion System
TCM	Triangular Current Mode
EMI	Electromagnetic Interference
HVDC	High Voltage Direct Current
OPF	Optimal Power Flow
IGBT	Insulated-Gate Bipolar Transistor
NPC	Neutral-Point Clamped
PSPWM	Phase Shifted Carrier Pulse Width Modulation
IPDPWM	In Phase Disposition Level Shifted Pulse Width Modulation
PODPWM	Phase Opposition Disposition Level Shifted Pulse Width Modulation

LIST OF SYMBOLS

V_{CE}	Collector-Emitter Voltage
V_{CESat}	Collector-Emitter Saturation Voltage
I_C	Collector Current
I_{avg}	Average Current
$I_{avg,SM}$	Submodule Average Current
I_{rms}	Root Mean Square Current
R_{on}	On Resistance
P_{cond}	Conduction Loss
$P_{cond,SM}$	Submodule Conduction Loss
N_{cond}	Number of Conducing Switches
$E_{tot,fixed}$	Fixed Total Energy
$E_{tot,var}$	Variable Total Energy
P_{SW}	Switching Loss
$P_{SW,SM}$	Submodule Switching Loss
f_{SM}	Submodule Frequency
k	Linear fitting coefficients of IGBT and diode conduction characteristics
λ	Curve fitting coefficients of IGBT and diode devices
D	Duty Cycle

α	Shifting Angle
wt	Thetha
E_{off}	Turn-off Energy
E_{on}	Turn-on Energy
V_d	Diode Voltage
I_F	Forward Current
E_{rr}	Reverse Recovery Energy
Q_{rr}	Reverse Recovery Charge
I_{rr}	Reverse Recovery Current
t_{rr}	Reverse Recovery Time
P_{cond_Q}	IGBT Conduction Loss
P_{cond_D}	Diode Conduction Loss
P_{sw_Q}	IGBT Switching Loss
P_{sw_D}	Diode Switching Loss
T_j	Junction Temperature
$P_{sw\_Q\_on}$	Turn-on IGBT Switching Loss
$P_{sw\_Q\_off}$	Turn-off IGBT Switching Loss
V_{CC}	DC Bus Voltage
V_R	Reverse Blocking Voltage
P_{sw_off}	Diode Turn-off Loss

PERBANDINGAN KECEKAPAN SISTEM PENUKARAN KUASA DC-AC LANGSUNG DAN SISTEM PENUKARAN KUASA KONVENSIONAL

ABSTRAK

Populariti penyongsang bertingkat semakin berkembang terutamanya dalam aplikasi kuasa sederhana hingga tinggi. Hari ini, penyongsang DC-AC langsung seperti konfigurasi lata titi-H dan modular bertingkat (MML) titi separuh mendapat permintaan yang tinggi disebabkan kelebihan-kelebihan yang dimiliki berbanding konfigurasi konvensional seperti penyongsang apitan titik neutral dan kapasitor terbang. Fokus kertas kajian ini adalah pada perbandingan tahap kecekapan antara konfigurasi penyongsang DC-AC langsung dan penyongsang konvensional yang telah dinyatakan berdasarkan aplikasi sambungan grid. Ianya untuk memperolehi pengetahuan jelas tentang prestasi topologi-topologi yang dikaji. Penilaian kecekapan dilakukan sepenuhnya menggunakan pakej perisian simulasi PSIM. Untuk setiap topologi penyongsang, kuasa keluaran, voltan pautan DC, konfigurasi komponen semikonduktor dan kaedah penghasilan modulasi lebar nadi (PWM) telah dimalarkan bagi perbandingan yang adil. Dalam pengawalan kuasa, kawalan berasaskan kuadratur langsung (DQ) melalui kawalan kamiran berkadar (PI) bagi kuasa sebenar-kuasa reaktif (PQ) telah digunakan pada setiap topolgi yang dipilih. Bagi kaedah PWM pula, teknik anjakan tahap dalam fasa (IPDPWM) digunakan atas kemampuan penghasilan prestasi hormonik yang baik dengan komponen yang minima. Menerusi simulasi, penyongsang DC-AC langsung didapati mempunyai kecekapan yang lebih baik jika dibandingkan dengan penyongsang konvensional di mana kecekapan minimanya ialah 98.3 % dan mampu mencapai sehingga 99.1 %. Sebaliknya, kecekapan penyongsang DC-AC konvensional adalah pada julat 98.01 % ke 99.0 %.

EFFICIENCY COMPARISON OF DIRECT DC-AC POWER CONVERSION SYSTEM AND CONVENTIONAL POWER CONVERSION SYSTEMS

ABSTRACT

Multilevel inverters are gaining popularity especially in medium to high power applications. Today, direct DC-AC inverters with the like of cascaded H-Bridge and modular multilevel (MML) Half-Bridge configuration are becoming much more accepted due to their vast advantages compared to older conventional inverter configurations such as neutral-point clamped and flying-capacitor inverter. This study focussed on efficiency comparison between these direct DC-AC inverter and conventional inverter topologies based on grid link application. The purpose is to get a clear overview of the performance of tested inverter topologies. The efficiency evaluation was fully performed by using PSIM simulation software package. For every selected inverter topology, the output power, DC link voltage, semiconductor devices configurations and pulse width modulation (PWM) method were kept constant for a fair comparison between them. In controlling the power, real power-reactive power (PQ), proportional-integral (PI) based direct-quadrature (DQ) control scheme was implemented in all selected topologies. As for the PWM method, In Phase Disposition Level Shifted PWM (IPDPWM) was used since it produces decent output harmonic performance with minimum components. From the simulations, it was observed that direct DC-AC inverters have better efficiency performance in overall compared to conventional DC-AC inverters where their minimum efficiencies were around 98.3 % and able to reached up to 99.1 %. On the other hand, conventional DC-AC inverters' efficiencies ranged from 98.1 % to 99.0 %.

CHAPTER 1

INTRODUCTION

1.1 Research Background

Today, the increasing demand for renewable energy resources has been the reason for the increasing importance of grid-linked energy storage in an effort to create a more sustainable power grid system. Renewable energy resources will be crucial in the future because of the demand for efficient energy sources in term of its ready availability in a wide range of geographic areas. Energy storage has the ability to deliver power quickly to service areas. One of the most common energy storage technology is by using batteries because of its cost-effectiveness and its readiness for large-scale energy storage requirement.

Interfacing energy storage to the grid will require hardware components which are a power conversion system (PCS) and a network of energy storage units such as battery. Throughout this project, three-phase inverter will be studied for all topologies. When choosing an inverter topology, the most important feature is reliability which includes the analysis of harmonic content as well as the efficiency [1]. Determining the most efficient type of inverter is very crucial in an effort to build a more cost friendly system. Thus, it is one of the project's motivation.

For the efficiency study on PCS, there are two main sources of losses which bring the most impact to a system's efficiency. These losses are the conduction losses and the switching losses. Electrical energy that flows from the energy storage systems into the grid system depends on the limitation of the storage systems and efficiency of the inverter.

Utilization of the topologies of a grid inverter depends on the type of such renewable energy source [2]. Multilevel inverters are suitable for medium to high voltage and power application because of less harmonic spectrum output voltage that results into a better synchronization [3]. Besides, multilevel inverters are preferred over the conventional two-level inverters because of the limited switching speed and voltage-blocking capability of the semiconductor devices [4].

IGBT is commonly used for grid-linked PCS because of its capability of handling higher current rating, voltage and frequency. However, at a high switching frequency, switching losses will as well increase and will become more dominant in the overall losses of a system. This might reduce the efficiency of a PCS system and this condition is undesirable. So, it is best to make a power loss analysis comparison between several PCS topologies so that the best system can be identified and implemented for a long-term profit.

There are several type of available PCS in energy storage system. Dividing into categories, there are single-stage DC-AC converter, multi-stage DC-DC-AC converter and direct DC-AC converter. By analysing types of converters from different category, a clear view of PCS efficiency performance can be obtained.

If a single DC-AC conversion stage is used, the voltage balance at all operating conditions is not possible. For instance, in the application of neutral-point clamped multilevel converter, it can be proved that when the number of DC link capacitors is greater than two and real power is delivered to the load, the energy drawn from the inner capacitor is greater than the energy drawn from the external ones [5]. So, to implement this topology, capacitor balancing need to be done by using additional components. However, this solution causes an increase in system cost and additional power losses.

High power density AC-DC and DC-AC converter systems typically employ Triangular Current Mode (TCM) modulation or conventional pulse width modulation (PWM). TCM is characterized by a wide variety of switching frequency over the mains period and ensures soft-switching in all operating points, but results in increased conduction and high-frequency losses due to the necessary large current ripple. In contrast, Pulse Width Modulation (PWM) with constant switching frequency features a lower RMS current and thus reduced conduction losses, but cannot achieve soft switching over the entire mains period and suffers from turn-on losses [6]. Thus, it is important to take into account about the suitability of modulation technique to be used in any PCS since it can bring about higher and undesirable losses.

1.2 Problem Statement

To date, there are still very few numbers of research done based on efficiency comparison between power conversion system (PCS) topology mainly in medium to high voltage systems on grid application. In other application such as motor, several studies have been done [7, 8]. Furthermore, most of the studies focussed only on two to three type of PCS topologies. Besides, efficiency comparison of topologies between the same PCS categories has always been favourite. It will be best if the comparison includes topologies between categories. These categories include multi-stage and direct DC-AC converter.

Next, there are several different equations proposed by researchers to calculate both conduction and switching losses. Furthermore, there is no comparison made between type of proposed equations in term of accuracy. In order to obtain the most accurate result, the best mathematical model should be chosen. Two of the common methods are linear approximation and parabolic interpolation [9, 10].

There are several approaches that can be done in PCS efficiency study. However, every approach has their own limitation. For instance, one of the main challenge in fairly comparing the topologies is the utilization of the device with the smallest current rating that satisfies operation requirements [11]. This will be a problem if different components are used in different topologies in comparison. Other factors need to be fixed for fair comparison are rated power, value of DC link voltage and pulse width modulation (PWM) scheme used [7].

Lastly, analysis of efficiency can be done in several ways such as calculation, simulation or experiment. Several factors need to be taken into account when choosing the type of approach to be used such as cost, time constraint, and accuracy [4].

1.3 Objectives of Research

The objectives of this research are as follows:

1. To fairly compare the efficiency of four power conversion system (PCS) topologies which are neutral-point clamped (NPC) and flying-capacitor from conventional DC-AC category as well as modular multilevel (MML) Half-Bridge and cascaded H-Bridge from from direct DC-AC category on grid-link application.
2. To analyse both conduction and switching losses of switching devices in selected PCS topologies using parabolic interpolation mathematical model.
3. To use computer's simulation software, PSIM to retrieve accurate analysis results at a minimal time and cost.

1.4 Scope of Research

The scope of this research covers the simulation of losses and comparison of several grid-linked power conversion system (PCS) topologies as described in the objective. Comparisons were aimed mainly between direct DC-AC and conventional DC-AC converter configurations. The whole research was performed fully through software simulation without any hardware parts involved. PSIM software was entirely used for losses simulation and calculation with the aid of several other software to obtain the most accurate results. Conduction and switching losses of semiconductor devices in PCS were simulated at different test conditions for the purpose of efficiency comparison. In this research, real power-reactive power (PQ), proportional-integral (PI) based direct-quadrature (DQ) control scheme was implemented in all PCS topologies for the purpose of simulating three-phase grid-linked systems. There are also some important parameters that must be kept constant across all PCS topologies for fair loss comparison. They are the characteristics of semiconductor devices, pulse width modulation (PWM) technique, output power and DC link voltage. Finally, analyses were made on compared efficiencies in determining the most advantageous topology.

1.5 Project Contribution

With the advancing popularity and attention towards clean and sustainable energy, distributed energy systems (DE) are as well gaining popularity and their demand is increasing. Examples of DE system are renewable energy system and energy storage system. As mentioned earlier, power electronics such as multilevel inverter are an integral part of these energy systems to convert generated electricity into consumer usable and utility compatible forms. Thus, there is a need for utility companies to provide customers with the best service at a reasonable cost. So, efficiency study on multilevel inverters is

one of the ways that will help these utility companies to choose the best power conversion system (PCS) topology that suits their requirement. Efficiency is one of the aspects in determining a system's reliability where poor reliability has always been an issue in power electronics application [12]. Thus, it is clearer why efficiency study is important towards both stakeholder as well as the community because it can be a very useful measure to solve the reliability problem.

From efficiency study as well, a clear overview of how well a system able to perform can as well be obtained. So, continuous study and improvement can be done. This will aid in the advancement of DE systems especially renewable energy system in Malaysia since the country is currently moving towards increasing the capacity of renewable energy and reducing the dependency on non-renewable energy sources such as fossil fuel. It is well known that the usage of fossil fuels generally releases pollutants such as carbon dioxide to the environment. Carbon dioxide is one of the primary contributor to the global warming. Besides, power generation using fossil fuel also releases greenhouse gasses and toxic elements as a result of fossil fuel combustion. These emissions can cause serious health complications such as chronic asthma, low lung functioning, chronic bronchitis and cardiovascular diseases if they are not controlled.

Throughout the project, all systems are designed to be in compliance with Tenaga Nasional Berhad's (TNB) regulation. For instance, the grid voltage and frequency used were 240 V and 50 Hz respectively and the grid current was made sure to be within the range of 10 A to 100 A as stated in TNB's Electricity Supply Application handbook.

1.6 Thesis Outline

This thesis consists of five chapters. The first chapter introduces the whole project in general and describes the importance of performing efficiency study on power conversion system (PCS) along with problem statements description and project's objectives.

Literature review is presented in the following chapter where reviews on previous works published by other researchers based on related topics are made. These reviews include the advantages and disadvantages of certain aspects of the researched topic and the way to optimize and minimize errors are reviewed and summarized.

Chapter 3 explains the methodology of the whole project in depth which includes the software used for simulation, the modelling technique of circuit elements, the parameters used for simulation and also the way to analyse losses. For each part of methodology, theories are included for better understanding on every process involved in this project.

In Chapter 4, results obtained throughout the project are presented. These results include simulation outputs, simulation analysis and results comparison. The efficiency of PCS topologies are compared and the results are analysed in this chapter. A summary on key results and findings is also presented.

Chapter 5 presents the conclusion of the whole project as well as several recommendations for future works on the researched topic.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In analysing the efficiency of a power conversion system (PCS), loss analysis mainly need to be done on switching devices. For instance, gating technique used in device turning on and off might give an impact on overall loss of a system. Several studies have already been conducted on this. Pulse width modulation (PWM) features lower conduction and winding losses due to the comparably small current ripple and thus lower RMS value of the inductor current. However, a hard turn-on of the high-side transistor over a wide range of the mains period results in high switching losses. On the contrary, operation using triangular current mode (TCM) modulation in turns cause large current ripple which significantly increases conduction and winding losses [6].

For grid application, in implementing PCS, multilevel inverter has been one of the most popular choice today because of its advantages. There are several studies conducted which support the claim. Multilevel converters have been recommended for high and medium level power applications for decades. They have received widespread attention because of their attractive features which consist of staircase waveform quality, small common-mode voltage, input current with low distortion and low switching frequency. In fact, due to their increasing number of levels, multilevel converters have the ability to synthesize the desired output voltage from several levels of DC voltage input source. Recent multilevel converter topologies have overcome the need for series switching when addressing lower switching loss and improved power quality [13].

Another supporting reason to support the previous claim is that multilevel converters are formed by the connection of individual semiconductors in different structures, enabling operation at higher voltages and currents than the rating of single devices [7]. These converters have been the scope of a tremendous number of researches due to their outstanding advantages such as low common-mode voltages, low dv/dt stresses, low propagated electromagnetic interference (EMI) emissions and high efficiency. As a result, multilevel converters have been employed in a wide variety of applications such as grid-linked inverters, active front-end rectifiers, HVDC, motor drives, and so on [14].

Besides the technique used to switch on and off devices, another factor such as load stress might as well affect the overall efficiency of a system. For instance, the multi-terminal onshore and offshore dc grids schemes are a reality for power transmission. The overall efficiency of the power transmission scheme has a relevant impact from the converter insight, whose efficiency, varies according to the load stress. Therefore, to properly introduce the converter losses into the optimal power flow (OPF) system studies, an accurate analytic calculation of the losses for a converter must be used [15].

2.2 Power Semiconductor Losses

2.2.1 Conduction Loss

Conduction loss occurs in all semiconductor devices when they are in full conduction period [16]. For a conducting device, the current in the device is the device's required current itself and the voltage at its terminals is basically the voltage drop due to the device. Conduction loss is in direct proportion to the duty cycle of the device [17].

For every inverter topology, conduction loss mostly occurs in switching device such as Insulated-Gate Bipolar Transistor (IGBT). In this paper, IGBT were entirely used

as the switching devices for all of the selected inverter topologies. In case of IGBT, the total dissipated power can be calculated by multiplying the on-state voltage, V_{CESat} with the on-state current, I_C. This on-state voltage is generally a function of switch's current and switch's gate voltage and most of the time they can be easily found in device's datasheet provided by the manufacturer [18].

With the Pulse Width Modulation (PWM) application, conduction loss will need to be multiplied by the duty cycle in order to obtain the average power dissipation in calculating conduction loss. The standard conduction loss can be calculated using Equation (2.1) where $V_{CE,sat}$ is the fixed voltage source. R_{on} is the on resistance. I_{avg} is the average current and I_{rms} is the rms current conducted by the device [19]. In a situation of using several submodules (SM), the whole Equation (2.1) should be multiplied by the number of switches conducting at a given time, N_{cond} [17]. The new formula for conduction loss will be as shown in Equation (2.2). However, this proposed model does not include diode loss equation.

$$P_{cond\_IGBT}=V_{CE,sat}I_{avg}+R_{on}I^2_{rms} \tag{2.1}$$

$$P_{cond\_IGBT,SM}=N_{cond}(V_{CE,sat}I_{avg,SM}+R_{on}I^2_{rms,SM}) \tag{2.2}$$

Linear conduction loss mathematical model can as well be obtained through linear approximation. The approximation is based on the fact that IGBT and diode devices normally work at their saturation region. So, the rated current flowing through IGBT, I_N and the on-state voltage drop V_{CE} nearly presents a linear relationship with the conducted current, I_C. The same goes to diode. Thus, the conduction loss of IGBT and diode are given as in Equation (2.3) and Equation (2.4) where I_F is the conducted current and V_F is the on-state voltage drop of a diode. The constants k_1 to k_4 are the linear curve fitting

coefficients of the IGBT and diode conduction characteristics which are related to the junction temperature [9].

$$P_{cond\_IGBT} = k_1 I_C^2 + k_2 I_c \quad (2.3)$$

$$P_{cond\_Diode} = k_3 I_F^2 + k_4 I_F \quad (2.4)$$

Another method to model the mathematical equation of IGBT and diode conduction loss is by implementing the parabolic interpolation method which fit the losses characteristic curves instead of assuming a linear approximation. With this, the relationship between the drain current, I_C and the conducting voltage, V_{CE} for IGBT as well as the drain current, I_F and conducting voltage, V_F in a diode will be used. Therefore, IGBT and diode conduction loss can be expressed as in Equation (2.5) and Equation (2.6) where D_Q and D_D represents the duty cycle of IGBT and diode respectively [10].

$$P_{cond\_IGBT} = V_{CE} I_C D_Q \quad (2.5)$$

$$P_{cond\_DIODE} = V_F I_F D_D \quad (2.6)$$

2.2.2 Switching Loss

Differ from conduction loss, switching loss occurs at the transition moment of a device from its conducting state into blocking state and vice versa. In other words, it is the loss occurring during the moment between turning on and turning off of a device. During the transition interval, both the current through and the voltage across the device are substantially larger than zero which leads to large instantaneous power loss [17]. This interval is characterized by a significant voltage across its terminals and a significant current through it. The energy dissipated in each transition needs to be multiplied by the frequency to obtain the switching loss [20].

The energy loss at each turn on and off of switching devices can be assumed to have a fixed, $E_{tot,\ fixed}$ and variable component, $E_{tot,\ var}$ [19]. Switching losses can now be calculated by using Equation (2.7) where f is the switching frequency and I_{avg} is the average current of the switching device. In case of several submodules, N_{SM} is the number of switches conducting at a given time, f_{SM} is the frequency of switches in the standard submodule and $I_{avg,SM}$ is the average current conducted by a submodule [19]. The new formula for switching loss will be as shown in Equation (2.2). However, this model does not include diode loss equation.

$$P_{sw\_IGBT}=f(E_{tot,fixed}+E_{tot,var}I_{avg}) \quad (2.7)$$

$$P_{sw\_IGBT,SM}=f_{SM}N_{SM}(E_{tot,fixed}+E_{tot,var}I_{avg,SM}) \quad (2.8)$$

The same as discussed in the conduction loss part, a linear approximation can be used to model mathematical equation for switching loss as well. A large amount of loss occurs in IGBT due to a large current that flows through the device at the moment of its turn-on and turn-off. As for diode, switching loss is produced from its reverse recovery characteristic during switching off process. The switching loss characteristics of IGBTs and diodes can be expressed as in Equation (2.8), Equation (2.9) and Equation (2.9) where I_F is the conducted current, I_C is device's conducted current and λ_1 to λ_9 are the curve fitting coefficients of IGBT and diode devices, which are related to the junction temperature [9].

$$P_{sw(on)\_IGBT} = \lambda_1 I_C^2 + \lambda_2 I_{C+} \lambda_3 \quad (2.8)$$

$$P_{sw(off)\_IGBT} = \lambda_4 I_C^2 + \lambda_5 I_{C+} \lambda_6 \quad (2.9)$$

$$P_{sw\_DIODE} = \lambda_7 I_F^2 + \lambda_8 I_{F+} \lambda_9 \quad (2.10)$$

An alternate mathematical model can as well be obtained by using parabolic interpolation method which takes into account the losses characteristic curves instead of assuming a linear approximation. This method is applied by using the relationship between the drain current I_C and IGBT turn-on energy consumption E_{on}/E_{off}. The switching losses of IGBT during turn-on and turn off are given as in Equation (2.11) and Equation (2.12) respectively while the switching loss of diode is given as in Equation (2.13) [10].

$$P_{sw(on)\_IGBT} = E_{on} \times f_{on} \tag{2.11}$$

$$P_{sw(off)\_IGBT} = E_{off} \times f_{off} \tag{2.12}$$

$$P_{sw\_DIODE} = E_{rr} \times f_{rr} \tag{2.13}$$

2.2.3 Efficiency Calculation

The efficiency calculation for any power conversion system (PCS) topology can be achieved by assuming that conduction and switching losses are the primary and major sources of losses. Then, one way to obtain the efficiency of an inverter topology is by choosing a fixed rated power, P_{rated} which should be chosen based on the rated average current of a system. Power injection method is discussed in section 2.5. In case of a modular multilevel converter with centralized energy storage system, the rated current is calculated at the minimum DC link voltage [19]. From the previously discussed losses calculation mathematical models, the total loss value of any inverter topology can be easily computed by summing up the losses value for every semiconductor devices. Thus, efficiency can be obtained from the fixed rated power value and the total loss value [21].

2.3 Power Conversion System (PCS) Topologies

Since voltage source inverter in a battery energy storage system is separated into a conventional DC-AC converter and direct DC-AC converter, two topologies from each of the group are chosen for efficiency comparison in this project. The chosen conventional DC-AC converter topologies are Neutral-Point Clamped (NPC) converter and Flying-Capacitor converter. On the other hand, Cascaded H-Bridge converter and Modular Multilevel (MML) Half-Bridge converter are chosen from the direct DC-AC converter category. DC link voltage will be made sure to be the same across all topology in order to obtain the same output which is crucial for fair efficiency comparison between them.

2.3.1 Neutral-Point Clamped (NPC) Converter

An NPC converter was derived from the modification of the old Two-Level converter topology. It requires twice the number of power semiconductor devices compared to the two-level topology with additional clamping diodes [22].

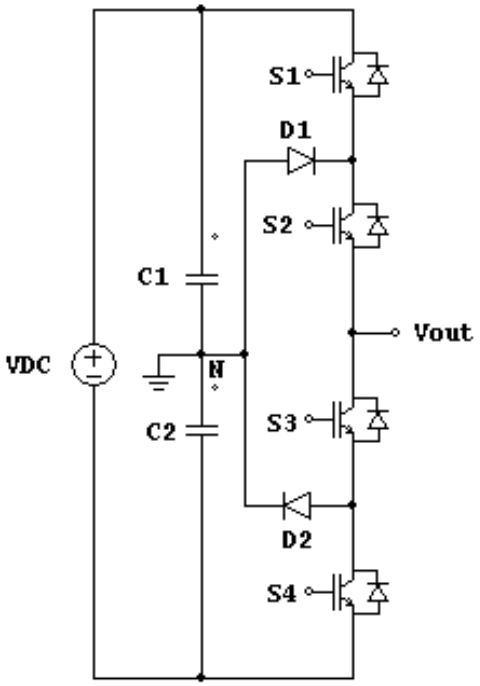

Figure 2.1: One-phase of three-level NPC converter.

Figure 2.1 shows one phase of a three-level NPC converter. The phase is capable of generating three output voltage levels which are $\frac{+V_{DC}}{2}$, 0 and $\frac{-V_{DC}}{2}$. The point N is the neutral point and diode D1 and D2 are called the clamping diodes which serve the purpose of generating 0 voltage level. A complete three-phase three-level NPC converter topology can be seen as in Figure 2.2.

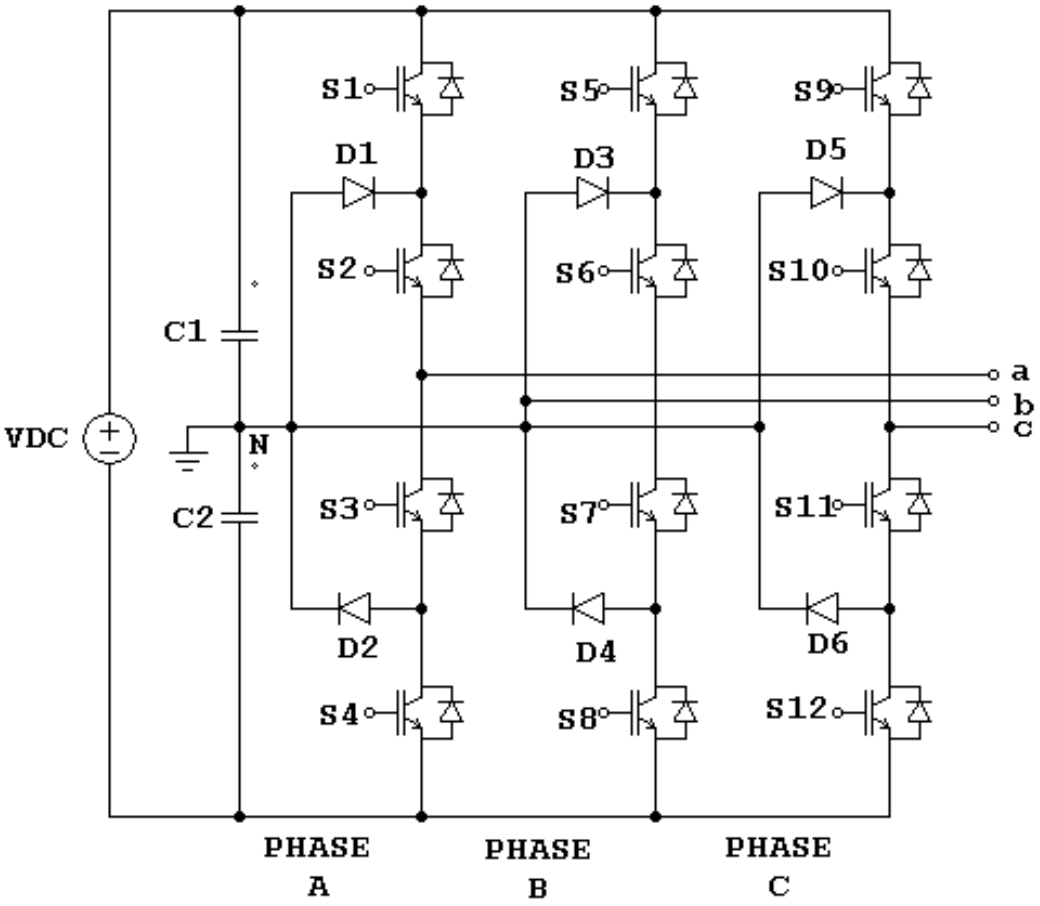

Figure 2.2: Three-phase three-level NPC converter.

The output of each phase to neutral voltage are the same as explained before, However, they are shifted by an angle of 120° for each corresponding phase. Take phase A as an example, S1 and S2 should be turned on for the positive half cycle while S3 and S4 should be on for the next half cycle. With this switching sequence, the phase current will flow into the neutral junction, N through the upper clamping diode if it is positive or

out of the junction through the lower clamping diode if it is negative [23]. The output obtained for different switching sequence of each phase is shown in Table 2.1.

Table 2.1: Switching combinations of three-level NPC converter per phase.

Switching States				Output Voltage
S1	S2	S3	S4	
1	1	0	0	$\frac{+V_{DC}}{2}$
0	1	1	0	0
0	0	1	1	$\frac{-V_{DC}}{2}$

Table 2.1 presents the switching combinations per phase. For a complete three-phase three-level NPC converter, the output line voltage will have five levels which are at ±100 % V_{DC}, ±50 % V_{DC} and 0 % V_{DC}. On the other hand, the output phase voltage will have nine levels which are at ±66 % V_{DC}, ±50 % V_{DC}, ±33 % V_{DC}, ±16.5 % V_{DC} and 0 % V_{DC} [23].

2.3.2 Flying-Capacitor Converter

The flying-capacitor topology is very much the same as the neutral-point clamped configuration which has been discussed earlier except that clamping diodes are absent and being replaced by clamping capacitors which served the purpose to hold voltage at the desired value [24]. In other words, the clamping capacitors are used to limit the voltage across an open switch in place of clamping diodes in NPC. Figure 2.3 shows one phase of a three-level flying capacitor converter.

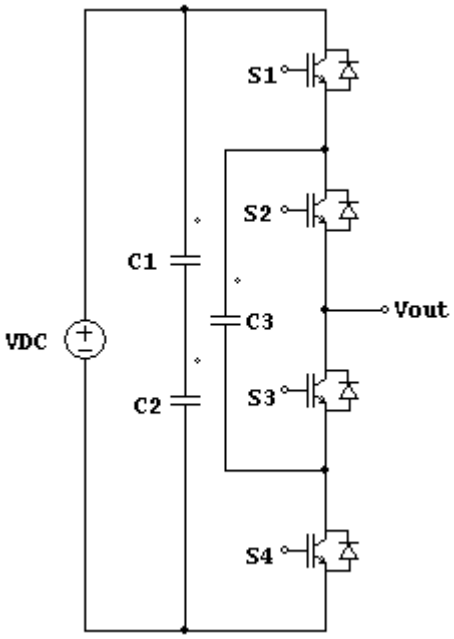

Figure 2.3: One-phase of three-level flying-capacitor converter.

Since the capacitor is not capable of blocking reverse voltage, the number of possible switching combinations also increased. The same as in NPC converter, flying-capacitor converter has three possible output voltage levels per phase which are $\frac{+V_{DC}}{2}$, 0 and $\frac{-V_{DC}}{2}$. However, unlike NPC, flying-capacitor has two possible switching combinations to achieve 0 voltage level [23].

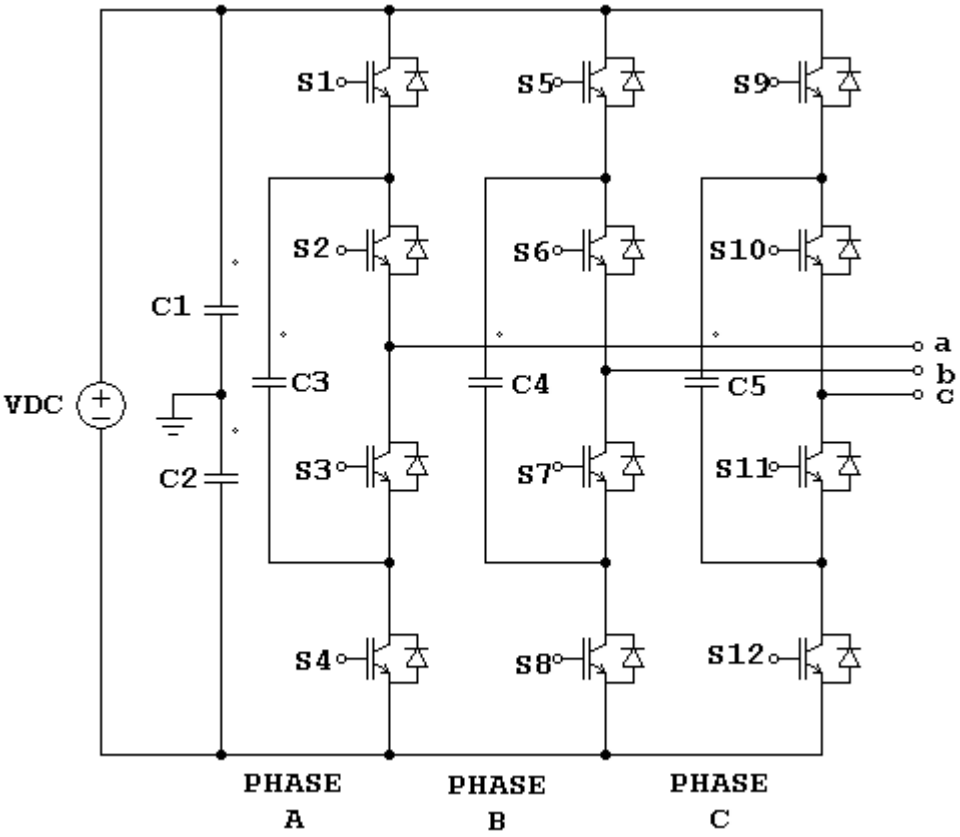

Figure 2.4: Three-phase three-level flying-capacitor converter.

A complete three-phase three-level flying-capacitor topology is shown in Figure 2.4. Take phase A as a reference. The inverter leg consists of two switching cells, S1 and S4 clamped by the DC link together with the clamping capacitor, C3 which work alternately forming the first switching cell, while S2 and S3 clamped by the same clamping capacitor work alternately to form the second switching cell [25]. This type of configuration has one significant advantage over NPC since it has switching redundancy within the phase which in turns balance the circuit [26]. Table 2.2 shows the output voltage and switch sequence for every switching state of a flying-capacitor three-level inverter.

Table 2.2: Switching combinations of three-level flying-capacitor converter per phase.

Switching States				Output Voltage
S1	S2	S3	S4	
1	1	0	0	$\frac{+V_{DC}}{2}$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	$\frac{-V_{DC}}{2}$

Table 2.2 presents the switching combinations per phase. For a complete three-phase three-level flying-capacitor converter, the output line voltage will have five levels which are at ±100 % V_{DC}, ±50 % V_{DC} and 0 % V_{DC}. On the other hand, the output phase voltage will three levels which are at ±50 % V_{DC} and 0 % V_{DC} [27].

2.3.3 Modular Multilevel (MML) Half-Bridge Converter

MML Half-Bridge is one of the earliest forms of the direct DC-AC converter topology. Figure 2.5 shows one leg of a three-level MML Half-Bridge converter and the Half-Bridge submodule respectively. In this configuration, the cells number in the upper arm are equal to the cells number in the lower arm and the number of submodule in both arms depends on the level of inverter [28].

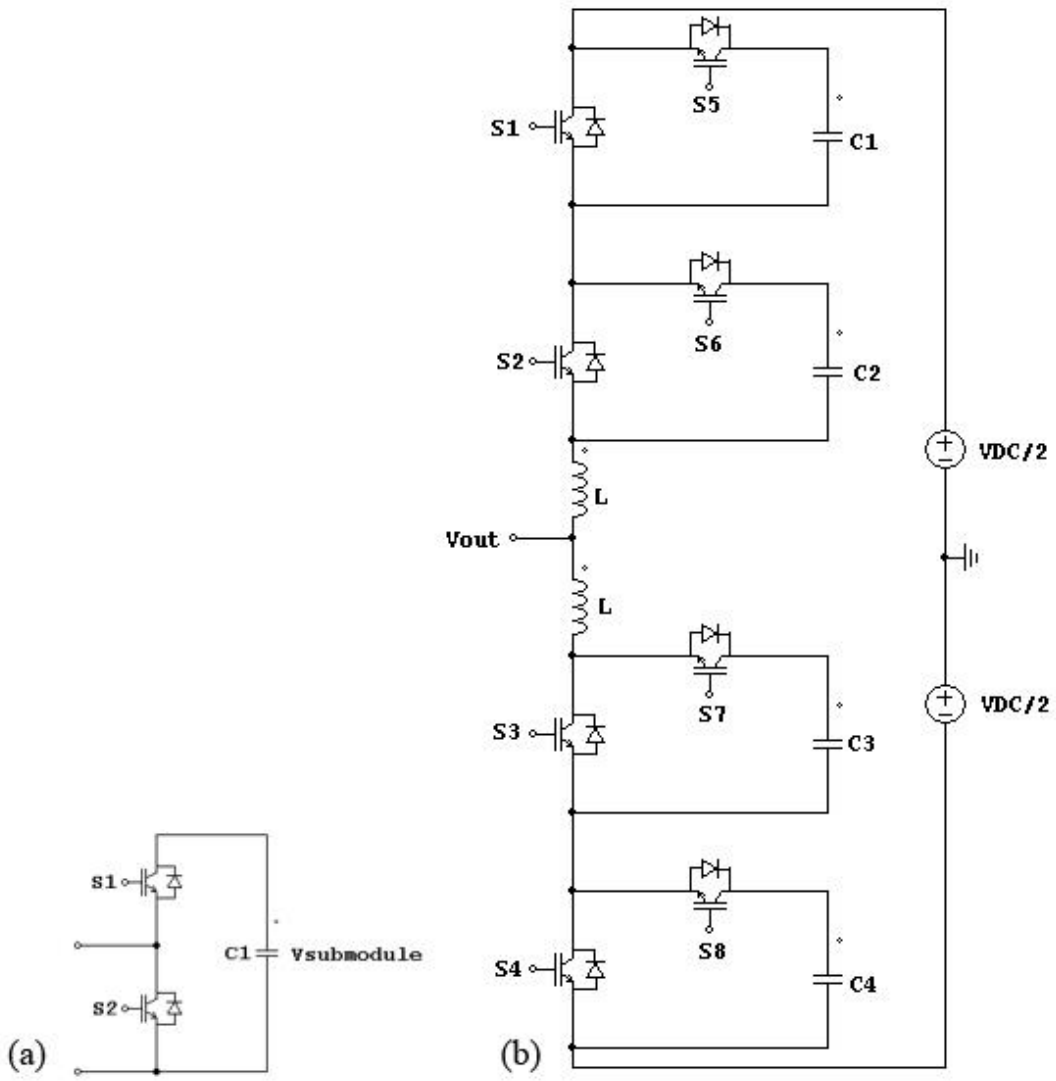

Figure 2.5: Half-bridge submodule (a) and one-phase of three-level MML Half-bridge converter (b).

Each submodule is capable of generating two voltage levels in accordance with the switching combinations of the complementary switch pairs. From Figure 2.5, if S1 is turned-on the moment S2 is off, the submodule will be inserted into the circuit, thus, the voltage between the submodule will be equal to V_{DC}. On the other hand, if S1 is turned-off the moment S2 is on, the voltage between the submodule terminal will be zero since the submodule is bypassed [19]. Figure 2.6 shows the complete three-phase three-level topology of an MML Half-Bridge Converter.

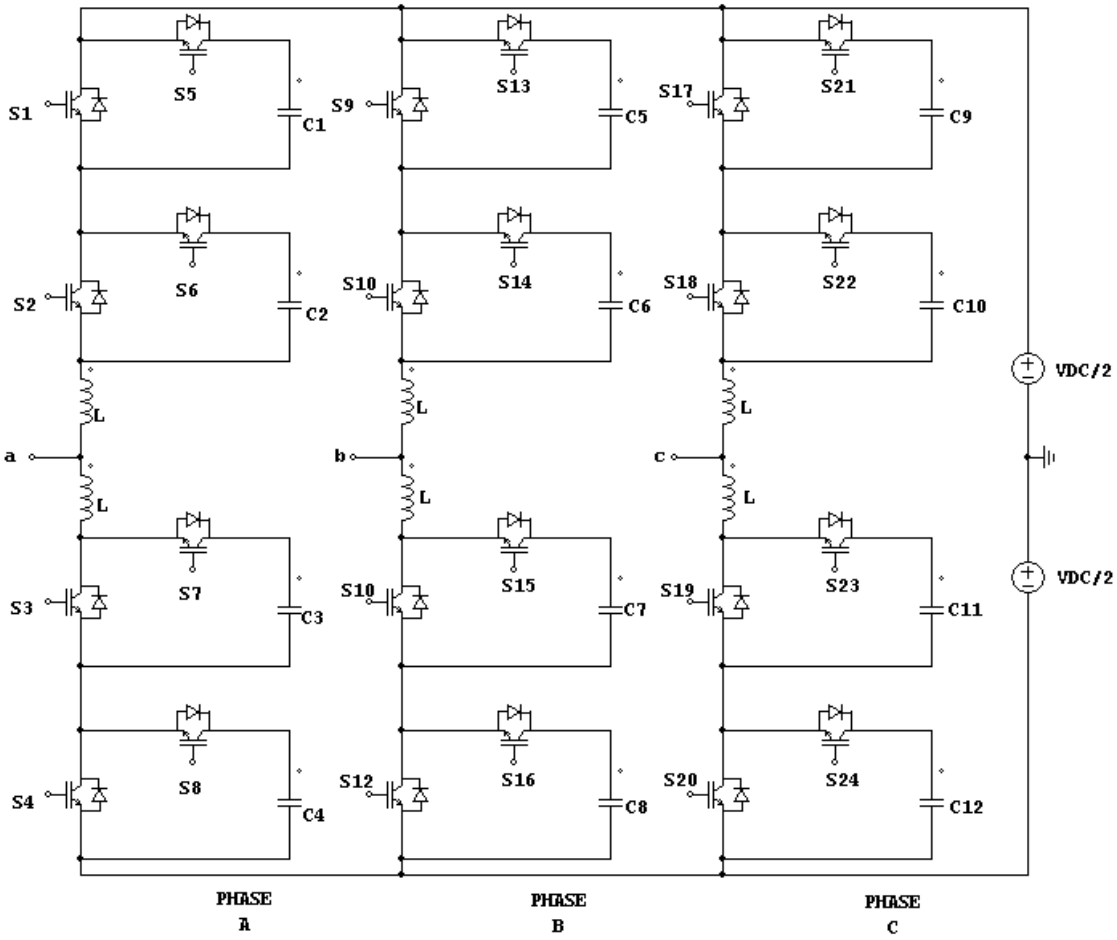

Figure 2.6: Three-phase three-level MML Half-bridge converter.

Each phase leg is able to produce three voltage levels which are $\frac{+V_{DC}}{2}$, 0 and $\frac{-V_{DC}}{2}$. However, there are several redundancies in switching combinations to obtain the 0 voltage level. For the three-level configuration, the submodule capacitor voltage should be $\frac{V_{DC}}{2}$ [29]. Table 2.3 shows all the switching combinations corresponding to output voltages of a three-level MML Half-Bridge converter.

Table 2.3: Switching combinations of three-level MML Half-bridge converter per phase.

Switching States								Output Voltage
S1	S2	S3	S4	S5	S6	S7	S8	
1	1	0	0	0	0	1	1	$\frac{+V_{DC}}{2}$
1	0	1	0	0	1	0	1	0
0	1	1	0	1	0	0	1	0
0	1	0	1	1	0	1	0	0
1	0	0	1	0	1	1	0	0
0	0	1	1	1	1	0	0	$\frac{-V_{DC}}{2}$

Table 2.3 provides the switching combinations per phase. For a complete three-phase three-level MML Half-Bridge converter, the output line voltage will have five levels which are at ±100 % V_{DC}, ±50 % V_{DC} and 0 % V_{DC}. On the other hand, the output phase voltage will have nine levels which are at ±66 % V_{DC}, ±50 % V_{DC}, ±33 % V_{DC}, ±16.5 % V_{DC} and 0 % V_{DC} [30].

2.3.4 Cascaded H-Bridge Converter

Cascaded H-Bridge is another type of direct DC-AC converter and is one of the most widely used configurations today. In this configuration, several isolated DC voltage sources will be needed and the number of output voltage levels will depend directly on the number of DC source. Cascaded H-bridge is as well characterized by high efficiency and high modularity [31]. Figure 2.7 shows an H-bridge circuit which is the basic module to build a cascaded H-bridge converter.

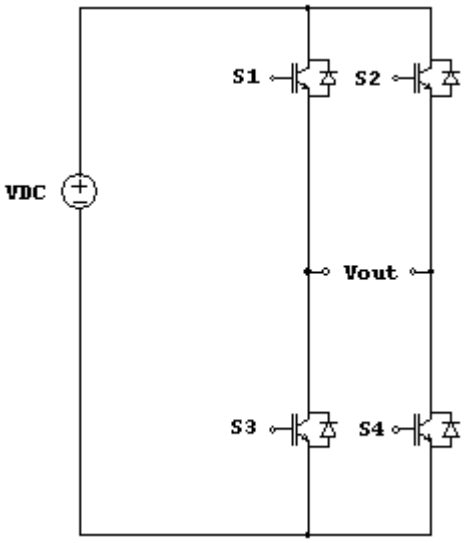

Figure 2.7: One-phase of three-level cascaded H-bridge converter.

Fundamentally, each H-bridge module is capable of generating three voltage levels which are $+V_{DC}$, 0 and $-V_{DC}$. The voltage level $+V_{DC}$ can be obtained on the output by turning on S1 and S4 while turning off S2 and S3. Inversely, when S1 and S4 are turned-off while S2 and S3 are turned-on, $-V_{DC}$ will be obtained at the output. A 0 level will appear at the output whenever the top two switches or bottom two switches are turned-on simultaneously.

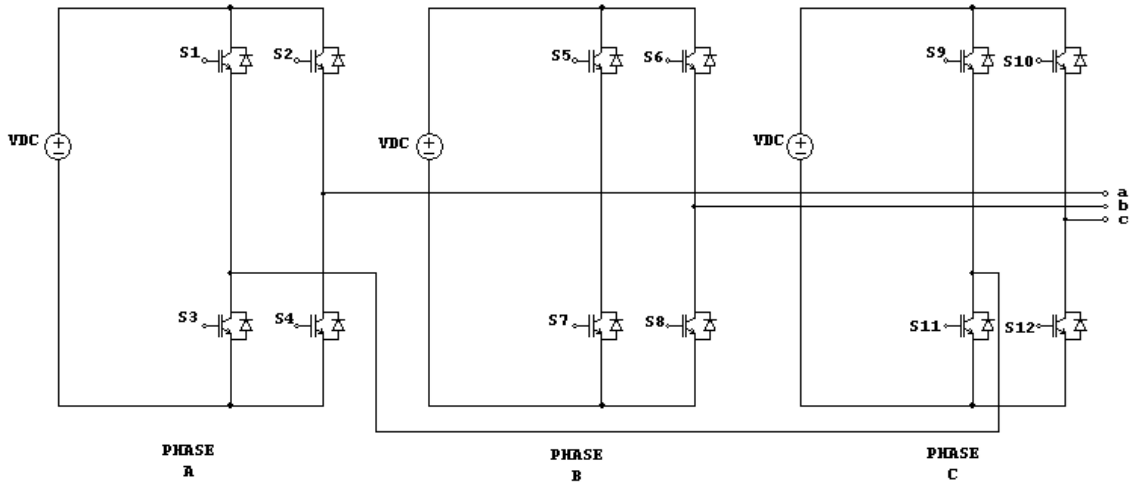

Figure 2.8: Three-phase three-level cascaded H-bridge converter.

Figure 2.8 shows the complete circuit of a three-phase three-level cascaded H-bridge converter topology. It can be seen that identical DC voltage sources are supplied to each H-bridge for each phase. The switching sequences are the same for every phase. It is only that the switching signals are shifted by 120° for each phase. As for the three-phase three-level cascaded H-bridge, the maximum possible number of line voltage levels is 5. Table 2.4 shows the switching sequence of an H-bridge circuit with its corresponding output voltage.

Table 2.4: Switching combinations of three-level cascaded H-bridge converter per phase.

Switching States				Output Voltage
S1	S2	S3	S4	
1	0	0	1	$+V_{DC}$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-V_{DC}$

Table 2.4 presents the switching combinations per phase. For a complete three-phase three-level NPC converter, the output line voltage will have five levels which are at ±100 % V_{DC}, ±50 % V_{DC} and 0 % V_{DC}. On the other hand, the output phase voltage will have nine levels which are at ±66 % V_{DC}, ±50 % V_{DC}, ±33 % V_{DC}, ±16.5 % V_{DC} and 0 % V_{DC} [23].

2.4 Pulse Width Modulation (PWM) Techniques

There are several types of PWM methods that can be implemented on inverter topology. Three of the most widely used PWM methods are carrier based PWM, selective